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Design of 3-Bit ADC in 0.18µm CMOS Process

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Abstract

Analog-to-digital converters (ADCs) are required to convert the real world analog signals into digital signals, as digital signals are more robust and easier to handle. Signal processing is increasingly being done in the digital domain along with the escalating levels of integration have forced ADC to reside on the same chip as digital circuits. The study describes the design method of 3-bit ADC using CEDEC 0.18 µm CMOS process. The designed ADC consists of; voltage divider, comparator and 7-bit encoder circuits. The pre-simulation has done with ELDO simulator with low power supply voltage (VDD) 1.8 V. The simulated results showed that the designed 3-bit ADC is able to convert analog signals to digital signals.

Keywords: *CMOS, ADC, vomparator, encoder, voltage divider*

1. Introduction

The trend toward increased integration of analog and digital circuitry requires data converters that can be embedded in large digital ICs [1-8]. Mixed-signal applications such as Partial Response Maximum-Likelihood (PRML) read channels and gigabit Ethernet require high-speed low-resolution ADCs, which are usually implemented with the flash architecture. These applications rely heavily on DSP, which performs best when implemented on the finest geometry CMOS process [9-15]. On the other hand, ADCs with analog circuits in general, tend to function best when fabricated on more mature CMOS process. CMOS based ADCs are utilized in a number of applications as the sources of store data in RFID application [16-23].

An Analog to Digital Converter (ADC), which converts the analog signal to digital output, is composed of three different stages that consist of voltage divider, comparator and encoder. Comparators are the key analog building block of any flash ADC and strongly influence performance. A high degree of comparator accuracy is essential for good ADC performance. However, integration of analog circuitry in low voltage scale VLSI technologies results in degraded precision due to large device mismatch and limited voltage swing. Reduced precision can be compensated for offset correction schemes. Analog offset correction techniques are typically used, but these schemes are increasingly difficult to implement in modern CMOS processes. Therefore, the issue of comparator offset is becoming a bottleneck in the design of flash ADCs [25-29].

This study presents an improved 3-bits ADC circuit, which is designed using CEDEC 0.18 µm CMOS process. The designed ADC circuit has three sub circuits; voltage divider, comparator and the encoder circuit. This paper is organized with the architecture of the 3-bits ADC circuit. Then, the design methodology of the comparator, encoder circuits are presented. After that, the simulated results, the comparison study among other designed ADC circuits and conclusions are given, respectively.

2. Architecture

A typical flash ADC block diagram is shown in Figure 1. The input signal is compared to the 2^n nodes of resistor and the sampled input value is decoded into binary code. There are many different types of architectures, each with unique characteristics and different limitations. Flash ADCs, also known as parallel ADCs, are the fastest way to convert an analog signal to a

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digital signal [25]. Flash ADCs are ideal for applications requiring very large bandwidth; however, they typically consume more power than other ADC architectures and are generally limited to 8-bits resolution [30-31].

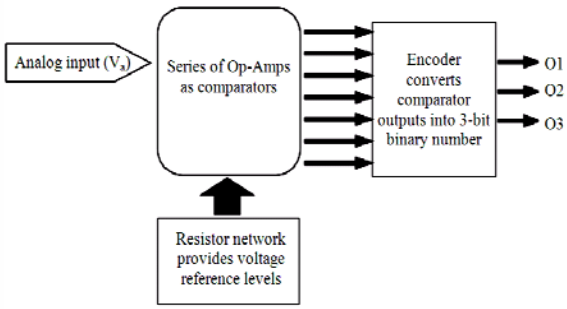

Figure 1. Block Diagram of 3-bit Flash ADC

As shown in Figure 1 the flash ADC is composed of three major components: resistors string, comparators and encoder. The analog input voltage is concurrently compared to the reference voltage levels provided by the resistor network string. The comparison maximizes the speed of the conversion of the ADC circuit. The outputs of comparators are encoded by the encoder block, which is a combination of a series of zeros and a series of ones, e.g., 000...011...111. Because binary code is usually needed for digital signal processing, an encoder code is then transformed to a binary code through an encoder, to get the desired 3-bits binary number for the ADC. The cost of such a traditional encoder increased exponentially with the resolution. Optimizations on area cost, circuit latencies and power consumptions are greatly expected. In this research, low power comparator circuit is designed to minimize the cost [32].

3. Methodology

As mentioned earlier, in order to design the components of the 3-bit ADC, CEDEC 0.18 µm process have been used to design the circuit diagram and the layout of all the three components of the ADC circuit. Figure 2 shows the schematic diagram of 3-bit ADC circuit. In the schematic diagram as shown in Figure 2 it is clear that 3-bits ADC circuit is composed of voltage divider circuit, comparator block and the encoder circuit.

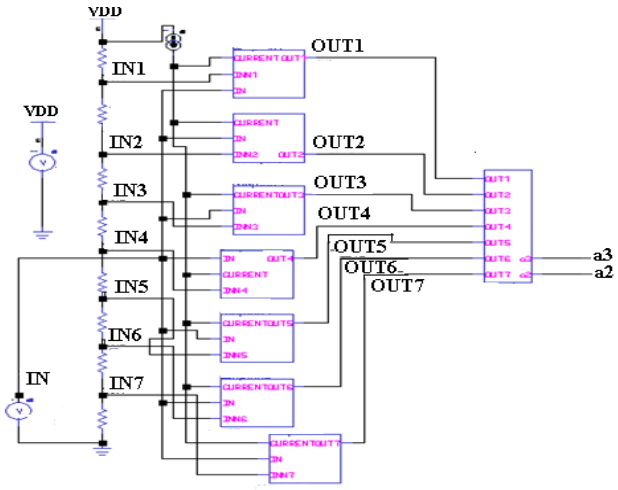

Figure 2. Schematic Diagram of 3-bits ADC Circuit

The circuit diagram of the voltage divider by using 8 resistors, which serially connected is shown in Figure 2**.** Each resistor value can be obtained by making resistor R1 at 750Ω, R2 to R7 at 500Ω and R8 at 250Ω with Vdd at 1.8V.

All the outputs of the voltage divider circuit are compared with the comparator circuit diagram as shown in Figure 3. Two outputs from each voltage divider circuit are taken as the input signals for each comparator circuit to produce one-bit output signal. To design the comparator circuit as shown in Figure 3 current mirror method has been utilized. In the comparator stage, an operational amplifier has been used as comparator. To design a complex comparator 3 pMOS and 5 nMOS are required.

To design 3-bit ADC circuit as shown in Figure 2, **7** comparators have been required to produce 7 output bits. All the 7-bits output is taken as the inputs for the 7-bits encoder circuit, which eventually produce the 3-bits ADC signals. For the convenience, the three sub circuits are designed and simulated separately. Finally, all the three components are combined together and tested at physical description level based on available CEDEC 0.18μm CMOS process.

The outputs of the comparator circuit is required to use as the inputs of the encoder circuit, which is also drawn using CEDEC 0.18 μm CMOS process DA tools as shown in Figure 4. To design the encoder circuit, “CEDEC standard cells” logic gates are utilized. All the outputs of the comparator circuit is used as the 7 inputs for the designing of the encoder circuit using five inv01a and seven nand02a logic gates.

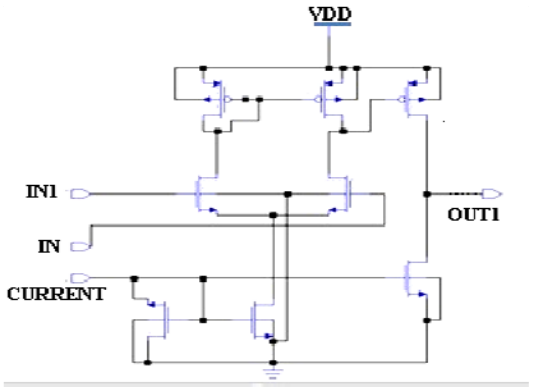

Figure 3. Schematic Diagram of Comparator Circuit for 3-bits ADC

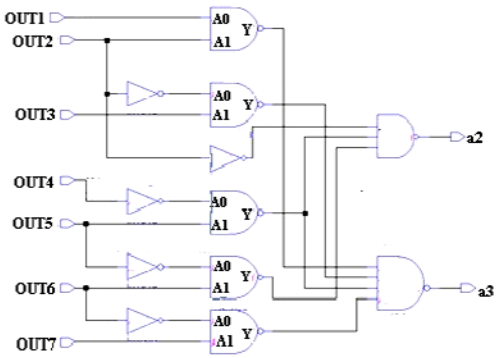

Figure 4. Selected Logic Gates for 7-bits Encoder Stage

4. Results and Analysis

The The ADC circuit is designed in CEDEC 0.18-μm CMOS process. The enhanced ADC circuit has been verified by using the ELDONET simulator of the CEDEC process. Figure 5 shows the simulated output results for the comparator circuit.

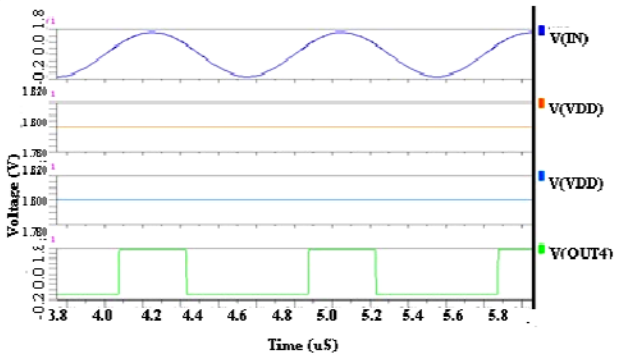

Figure 5. Simulation results for the comparator circuit

In the coding stage for 3-bit ADC, the circuit design and MOS layout should consist of simple logic circuit with 7 inputs and 3 outputs according to the output equation of O1, O2 and O3 from the truth table as shown in Table 1.

Table 1. Input and output of encoder

Input OUT1	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
OUT2	0	0	0	0	0	0	1	1
OUT3	0	0	0	0	0	1	1	1
OUT4	0	0	0	0	1	1	1	1
OUT5	0	0	0	1	1	1	1	1
OUT6	0	0	1	1	1	1	1	1
OUT7	0	1	1	1	1	1	1	1
O1	0	0	0	0	1	1	1	1
O2	0	0	1	1	0	0	1	1
O3	0	1	0	1	0	1	0	1

After designing all three stages of the 3-bits ADC, all the different components are simulated and verified. Finally, all the three components are combined to form a 3-bits ADC circuit, which is simulated and verified again to get the desired output signals as illustrated in Figure 6.

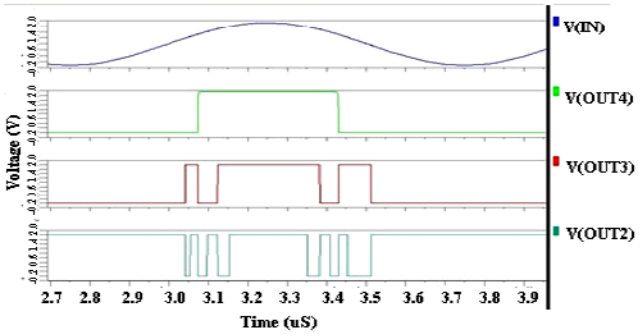

Figure 6. Simulated Output Results for the Test of 3-bits ADC Circuit

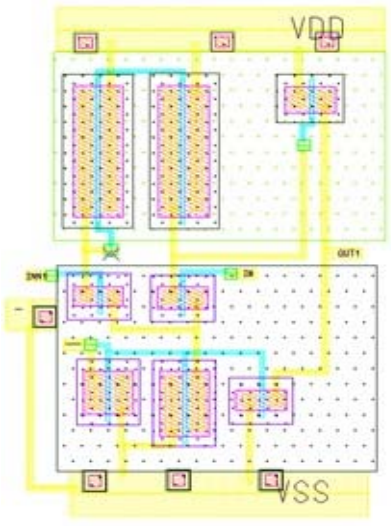

Figure 7. Layout Diagram of Comparator Circuit

The layout diagram for the comparator circuit is shown in Figure 7. After successfully design the schematic diagram of comparator circuit, the design has been simulated and with the successful simulation result, the designed is prepared for the layout diagram, which is shown in Figure 7.

It is found that, with the power supply voltage 1.8V and the input analog signals as V (IN) the comparator is successfully produce the output results asV (OUT), which is shown in Figure 5.

It is observed that the results meet the requirement of the truth table indicated in Table 1. The input value of the OUT4 is same for the output O1.

The simulation result in Figure 6 shows that a proper conversion is happened with the analog input signal to digital output signal. It is observed that the signal is interpreted well beginning from the early stage to the final stage and the output obeyed the theoretical truth table of 3-bits ADC.

Flash analog-to-digital converters, also known as parallel ADCs, are the fastest way to convert an analog sign to a digital signal. Flash ADCs are ideal for applications requiring very large bandwidth; however, they typically consume more power than other ADC architectures and are generally limited to 8-bits resolution [32]. To achieve low-power consumption with high conversion-speed and to enhance design reusability in terms of digital implementation with more regular mask patterns, the time-domain comparison is devised in the flash ADC. The prototype, which has been fabricated in a standard 0.18 um CMOS technology, achieves a FOM of 0.91pJ/conv. Although no low-power digital circuit technique has been comprised, further low-power operation can be easily achieved by voltage scaling or reduction techniques of leakage power. Table 2 provides the performance analysis and the comparison study of the different ADC circuits.

Table 2. Performance Comparison

Parameters	This study	[28]	[31]	[32]
Technology (CMOS)	0.18 μm	0.18 μm	0.18μm	0.13 μm
Resolution	3-bit	5-bit	8-bit	6-bit
Architecture	Flash	Time-Domain Flash	SAR - Flash	Flash
Supply voltage	1.5 V	1.8 V	1.2 V	1.5V
Power consumption	36.327 mW	8mW	166 nW	160 mW
Chip area	1.044 mm²	0.132 mm²	0.132 mm²	0.12 mm²

4. Conclusion

In this research, design of 3-bits ADC using CEDEC 0.18 μm process is described to convert the analog input signal to digital output signal. Moreover, 3-bits flash ADC architecture with low hardware complexity and low latency is proposed. All the three sub circuits; voltage divider, comparator and encoder have been designed successfully to comply with the ADC circuit. However, this 3-bits flash type ADCs have limitations such as the device is accurate for the conversion of analog voltage to digital form from 0 to 3 voltage in amplitude and for accurate result the input voltage should be greater or lesser than the reference voltage of the comparator about ±0.05 volt. Moreover, this architecture can be extended to medium-to-high resolution applications because this simplicity of the circuit.

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