TELKOMNIKA Indonesian Journal of Electrical Engineering
Vol.12, No.7, July 2014, pp. 5191 ~ 5196
DOI: 10.11591/telkomnika.v12i7.5209

Digital Image Storage System Based on USB and NAND Flash

Yongjun Cui*[1], Wei Liu[2]
[1]National Key Laboratory for Electronic Measurement and Technology, North University of China, Taiyuan 030051, China
[2]Key Laboratory of Instrumentation Science and Dynamic Measurement of Ministry of Education, North University of China,
Taiyuan 030051, China
*Corresponidng author, e-mail: Cui234@163.com[1], liuwei0665@163.com[2]

Abstract

Focusing on the storage of large number of digital image information, a system is designed which based on USB bus and NAND-type FLASH using alternating two-plane page program. The aim of this study is to short the writing-reading FLASH time and improve the transmission of data in order to enhance the efficiency of the system. In hardware implementation, the paper introduced the interface between every module especially the USB connection. In software, detailed analysis of the key technology about the alternating two-plane page program was shown. By commissioning, the speed of data stored in the FLASH is 30MB/s, achieving fast data storage and accurate feedback purposes, making sure that the data was reliable.

Keywords: *USB, transmission, storage, FLASH, alternating two-plane page program*

1. Introduction

Nowadays measurement and contral technology have grately changed our society. In many areas such as industry, aerospace, we measure whether the devices can work stable or not according to the feedback data. In these measurements, countless data was got so the storage speed is critical to effenciency of the system. In aerospace, some equipments need to collect huge number of digital image information, and the data transmission between them and ground test benches require a high transfer rate [1-3]. The accuracy of data transmission influences the precision of the system [4].

Recently, the data was proposed to be transmitted in high-speed and long-distance. It's high time for us to find new way to achieve the requirements. At present, the physical interface unable to meet the required data transfer rate. The commonly used RS-422 interface, which the maximum transmission speed of twisted is 1Mb/s in per one hundred meter [5, 6]. Speed and distance like this can not meet these transmission requirements.

In this paper, a new system was designed to meet the high-speed, long-distance transmission and accurate storage of the digital image information. These requirements were achieved using USB interface, LVDS technology and NAND-type FLASH for alternating two-plane page program. USB has many features like faster speed, hot-swappable, and it has been widely used in various devices [7, 8]. LVDS technology provides a solution to fast long-distance transmission. For NAND-type FLASH K9WBG08U1M, using the method of alternating two-plane page program, data can be stored quickly. USB technology combined with alternating two-plane page program achieves the purpose of fast data transmission, storage and accurate feedback [9, 10]. This method provides a new approach to the transmission and storage of a large number of images.

2. Overall System Design

The design is based on USB technology and alternating two-plane page program. The system uses a modular design approach, that's to say various components are distinct in composition but functionally complement. The great breakthroughs in the design are accurate

Received November 26, 2013; Revised March 19, 2014; Accepted April 3, 2014

and fast data storage and high-speed transmission. They are the bottlenecks troubled acquisition system technology development. Data acquisition and storage system includes FPGA master interface module, USB communication interface and timing control design of read-write operation, logic design of one pair of parallel FLASH.

Figure 1 shows digital image acquisition and storage system work flow. Specific operational procedures: a video or a complete picture is divided into a continuous picture frames. USB chip FT245RL makes the picture transmitted to the acquisition and storage system. Under the control of FPGA, the download data are stored in two parallel FLASH chip K9WBG08U1M medium. When the image needs to be sent, the three groups of data stored in the FLASH would be fast read out. Through the MAX9247, 16-bit parallel data would be into serial data and be sent as the LVDS module to the image store and transfer device. One group of the three would be stored in the image store and transfer device .Another way would be transmitted to downstream equipments in PCM code for them to be obtained. The third way would be read-back to the host computer similarly in PCM code.

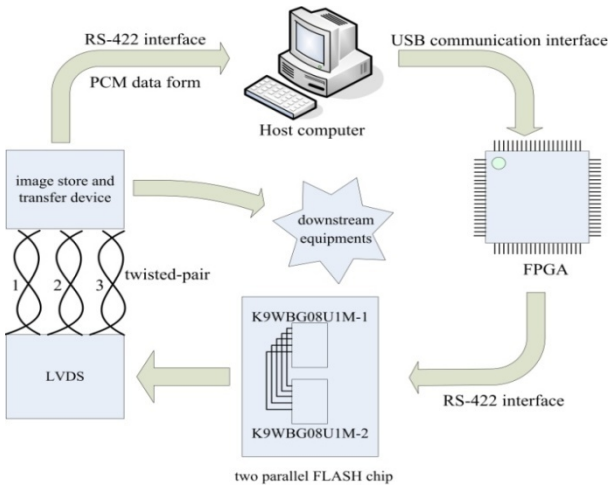

Figure 1. Digital Image Acquisition and Storage System Work Flow

3. Hardware Components of the System

Digital image acquisition and storage system in terms of hardware mainly by the power module, USB interface module, FPGA control module and FLASH memory modules.

FPGA is the digital image acquisition and storage control core, controlling the image data reception, conversion, storage and transmission. Digital image data acquisition interface uses the PCM form, while memory and logic control units adopt TTL level. PCM interface circuit is structured by PCM interface chip SN65HVD10, completing TTL → 422 and 422 → TTL level converter. DS92LV18 chips compose acquisition and storage system feedback interfaces which with both internal integrated deserializer and serializer [11]. In this design, DS92LV18 works as a deserializer. When the acquisition and storage system receives the serial differential signal, the DS92LV18 would make them into a 16-bit parallel data and then send to FPGA. When FPGA receives the data, it would upload to the PC for analysis.

Communication between control board and PC relys on USB communication interface; It has many features, such as high data transfer, can be hot-swappable, flexible application, etc. [12]. In the digital image acquisition and storage system design, FT245RL was being choosen as USB communication chip. It had been integrated firmware library, so eliminates the need for additional complex programming. USB interface circuit connection diagram was shown in Figure 2. In the figure, ACM-2010-900-2P is the common-mode inductance and R24 is a ferrite bead. Adding these two small modules in USB interface circuit, they reduce the mutual interference between the FPGA and the USB device. In the process of the PCB layout, to ensure that the data lines D0 ~ D7 are equal in length and as short as possible in order to achieve the purpose of weakening external electromagnetic interference.

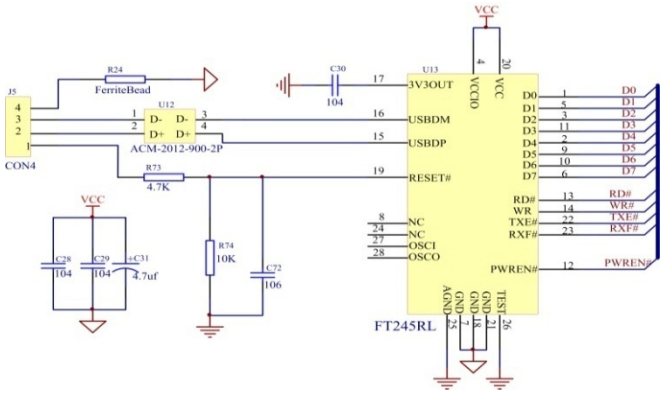

Figure 2. USB Interface Circuit Connection Diagram

4. Key Logic Design

Logic control main achievements: USB read and write functions; using alternating two-plane page program for the next pass of the image data storage, read and erase functions; putting forward the image data stored in the image store and transfer device to the main control computer.

4.1. USB Read-write Logic Design

Channel A in FT245RL chip can be set to synchronous FIFO mode. In this operating mode, data is written or read out on the rising edge of the CLKOUT. Reading and writing can not be operated simultaneously.

When reading the FT245RL, RXF # has the highest priority. When the FIFO data to be read out, RXF # is low, at the same time, the output enable signal OE # is low, then, the read enable signal RD # changes to low. In this operating mode, only both the RXF # and RD # are low, the data will be read out. The data coming from the FIFO would be output to the A-channel 8-bit data port at the RD # falling edge. Then the RD # is pulled high, achieving a byte read operation. During a write operation, TXE # priority is in the highest level. So determining the level TXE # is the most important. If low, write operation can not be performed; in the opposition, writing can be performed. When TXE # is low, the write enable signal WR is set to high and writing data. Then the WR low, data will be sent to the FIFO, completing a byte write operation. USB internal FIFO read and write timing shown in Figure 3.

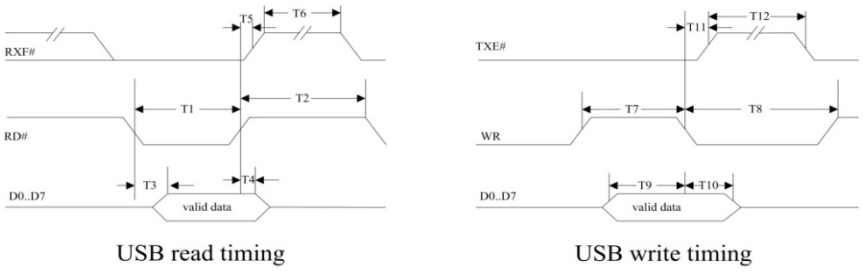

Figure 3. USB Internal FIFO Read and Write Timing

4.2. Alternating Two-plane Page Program Logic Design

K9WBG08U1M is a NAND-type FLASH memory chip and the data width is 8. But the data need to read, write and storage achieve to 16-bit. To fulfill this requirement, generally the data was dividing into two 8-bit data and then store them in a K9WBG08U1M twice. This method is feasible, but it spends execute two stored procedure in storing a 16-bit data, which greatly restricts the storage rate. That means it can't reach the technical requirements of fast storage. In this design, FLASH K9WBG08U1M-1 and K9WBG08U1M-2 were used in parallel to

achieve the 8-bit memory changed into 16 bits wide purpose. Specific operation is putting the two chip select pin CE, command enable pin CLE, address enable pin ALE, read and write enable pins WE, RE series, and each chip R/B pin respectively. Thus, the two chips can simultaneously write command or address, comparing with ordinary method, storage speed doubling. Independent of R/B pin is the control basis of alternating two-plane page program. FLASH pin parallel connection diagram shown in Figure 4.

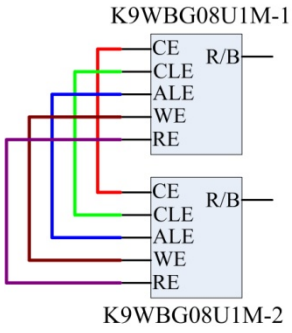

Figure 4. Paralleled FLASH Pin Connection Diagram

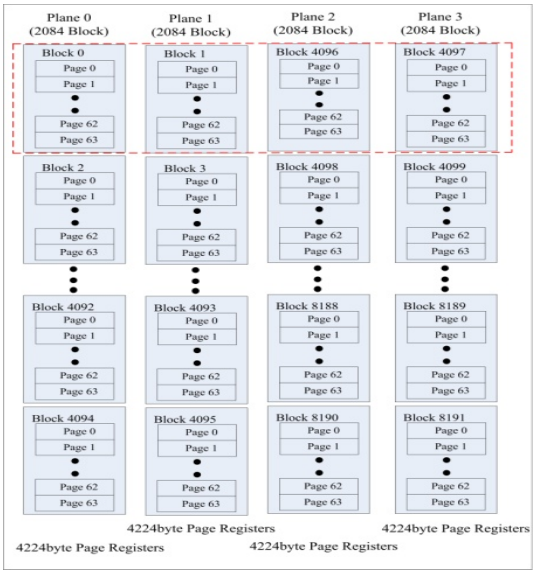

Figure 5. Internal Structure

K9WBG08U1 chip is divided into 8192 Block and each Block comprises a total of 64 Page, numbered from 0 to 63. Every 2048 Block makes up a Plane. During the Block number ranged from 0 to 4095, the even numbered Block compose Plane0, odd Number Block consist Plane1. During Block 4096 ~ 8191, with the former division, it is divided into Plane2 and Plane3. Figure 5 shows the internal structure.

K9WBG08U1 internal data storage is a one Page carried out. Such a page program can be divided into command, address and data loading process and automatic programming of the implementation process. Loading process means controlling by the external clock, the command, address, data and other information written into the internal registers. Automatic programming process is the chip according to the loaded information putting the data stored to the corresponding position. So the process of data storage is finished. The time it takes is programmed time, usually between the 200us ~ 700us. According to the chip information, the speed of read and write to the FLASH chip is 40MB/s. The time required to read or write one data is:

$$T_{WR} = \frac{1}{40M} \times 4K = 102.4\mu s \quad (1)$$

The general page program is a sequence. Firstly, load one unit's command, address and data, then automatic programming. Following this speed calculation, the write speed of FLASH is:

$$V = \frac{4096byte}{200\mu s + 102.4\mu s} = 13.54MB/s \quad (2)$$

This speed can not meet the requirement of the mission statement. The choice of alternating two-plane page program will enable the programming time greatly reduced. Alternating two-plane page program operation is as follows: First, write into K9WBG08U1M-1 in the Block0 Plane0 Page0, followed by written K9WBG08U1M-1 Plane1 Block1 Page0, as shown in Figure5 red box. When returned to the Plane0 K9WBG08U1M-1, it is already gone 25ns × 4096 × 7 = 716.8us, greater than tPROG (tPROG stands for the programming time) maximum 700ns. So it will not affect Plane0 to make the second operation. Such reuse of time can shorten the time of the loading process which has greatly improved the storage speed. FLASH write process is shown in Figure 6.

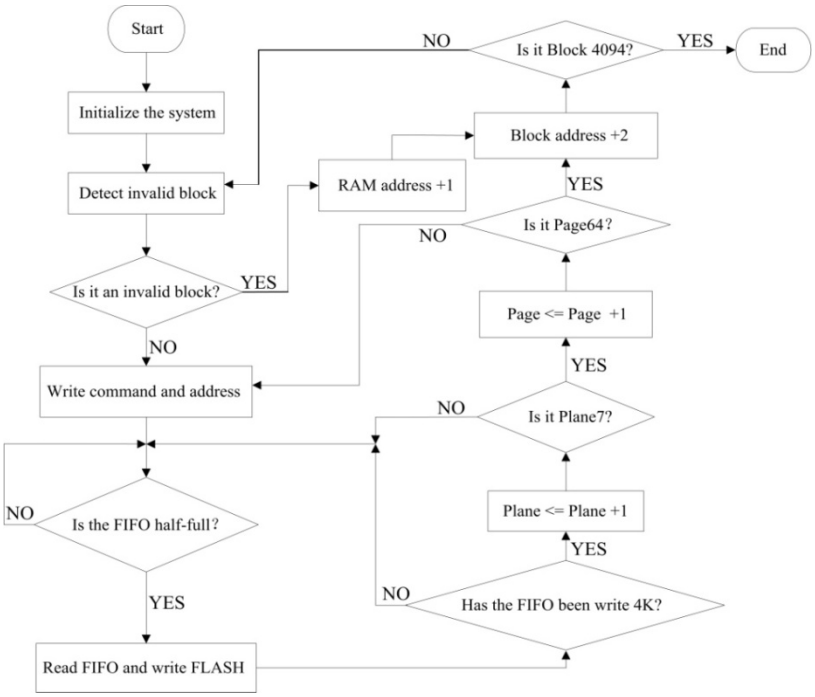

Figure 6. FLASH Write Process

In memory chip parallel operation mode, when powered on digital image acquisition and storage system immediately makes bad blocks monitor. As long as there is an invalid block, the entire block will be deemed to be invalid block. Such invalid block address integrated management, greatly facilitates the streamlined alternating two-plane page program operation, reducing the complexity of the control logic and enhance the storage speed.

4.3. Issued and Upload the Image Data Process Flow

Image data issued process: makes the issued picture or video into a continuous frame format. The frame image is encoded adding self-signs and frame signs, and then send the image data to the next.

Image data read-back process: the host computer uses USB interface to make the collected or image data read back transmitted to the PC. PC receives image data and calculates the error rate, then showing in the form of animation, the frame image playback. Finally, the results of data analysis would generate files and save in the specified directory.

5. Results and Discussion

When each module individually tested successfully, each module is connected, making the entire system functional test. Experimental results show that data stored in the FLASH at the speed of 30MB/s. It is better than the maximum transmission speed of twisted is 1Mb/s in per one hundred meter by the commonly RS-422 interface. Through some changes, the host

computer gets the issued data from the image store and transfer device. PC analysis software can compare the read back data and sending raw data, and we can restore the image to be displayed. Testing phase, issued a good cyclical picture, and displayed the received data through the PC software. Data comparison showed that error rate is 0. The decrypted data is read back by the host computer. The data is shown in graphics in Figure 7. It is more easily to observe the experimental results.

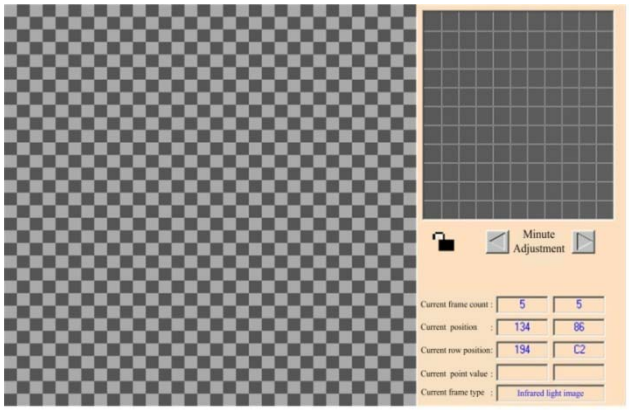

Figure 7. Data Shown in Graphics

6. Conclusion

To achieve a large number of digital image signal acquisition and storage, a design based on USB and alternating two-plane page program is proposed. The system achieves a fast storage, high-speed transmission and accurate feedback in the use of the two technologies. Actual test results have fully proved that the proposed design correctness and reliability.

References

[1] Bai Xianmin, Zhang Yating, Zhan Jianhua, Liu Wenyi, Han Huilian. The high-speed data acquisition system based on LVDS interface and two-plane flash-operating way. *IEEE 2nd International Conference on Software Engineering and Service Science*. 2011: 516-519.
[2] Zhang Huixin, Guo Zheng, Ye Yong. Design of high-speed remote image data storage memory based on LVDS. *Advanced Materials Reasearch*. 2013; 605-607: 1989-1993.
[3] Wei Zukuan, Kim Hongyeon, Kim Youngkyun, Kim, Jaehong. An efficient content based image retrieval scheme. *TELKOMNIKA Indonesian Journal of Electrical Engineering.* 2013; 11(11): 6986-6991.
[4] Bisht Amit Singh, Rathod Somsing, Varadarajan V, Kumar S. Yogeesh. *FPGA based hardware design of high speed compact T/R unit controller.* Proceedings of the International Conference on Electromagnetic Interference and Compatibility. 2008: 573-577.
[5] Wang Hongliang, Wang Hairui, Ding Haifei. Design of data acquisition and storage system for digital and analog signal based on FPGA. *Advanced Materials Research.* 2013; 605-607: 955-959.
[6] Dietz Jim, Hubbard Richard. The secrets of successful communications using LVDS. *EDN.* 2005; 50(21): 89-92.
[7] Xu Jian, Wang Zhigong, Niu Xiaokang. Design of high speed LVDS transceiver ICs. *Journal of Semiconductors.* 2010; 31(7): 11-14.
[8] Pravossoudovitch S, Godard B. *NAND flash testing: A preliminary study on actual defects.* Proceedings - International Test Conference. 2009.
[9] Tseng, Hung-Wei, Grupp, Laura M, Swanson Steven . *Underpowering NAND flash: Profits and perils.* Proceedings - Design Automation Conference. 2013.
[10] Hyde John. Interconnecting USB devices. *Electronics World.* 2011; 117(1906): 44-45.
[11] Szecowka, Przemyslaw M Pyrzynski, Kamil J. *USB receiver/transmitter for FPGA implementation.* International Conference on Signals and Electronic Systems, ICSES 2012 - The Conference Proceedings. 2012.
[12] Shujing Su, Jiansheng Lei. A method of multi-channel data acquisition with adjustable sampling rate. *TELKOMNIKA Indonesian Journal of Electrical Engineering.* 2013; 11(9): 5299-5307.