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Circuit Design of Digital Closed Loop Control System for FOG

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Abstract

Fiber optic gyroscope (FOG) is a new angular rate sensor based on the Sagnac effect. It has been widely applied in the navigation control system of aircrafts, spacecrafts and ships. But its stability, reliability and miniaturization are always the research focuses and difficulties. This paper presented a circuit design method for the digital closed loop control system of FOG based on FPGA. Based on a large number of experiments, this paper summarized the parameter demands for each module of closed loop control circuit and designed a corresponding circuit using FPGA. The proposed dual closed loop technique improved the zero offset stability of FOG. The using of FPGA brought the digital signal processing by software, the system reliability and agility enhancement as well as the system miniaturization. Particularly, we discussed the problems of component selection and the anti-jamming measures for PCB design to improve the performances of the system. We also developed some samples of FOG using this design method. The experiments and tests show that the proposed method is efficient and valuable. The stabilities of zero-offsets of all samples are less than 0.075deg/h.

Keywords*: fiber optic gyroscope, circuit design, digital closed loop, second closed loop, FPGA*

1. Introduction

As a new angular rate sensor, the fiber optic gyroscope (FOG) has many advantages, such as completed solid state, small size, light weight, long using life, low cost and high anti-impact capability [1]. It has been paid widely attention by the world and increased investment in its research and development annually. It also has been applied to the field of the inertial measurement in the areas of space productions, military productions and civilian productions.

The basic principle of interferential FOG based on the Sagnac effect [2-7] and the reciprocity theorem of its component are introduced in this paper. The work characteristics of the digital closed loop applied to FOG are also analyzed. According to the design requirements, the digital closed loop feedback control system of FOG is implemented. On the basis of the amount of testing, the parameter adjustments of modules in the closed loop control system are summarized, and the relevant circuit is schemed out. At the same time, we discuss the component selection and the issues of anti-jamming in PCB design in detail. Finally, we develop some samples of FOG using the hardware design method proposed in this paper and combining the relevant software development in FPGA.

This paper is organized as follows. In section 2, we introduce the control technique of digital closed loop for FOG. Section 3 presents the circuit design method of digital closed loop system for FOG in detail. Section 4 gives some considerations for the hardware design. Section 5 shows a good performance of FOG samples through experiment testing. Section 6 gives the conclusions of this paper.

2. Technique of Digital Closed Loop Control for FOG

2.1. Main Frame

In passed years, the digital scheme of FOG occupied a dominant position gradually. Its principle can be described by a style, in which the original analog signal should be quantified a digital available measuring range quantity as early as possible and be processed in digital field,

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then the processed digital signal should be converted into an analog signal by D/A convertor to control the system.

The typical system mainly consists of optical source generator, photoelectric detector, A/D convertor, digital logic module, D/A convertor, optical integrated component (coupler, Y-waveguide) and optical fiber ring [8-10]. Its frame is shown as in Figure 1. In this system, we input the phase modulation signals with the ladder wave and square wave into the interferometer through the optical integrated component. The ladder wave is applied to counteract the Sagnac phase shift through closed loop feedback control. The square wave is as an offset signal to enable that the output signal of the Sagnac interferometer has a linear relationship with the phase shift signal. The step height of the ladder wave is the measured Sagnac phase shift, which is the angular rate signal. In this scheme, besides the output of detector, the drive signals of ladder wave and square wave, the main signal processing is done in the digital field to avoid the circuit noises and to improve the measuring precision [11]. Hence, this scheme is one of the main methods of signal processing system for the medium or high precision FOG.

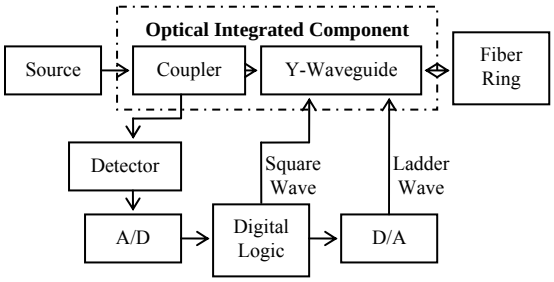

Figure 1. Frame of Closed Loop Control System of FOG

2.2. Basic Principle

The phase difference of FOG can be obtained through measuring the intensity of the output of the photoelectric detector. The light intensity variable P of the output from the Sagnac interferometer has a relationship with the Sagnac phase shift △・S as following [11]:

$$P = P_{\mathrm{d}}\left[1+\cos\left(\Delta\phi_{\mathrm{S}}+\Delta\phi_{\mathrm{FB}}+\phi_{\mathrm{f}}\right)\right] \tag{1}$$

Where P_{d} is the amplitude of light intensity, ・f is the phase shift generated by the square wave modulation as shown in Figure 2, and △・FB is the phase shift of ladder wave generated by the closed loop control system as shown in Figure 3. From this equation, we know that the light intensity is a cosine function of phase shift. But, the output light intensity can not reflect the direction of rotation, and the system has a lower sensitivity. Therefore, the system should be added a nonreciprocal ±π/2 phase offset through the square wave modulation. In the light path, we draw two alternative phases with the values of π/2 and -π/2 into two lights in the opposite directions. These two states have their own output light intensities respectively:

$$\begin{aligned} P_2 &= P_{\mathrm{d}}\left[1+\cos\left(\Delta\phi_{\mathrm{S}}+\Delta\phi_{\mathrm{FB}}+\pi/2\right)\right] \\ &= P_{\mathrm{d}}\left[1-\sin\left(\Delta\phi_{\mathrm{S}}+\Delta\phi_{\mathrm{FB}}\right)\right] \end{aligned} \tag{2}$$

$$\begin{aligned} P_1 &= P_{\mathrm{d}}\left[1+\cos\left(\Delta\phi_{\mathrm{S}}+\Delta\phi_{\mathrm{FB}}-\pi/2\right)\right] \\ &= P_{\mathrm{d}}\left[1+\sin\left(\Delta\phi_{\mathrm{S}}+\Delta\phi_{\mathrm{FB}}\right)\right] \end{aligned} \tag{3}$$

To do the different demodulation for equation (2) and (3), we obtain:

$$\Delta P = P_2 - P_1 = -2P_{\mathrm{d}}\sin\left(\Delta\phi_{\mathrm{S}}+\Delta\phi_{\mathrm{FB}}\right) \tag{4}$$

In the Equation (4), the Sagnac phase shift △・$_S$ is always approximately equal to △・$_{FB}$ and their signs are opposite, because the added ladder wave is used to counteract △・$_S$. Therefore, △・$_S$ +△・$_{FB}$ is always approximately equal to 0, then we have:

$$\begin{aligned}\Delta P &= -2P_d \sin\left(\Delta\phi_S + \Delta\phi_{FB}\right) \\ &= -2P_d \sin\left(\Delta\phi\right) \approx -2P_d \Delta\phi\end{aligned} \tag{5}$$

Apparently, if △・$_{FB}$ can counteract completely △・$_S$, that is △・=0, △P should be equal to zero. If △P≠0, it is said that the nonreciprocal phase shift generated by the ladder wave does not counteracts the nonreciprocal phase shift caused by rotation yet. This time, we can take ΔP as an error control signal to change the step height of ladder wave through the closed loop system to counteract △・. The additive nonreciprocal phase shift generated by ΔP through the closed loop system is:

$$\Delta\phi' = K\Delta P \tag{6}$$

Where K is a scale coefficient to generate the nonreciprocal phase shift through the closed loop system. Then we have:

$$\begin{aligned}\Delta P_1 &= -2P_d\left(\Delta\phi + \Delta\phi'\right) \\ &= -2P_d\left(\Delta\phi - 2P_d K\Delta\phi\right) \\ &= -2P_d\Delta\phi\left(1 - 2P_d K\right)\end{aligned} \tag{7}$$

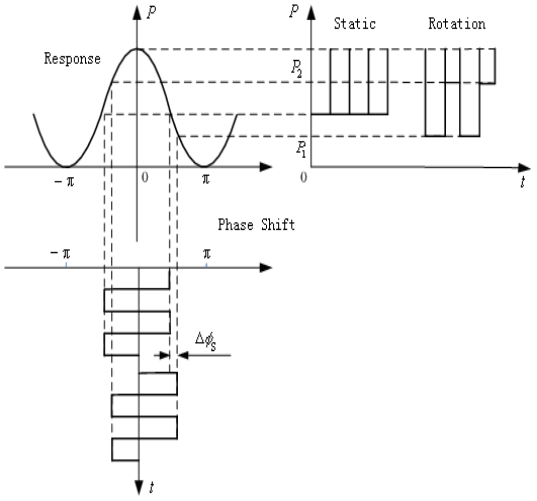

Figure 2. Schematic Diagram of Square Wave Modulation

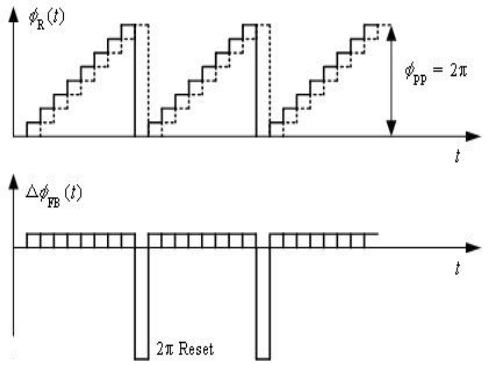

Figure 3. Schematic Diagram of Ladder Wave Modulation

In Equation (7), if 2$P_d K$=1, then △P_1 =0, that means the control error of the digital closed loop system is zero, it is indicated that the closed loop reaches balance. If 2$P_d K$≠1, then the closed loop feedback control will be continued. After feedback controlling n times, the system will be in a state as following:

$$\Delta P_n = -2P_d\Delta\phi\left(1 - 2P_d K\right)^n \tag{8}$$

From Equation (8), we know that when 0<$P_d K$<1/2, the closed loop system can be monotonic convergence and will reach the balance gradually. The condition 0<$P_d K$<1/2 can be ensured by the system design.

When the closed loop system reached the state of balance, the angular rate of rotation can be calculated by the equation as following and be measured by the FPGA module.

$$\Omega = -\frac{\lambda C}{2\pi LD}\Delta\phi_{\mathrm{FB}} \tag{9}$$

Where λ is the wavelength of the optical source, *LD* is the product of the length of optical fiber rings and the diameter of optical fiber ring.

3. Circuit Design

3.1. System Frame Based on FPGA

The scheme used in this paper is the continuation of the traditional idea for designing the closed loop control system of FOG, which consists of 6 components such as optical source generator, integrated light path, coupler, optical fiber ring, photoelectric detector and drive control circuit.

Structurally, we choose the integration solution of aluminum alloy material, i.e., the optical source control circuit board and the closed loop control circuit board are fixed in the body of optical fiber rings. We select the super luminiferous diode with a property of wide spectrum as the optical source and do constant power control in whole temperature range (-40~60℃) using the optical source control circuit board. The used optical fiber is the polarization maintaining fiber and the rings are winded by the quadrupole symmetrical winding pattern [12]. The total length of the fiber coil is about 650m.

FPGA is a logic gate array, which is composed of many independent macrocells. These macrocells can be marked out some mutual non-interferential logic units, which can work in parallel style. The signal exchange between the different logic units can be realized through simple logical connections or some trigger levels [13]. This digital logic completely fits the demands of the application of the closed loop control system for FOG.

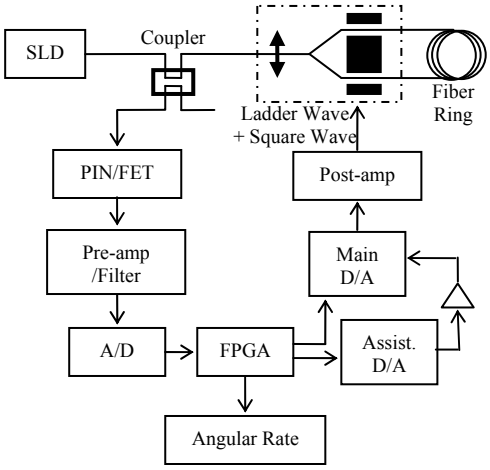

Figure 4. Frame of Closed Loop Control System of FOG Based on FPGA

The FPGA based scheme is shown as in Figure 4. We choose PIN/FET with bandwidth about 7~8MHz as the photoelectric detector. From the photoelectric detector to the post amplifier, all modules compose the digital closed loop control circuit, and they are integrated into a single PCB as a control circuit board of FOG. In the following sections, we will discuss the implementation of the control circuit board.

3.2. Preamplifier and A/D Module

Since the optical signal is complicated relatively, after photoelectric converted, the electric signal come out from the detector has plentiful noises. As a signal picking up amplifier, the preamplifier needs to suppress the noises as clean as possible but must ensure its effective bandwidth. Therefore, we choose a operational amplifier with high rate, low excursion and low noise as the preamplifier. And we also design a cascaded directly coupled amplifier as shown in Figure 5 to magnify the signal. Its gain should be adjusted according to the sensitivity of FOG and the precision of the closed loop control.

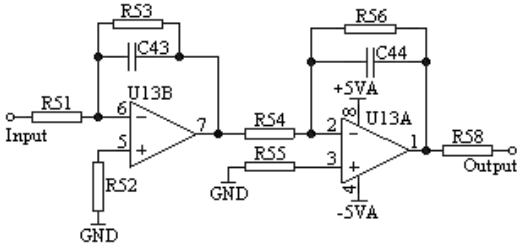

Figure 5. Circuit of Preamplifier

After amplified, the signal should be converted from analog field into digital field to be processed conveniently. Due to existing of the white noise in the circuit, the A/D convertor should meet some requirements. If the LSB of A/D convertor is smaller than the standard deviation of the noise, then the sampling against the signal will be satisfied. According to the analysis, the ratio of the standard deviation of the noise over π/2 offset power is 2.83×10^{-3}. For this order of magnitude, it is enough to satisfy the requirements of circuit in the whole dynamic range when we just use a 12bit A/D to convert an analog signal to a digital signal. The digital integrator may bring the noise suppression like a low pass analog filter, but there is no long-term drift existing in the electronic circuit generally [9].

Additionally, we should consider the eigenfrequency of system when doing A/D conversion. In our scheme, it is about 158kHz. In order to reduce the influence from noise to signal, the performance of A/D chip should ensure sampling 32 points at least in a semi-cycle (316kHz). At the same time, it should keep away from the peak of comb wave in favor of mean treatment. Therefore, the operating frequency of A/D sampling chip is at least 15MHz.

3.3. FPGA Logic Module

The main functions of FPGA include the integral filtering to the sampling signal, the digital generation of closed loop control, the digital generation of second closed loop control, the digital composition of square wave and ladder wave, the output of closed loop control and the output of angular rate.

Its complete parallel processing enables FPGA to control the event of every time edge and process the relative data on micro point as well as hold the direction of data stream and process the data on macro point. The system connection diagram of FPGA [13] is shown as in Figure 6. The digital logic in FPGA can be completed by software. Its detail will be described in the section 3.5.

3.4. D/A Module, Second Closed Loop and Post Amplifier

The final part of the digital closed loop control system is the module for phase excursion control from the control voltage output to Y-waveguide. As a vital part of closed loop circuit, it should guarantee the integrality of signal strictly and satisfy the necessary regional linearity.

The modulation gain drift, caused by the influence of Y-waveguide and post amplifier in temperature change, will depress the scale factor and zero-offset stability of FOG. Thus, in order to get a high capability FOG, the second closed loop control circuit should be introduced into the digital closed loop control system of FOG to track and compensate the 2π reset voltage undulate of the ladder wave caused by the modulation gain drift.

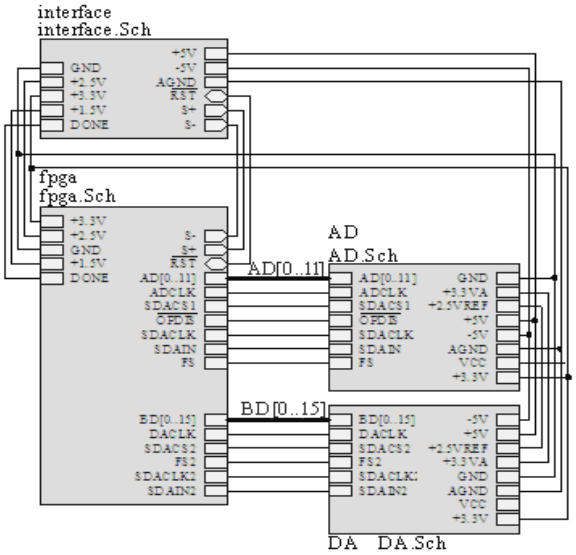

Figure 6. Connection Diagram of FPGA

The most direct approach to complete the second closed loop control circuit is detecting the error of interference signal around the $\pi/2$ reset of the ladder wave, and accumulating its value, then making this accumulated value as the feedback signal of the second closed loop. This feedback signal will be converted by the assistant D/A convertor into an analog signal to control the reference voltage of the main D/A convertor in the main feedback loop. The fundamental principle of the reset error control can be described by the Figure 7.

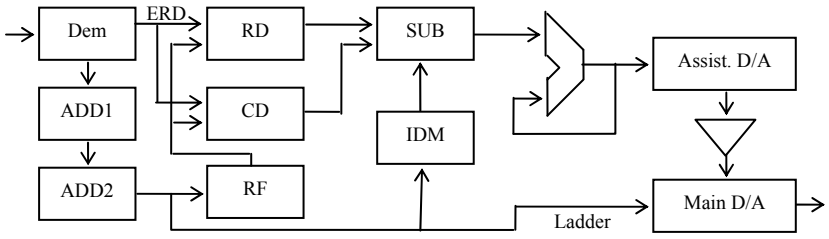

Figure 7. Second Closed Loop and Fundamental Principle of Ladder Reset Control

In Figure 7, ERD is the difference signal of the interference signals when the square wave changes from the positive semi-cycle to the negative semi-cycle. RD is the difference signal of the ladder wave being in reset cycle. CD is the difference signal of the ladder wave being in normal cycle. RF is the marking signal of reset cycle to judge if the signal is in the reset cycle. IDM is a module to detect the ladder wave increasing or decreasing. All these functions can be achieved in FPGA.

On the basis of full considering cost, energy consumption and performance, we select a 16 bit D/A convertor as the main D/A module and a 14 bit one as the assistant D/A module in practice. The main D/A is controlled using parallel interface, while the assistant D/A can only communicate with FPGA using SPI protocol because of the finite pins of FPGA. The two D/A modules are required of having higher establishing times, which are far shorter than the transition time of a light going through the fiber rings.

The basic connection idea is: the FPGA connects with and controls the main D/A and the assistant D/A, then take the output of the assistant D/A as a reference value and input it to the main D/A, form the second closed loop circuit to control its gain. Finally, the output signal of

the main D/A is magnified by two cascade operational amplifiers, and the result will be input into Y-waveguide with the difference method. The circuit of post amplifier is shown as in Figure 8.

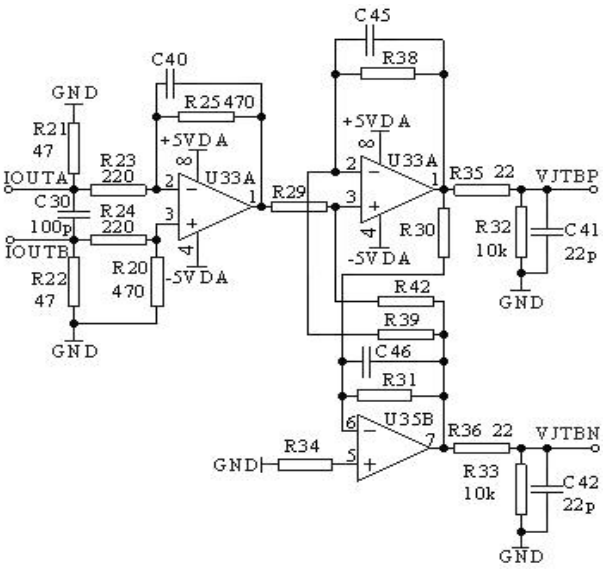

Figure 8. Circuit of Post Amplifier

4. Considerations for Circuit Design

4.1. Component Selection

When applied to the practice, the system may meet quite atrocious circumstance condition and should work reliably even when the temperature is from −40℃ to 60℃. Besides having compensation by software, the system needs very good components to support it. A nice performance represented in the closed loop control board is the stabilization of hardware parameters in whole temperature range.

In our project, the temperature drift coefficients of all chips used in the system should be less than 10ppm, and the voltage reference should be less than 3ppm. The precisions of resistors used near the operational amplifier and determining the gain of the amplifier should be 0.1% and their temperature drift coefficients should be less than 25ppm.

The demands for the capacitors in the system are also rigorous. The functions of capacitors in the circuit can be classified into two types: the bypass capacitor for filtering and the blocking capacitor for separating the direct current. In order to ensure the stability of working signal, the power supply circuit should use the army grade tantalum capacitors with low ESR and ESL. The other stacked capacitors should select the high precision capacitors made by the material C0G or X7R.

4.2. Anti-jamming Design for PCB

An excellent PCB design is the crucial factor for the system working normally.

(1) Basic principles for the PCB design

The basic principles for the PCB design are as follows:

(a) Using multilayer board

The high frequency circuits usually have a high degree of integration and high density of layout. Using multilayer board is obligatory for the layout as well as an efficient measure for reducing the mutual interferences. In PCB design, choosing the number of layers reasonably for the power supply layer can decrease the size of PCB greatly. At the same time, the interim layer can be well used to set shield and it can make an advantageous condition for handy grounding. This measure can reduce the parasitic inductance effectively and shorten the transmission lengths for signals availably as well as depress the cross interference between signals greatly. Such performances improved will advantage the credible working of high frequency circuit. Some one proved that 4-layered board can reduce 20dB more noise than 2-layered board when

using the same material. But more layers the board applied, more complicated manufacturing process adopted and higher cost will be.

(b) Abstaining bended lead wires

The lead wires between the legs of components in a high frequency circuit should be straight but not bended. When the bended lead wires are ineluctable, we should use 45°fold line or arc transition to reduce the emission of the high frequency signal and the coupling between the wires.

(c) Lessening via holes

The alternation of lead wires between the legs of components distributed in different layers in a high frequency circuit should be lessened. That is to say that via holes for connecting the components should be lessened. According to the test, a via hole can bring a 0.5pF distributed capacitance. Reducing via holes will enhance the rate of circuit remarkably.

(d) Lessening via holes

The cross interference inducted by close parallel lead wires should be paid attention when arranging the wires in a high frequency circuit. If the parallel arrangement is unavoidable, laying a large area of ground on the back of the parallel lead wires should be considered to depress the cross interference greatly.

(e) Ground surrounded processing

The ground surrounded measure should be used for the special signal wires or some local units such as the clock unit. It is also of benefit to the high rate system.

(f) No loop ground, no current loop

The lead wires can not form a loop ground or a current loop. A high frequency decoupling capacitor should be set near every integrated circuit.

(g) No loop ground, no current loop

The analog ground and digital ground connected to the common one need the high frequency choke links. When assembling the high frequency choke links, the high frequency ferrite beads with a lead passing through its central hole should be used.

(2) General layout criterion of PCB board

On the basis of principles mentioned above, we determined the current general layout criterion for PCB board design.

(a) Overall design

According to the requirements of structure of FOG in our project, PCB board is an anomalous roundness. Its diameter is 75mm. We design it using 6 layer PCB board. From the top to the bottom, they are upper signal layer, round layer, digital power supply layer, analog power supply layer, another ground layer and lower signal layer.

(b) Power supply design

According to the requirements of system, the power supply interfaces of control board are split into two groups, i.e., A group (+5V, -5V and GND) and B group (+5V and GND), as shown in Figure 9. They supply the powers for the main components and the output optocoupler on the control board respectively. In our project, we use decoupling design for every power entrance to the board and connect with 47□F and 10□F tantalum capacitors in turn to guarantee the calm of input power signal. And then, the signal of A group is split into tree routes. One of them connects to the input part of A/D through the high frequency ferrite bead. Another one is for D/A. The third one links to the digital part of FPGA through the power supply chip. Before connected to their aim regions, three power supply units should be separated by the high frequency choke links and be filtered by a series filter networks, which are composed of the tantalum capacitors with capacitances of 22□F and 10□F. Finally, a group of parallel capacitors of 0.1□F and 0.01□F should be connected to the nearest point from the power supplied chip. In order to ensure the calm of power supply, it should be transmitted in the form of surface through special layer to decrease the transfer impedance.

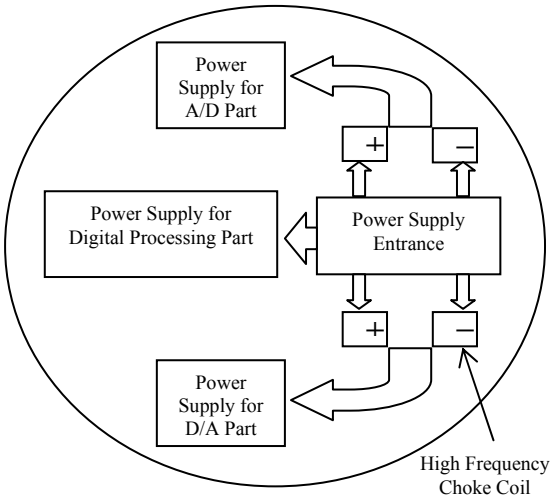

Figure 9. Layout of Power Supply for PCB

(c) Grounding design

All earth wires have their impedances. The current must flow back to its source point like all circuits. The current passing the efficient impedance produced by the earth wire will make a potential drop, which will generate a ground loop current to form the ground loop interference. When two or more than two circuits use the same section of earth wire, a common impedance coupling will be produced. So, using the advantage of 6 layer board, our system builds two groups of large area ground to solve the problems of shield and decreasing the available impedance. This method can make the grounding current flowing back rapidly and enable the functional components to connect the earth in a shortest distance as soon as possible. The scheme of grounding design is shown as in Figure 10.

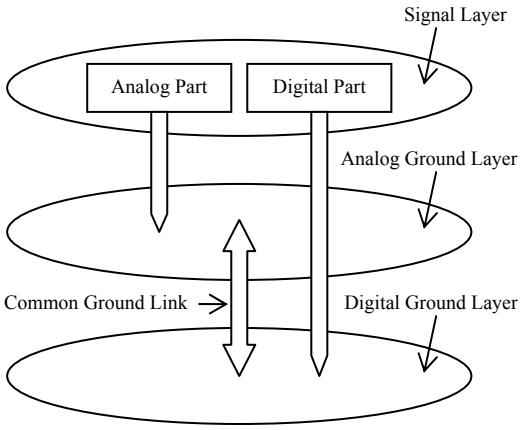

Figure 10. Layout of Ground for PCB

(d) Signal route design

According to the design principle, the lead wire of signal, which is susceptible to interference, should be short and thick. For example, the input signal wire of A/D convertor, the output signal wire of D/A convertor, the signal wire of reference source and so on, are such wires. Therefore, our project thinks over the routing manner of signal wires and selects the method of manual wiring, to insure having shortest distance of signal routing and to try our best to avoid via hole for signal routing. Additionally, using large area spreading coppers on two

signal layers may reduce the impedance of ground wire, provide the shield for numerous signals and lesser current loop. It also achieved a good effect.

5. Experiment Results

We have developed some samples of FOG using the design method described in above sections and programming in FPGA with relevant algorithms. We also tested them simply using the main performance items of scale factor and zero-offset through the experiments, although some better methods [14-15] for testing more details of FOG can be used when there are enough testing data.

5.1. Scale Factor

The scale factor represents the proportional relation between the change of input rotation rate and the change of output of FOG. According to the measured input data and output data in the whole range of input rotation rates, we can use the least square method to calculate the slope of them. That is the scale factor.

Through the experiment test, we obtained that the scale factor of our samples is about 0.0001154 deg•s/LSB, no matter the rotation direction of FOG.

5.2. Zero-offset

The zero-offset is the output value of FOG when it is at zero input state.

Through the experiment test, we knew that the stabilities of zero-offsets of all samples are less than 0.075deg/h.

The experiments and tests show that the proposed method is efficient and valuable.

4. Conclusion

This paper presented a circuit design method for the digital closed loop control system of FOG based on FPGA and developed some samples. Due to apply the dual closed loop technique, the zero-offset stability of FOG had been improved. After the test to the samples, the result data show that their stabilities of zero-offsets are all less than 0.075deg/h. Therefore, this method proposed in this paper is efficient and valuable. In addition, the agility of signal input and output interface of FPGA is convenient for hardware design. And, the digital signal processing by software in FPGA is also convenient for parameter adjustment in experiment. This technique can greatly shorten development period, improve the reliability of system and realize miniaturization of FOG.

The proposed method can be used in the fields of aviation, space, military affairs and so on. But the fluctuated zero-offsets of FOG during warm up and at extreme temperatures limit its application areas. That is our research work to improve them in the future.

Acknowledgements

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