TELKOMNIKA Indonesian Journal of Electrical Engineering
Vol.12, No.7, July 2014, pp. 5163 ~ 5173
DOI: 10.11591/telkomnika.v12i7.6013

Design and Simulation Low Voltage Single-Phase Transformerless Photovoltaic Inverter

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Abstract

The last Deckard years developing Inverter technology for renewable energy and high efficiency and more improvement solar and wind power plant. Transformer less inverter technology is best and improves efficiency, power quality and reduces switching loss. Single-phase grid connected transformerless photovoltaic (PV) inverter for residential application is presented. The inverter is derived from a boost cascaded with buck converter along with a line frequency unfolding circuitIn this research paper transformer less photovoltaic (PV) inverter is going to be more adopted in order to achieve high benefit. The selected inverters are the full-bridge inverter with bipolar modulation, full-bridge inverter with DC bypass and the Highly Efficient and Reliable Inverter Concept (HERIC). A low voltage single-phase grid-connected PV system is analyzed to verify the discussions.

Keywords*: PV inverter, transformerless, HERIC highly efficient and reliable inverter concept, AC-AC Baypass, DC-DC Baypass,*

1. Introduction

The renewable energy sources, in particular those of photovoltaic (PV) origin, have experimented a great development in recent years mainly due to the special feed in tariffs. The full-bridge (FB) inverter topology is widely adopted also for PV grid connected applications, but the need of high efficiency and manufacturing cost reduction has led to new innovative topologies [1].

As pointed out, the main method used to increase the efficiency is to eliminate the transformer. In this case the absence of galvanic isolation leads to leakage current flowing due to the capacitance coupling to earth provided by the PV panels. Hence the transformerless structure requires more complex solutions, typically resulting in newtopolo-gies in order to keep the leakage current and DC current injection under current control in order to comply with safety purposed. The aim of this paper is to analyze and to compare the performances of some new PV transformer less converters [2, 3].

Ideal transformer less inverter generates constant common mode voltage. However, if the voltage varies with time, then a leakage current is produced. For the sake of minimizing this leakage current, different topologies were studied in details. Among these are the full bridge with bipolar PWM, the half bridge, HERIC, H5, H6 and NPC [1, 2]. Sections II is mention block diagram of project scheme and explains this blocks, Section III is mention and explains control of transformer less PV Inverter and methods. Section IV is mention Simulation and Results discussion. In this paper we explain the Many transformerless topologies are derived by adding extra power devices into the Full-Bridge (FB) inverter. For example, the FB inverter with DC bypass (FB-DCBP) adds two power devices at the DC-side [2]; while the Highly Efficient and Reliable Inverter Concept (HERIC) provides an AC bypass leg [3]. Considering the fast growth of grid-connected PV systems, it is better for the next generation transformerless PV inverters to equip with Low Voltage capability in order to fulfill the upcoming requirements efficiently and reliably [4].

Received February 3, 2014; Revised March 23, 2014; Accepted April 4, 2014

2. Single-phase Transformer Less pv Inverter

The topology called "Highly Efficient and Reliable Inverter Concept" (HERIC), commercialized by Sunways, derives directly from the Full-Bridge converter, in which a bypass leg has been added in the AC side by means of two back-to-back IGBTs operating at grid frequency. The HERIC circuit is shown in Figure 1, where Cin is the DC-link capacitor, Lfi and Lfg are the output filter inductors, respectively on the inverter-side and gridside, and Cf is the filter capacitor. The bypass branch has two important functions: decoupling the PV array from The grid (using a method called "AC decoupling"), Avoiding the presence of high-frequency voltage Components across it and preventing the reactive power exchange between the filter inductors and Cin during the zero voltage state, thus increasing efficiency [2]. The converter operates as it follows (see Table 1): during the positive half-cycle S+ remains connected, whereas S1 and S4 commutate at switching frequency in order to generate both active and zero vectors. When an active vector is present (S1 and S4 are ON), current flows from the PV panels to the grid, while, when a zero vector occurs, S1 and S4 are switched OFF and the current flows through S+ and D-, this is the freewheeling situation. On the other hand, when the negative cycle is coming, S+ goes OFF and S- goes ON, whereas S3 and S2 commutate at switching frequency. It means that an active vector is present when S3 and S2 are ON, therefore the current flows from the PV panel towards the load, thus when S3 and S2 turn off, a zero voltage vector is present in the load, then current flows through S- and D+. With regard to the classical Full-Bridge [5-6].

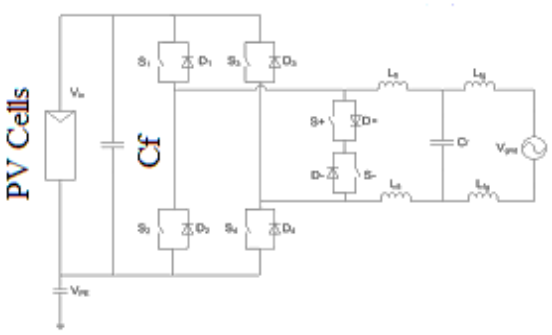

Figure 1. PV HERIC Inverter Topology

The modulation outlined in Table 1 [6] does not provide capability of reactive power processing since the bidirectional switch of this topology made up of S+ and S- is not controlled to be turned ON simultaneously, therefore current can only flow in a predefined direction, defined by the currently turned ON switch. Modifying the switching strategy this inverter can inject reactive power into the grid [7-9]. the PV inverters are responsible for converting DC source generated from PV panels to AC source efficiently and reliably.

Table 1. Conduction States for Inverter

S1	S2	S3	S4	S+	S-	D+	D-	Vout
On	Off	Off	On	Off	Off	Off	Off	Vin
Off	Off	Off	Off	On	Off	Off	On	0
Off	On	On	Off	Off	On	Off	Off	Vin
Off	Off	Off	Off	Off	On	On	Off	0

A widely adopted single-phase PV inverter is the FB topology as shown in Figure 1, where it is connected to the grid through an LCL-filter in order to ensure the injected current quality. There are two main modulation strategies available for this inverter: a) Unipolar

modulation scheme and b) Bipolar modulation scheme. When the transformer is removed from a grid-connected PV system, safety concerns (e.g. leakage current) will arise since the lack of galvanic isolations. Thus, transformerless inverters should eliminate or at least reduce the leakage current, e.g. by including passive damping components and/ or by modifying the modulations [10, 11].

In the light of this, the FB-Bipolar is more feasible insingle-phase transformerless PV applications. However, in every switching period, there are reactive power exchanges between the LCL-filter and the capacitor CPV and also core losses in the output LCL-filter, leading to a low efficiency of up to 96.5% [1], [12-13]. In order to further improve the efficiency and reduce the leakage current, a tremendous number of transformer less topologies have been developed, most of which are based on the FB inverter as it is shown in Figure 2. The first priority of a transformer less inverter is to avoid the generation of a varying instantaneous Common-Mode Voltage inverter [3, 10].

$$V_C = \frac{(V_{ao} + V_{bo})}{2} \tag{1}$$

$$I_C = C_p \frac{dv_{cmv}}{dt} \tag{2}$$

Besides those solutions to limit the leakage current by adding passive damping components and by modifying the modulation techniques, the elimination can also be achieved either by disconnecting the PV panels from the inverter or by providing a bypass leg at the AC side. For instance, the FBDCBP inverter patented by Ingeteam [14] shown in Figure 2 disconnects the PV panels from the inverter using four extra devices (two switching devices SD5, SD6 and two diodes D7,D8); while the HERIC inverter (Figure 2 by Sunways [15] provides an AC bypass using two extra switching devices (SD5, SD6). There have been other transformers less topologies reported in the literature. Some are based on the multi-level topologies [16, 18], and some are derived by optimizing traditional transformer less inverters.

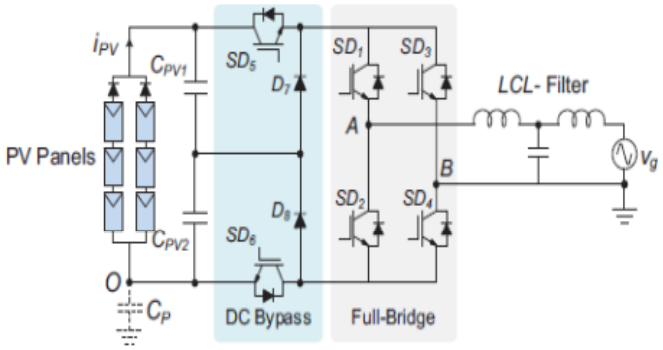

Figure 2. DC Bypass FB Inverter Base L-C-L Filter

DC Bypass: Another 'modified' FB topology is the full-bridge with DC bypass as patented (pending) by Ingeteam [8] and published in reference [9, 11]. This topology is depicted in Figure 2. 11 and is aclassical H-bridge with two extra switches in the DC link and also two extra diodes clamping the output to the grounded middle point of the DC bus. The DC switches provide the separation of the PV panels from the grid during the zero voltage states and the clamping diodes ensure that the zero voltage is grounded, in opposition to HERIC or H5 where the zero voltage is floating. Essentially both solutions ensure 'jump-free' VPE, leading to low leakage current and high efficiency due to prevention of reactive power exchange between L1(2) andCPV1(2) during zero voltage. The switching states for positive and negative generated AC currents are depicted in Figure 3 [13, 14].

It was the first structure able to take advantage of the first available force-commuted semiconductor devices. The H-bridge topology is very versatile, being able to be used for both DC–DC and DC–AC conversion and can also be implemented in FB form (with two switching legs) or in half-bridge form (with one switching leg) [5, 11, 15]. The AC bypass provides the same two vital functions as in the case of HERIC [5, 16]: Prevents the reactive power exchange between Land CPV during the zero voltage state, thus increasing efficiency.Isolates the PV module from the grid during the zero voltage state, thus eliminating the high frequency content of VPE.

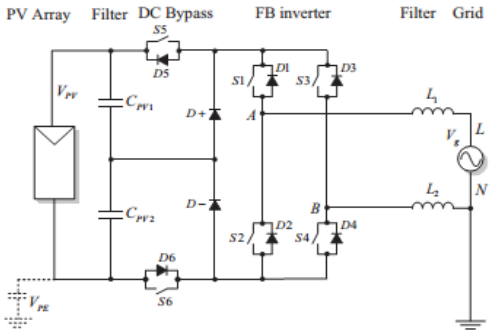

Figure 3. Basic DC Bypass Base FB Inverter

Advantages:

a) Voltage across the filter is unipolar (0→+VPV→0→−VPV→0), yielding lower core losses.
b) The rating of the DC bypass switches is half of the DC voltage.
c) Higher efficiency is due to no reactive power exchange between L1(2) and CPV1(2) during zero voltage and to a lower switching frequency in the FB and low voltage rating ofS5 andS6.
d) VPE has only a grid frequency component and no switching frequency components, yielding a very low leakage current and EMI.

Disadvantages:

a) Two extra switches and two extra diodes.
b) Four switches are conducting during the active vector, leading to higher conduction losses but without affecting the overall high efficiency.

AC Bypass: In 2006, Sunways patented a new topology also derived from the classical H-bridge called HERIC (highly efficient and reliable inverter concept) by adding a bypass leg in the AC side using two back-to-back IGBTs (insulated gate bipolar transistors), as shown in Figure 2 [6, 18]. The AC bypass provides the same two vital functions as the fifth switch in case of the H5 topology: Prevents the reactive power exchange between L1(2), and CPV during the zero voltage state, thus increasing efficiency. Isolates the PV module from the grid during the zero voltage state, thus eliminating the high-frequency content of VPE seen in Figure 4 The main features of this converter are: S1–S4 and S2–S3 are switched at high frequency and S+(S−) at grid frequency. Two zero output voltage states are possible:S+=on andS−=on (providing the bridge is switched off) [19, 20].

Advantages:

a) Voltage across the filter is unipolar (0→+VPV→0→−VPV→0),yieldi-ng lower core losses.
b) Higher efficiency of up to 97 % is due to no reactive power exchange between L1(2)and CPV during zero voltage and to lower frequency switching in one leg.
c) VPE has only a grid frequency component and no switching frequency components, yielding very low leakage current and EMI

Disadvantage:

a) Two extra switches.
b) We required gating circuit.

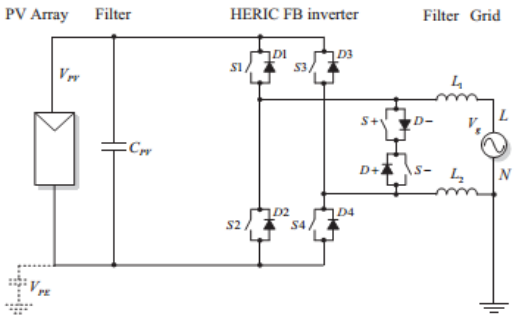

Figure 4. FB Inverter with AC Bypass Topology

LCL Filter: Like in the case of the LCL filter, the increase in the size of the capacitance leads to a reduction in the cost and weight of the filter [17-18], [20].

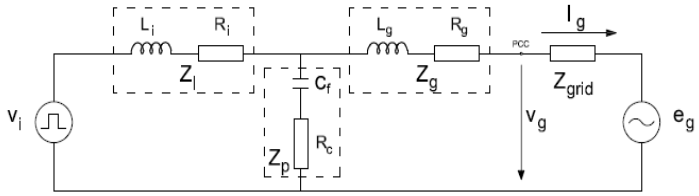

Figure 5. Circuit with LCL Filter

The LCL filter Figure 5 brings the advantage of providing a better decoupling between the filter and grid impedance (as it reduces the dependence of the filter on the grid parameters) and a lower ripple of the current stress across the grid inductor [1, 13, 21]. In order to obtain the transfer function of the LCL filter, the one phase electrical diagram in Figure 6 is considered. The components of the filter on each phase are considered to be identical, so the circuit below is suitable for the other two phases [1].

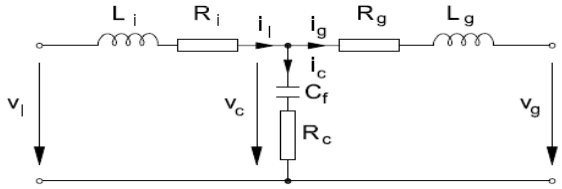

Figure 6. One Phase Electrical Circuit of an LCL Filter

The transfer function of the filter is expressed by Equation (3) to (7)

$$i\,i - i\,c - i\,g = 0 \tag{3}$$

$$v\,i - v\,c = i\,i(sL\,i + R\,i) \tag{4}$$

$$v\,c - v\,g = i\,g(sL\,g + R\,g) \tag{5}$$

$$H_{LCL} = \frac{i_g}{v_i} \tag{6}$$

$$H=\frac{sR_cC_f+1}{s^3L_gL_iC_f+s^2C_f(L_g(R_c+R_i)+L_i(R_c+R_g))+s(L_g+L_i+C_f(R_cR_g+R_cR_i+R_gR_i))+R_g+R_i} \quad (7)$$

2.1. Limits on the Filter Parameters

In the technical literature there are many suggestions that may be considered designing an LCL filter [13], [15-16], but there is no designated step-by-step strategy on this matter. However, in this project the following limitations on the filter parameters have been taken into account [15].

The value of the capacitance is limited by the decrease of the power factor that has to be less than 5% at the rated power. The total value of the filter inductance has to be less than 0.1 p.u. for low power filters. However, for high power levels, the main aim is to avoid the saturation of the inductors. The resonance frequency of the filter should be higher than 10 times the grid frequency and then half of the switching frequency. In respect to the modulation of a transformer less inverter, it should not generate a varying CMV. With a dedicated modulation scheme for those inverters, there is no reactive power exchange between the LCL-filter and the capacitor CPV at zero-voltage states, and thus higher efficiency is achieved. However, extra power losses, including switching losses and conduction losses, will appear on the required additional switching devices in these inverters as shown in Figure 7.

Moreover, the power losses of an individual switching device are dependent on its commutation frequency, which differs with inverter topologies, and its electrical stress. For example, the extra devices, S5 and S6 in the FB-DCBP inverter are commutated at a high switching frequency (e.g., 10kHz); while those in the HERIC inverter commutate at the line fundamental frequency (e.g., 50Hz). Since the total power losses will further introduce redistributions of both current and thermal stresses on the devices among these inverters, the efficiency and the lifetime will be affected [15].

2.2. Calculation of the Filter Values

The system parameters considered for the calculation of the filter components, for a power level of 100kVA, are presented in the table below for this High voltage system [1, 7, 20].

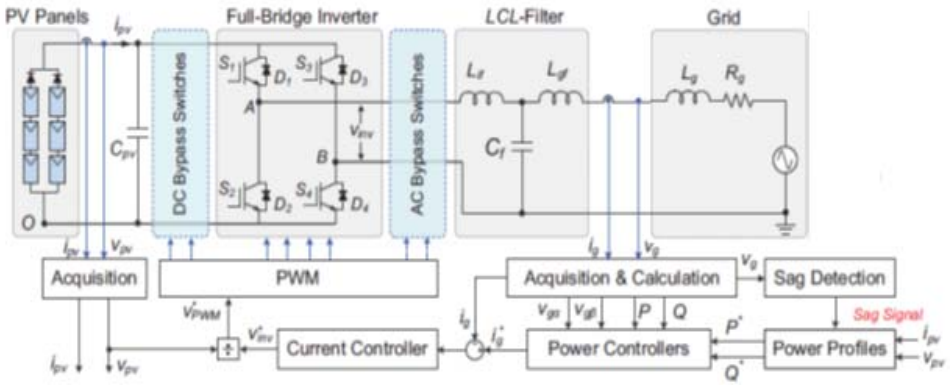

Figure 7. AC, DC Bypass Base LCL Filter with FB Inverter

For the further development, the base values are calculated, as the filter values are reported as a percentage of these.

Table 2. Parameters of the Considered System [1, 21]

Grid Line to Line voltage	En=380V
Output Power of the Inverter/Converter	Sn=100KVA
DC-Link voltage	Vdc=650V
Frequency of grid Voltage	F=50Hz
Switching frequency	Fsw=3KHz- 15kHz

$$Z_b = \frac{(E_n)^2}{S_n} = 1.444\,[\Omega] \tag{8}$$

$$L_b = \frac{Z_b}{\omega_n} = 4.596\ [mH\ ] \tag{9}$$

$$C_b = \frac{1}{\omega_n Z_b} = 2204\ .3621\ [\mu f\ ] \tag{10}$$

The first step is to design the inverter side inductance, which is determined by [15]:

$$\frac{i_i(n_{sw})}{v_i(n_{sw})} \approx \frac{1}{\omega_{sw} L_i} \tag{11}$$

$$\left[\left[\omega_{res} = \sqrt{\frac{L_i + L_g}{L_i.L_g.C_f}} = 14.97 * 10^3 \Rightarrow f_{res} = 1.337[kHz]\right]\right] \tag{12}$$

Where ω_{res}, sw is the switching frequency and nsw is the frequency multiple of the fundamental frequency at the switching frequency are mention above Equation (8) to (12).

2.3. Control Scheme of PV Transformer Inverter

In this Section, the control of the inverter is designed. In the first part, the PLL is described. Then the current loop is designed, for the case of PI control and the case of P+Resonant control. The last part deals with the design of the dc voltage loop. The block diagram of the inverter control considered in this project is presented in Figure 9.

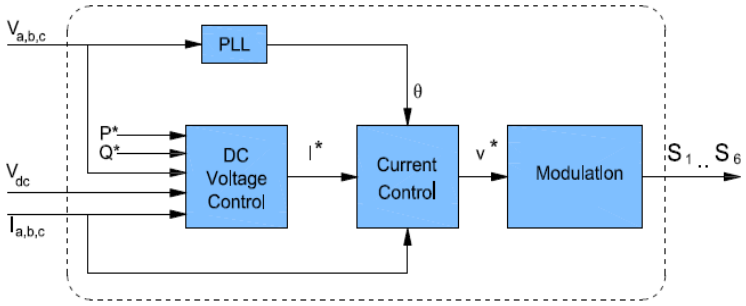

Figure 9. Block Diagram of Control Scheme

The current is oriented along the active voltage component (Vd), this is why this strategy is called voltage oriented control. A PLL algorithm detects the phase angle of the grid, the grid frequency and the grid voltage. The frequency and the voltage are needed for monitoring the grid conditions and for complying with the control requirements. The phase angle of the grid is required for reference frame transformations. If a PI current control is implemented, then the currents are transformed into the synchronous reference frame, and the algorithm implements also the decoupling between the two axes. If a P+Resonant controller is used, then the currents are transformed into the stationary reference frame and decoupling is not implemented. For the dc voltage control, a standard PI controller is used also for the DC voltage and it outputs the reference for the current control [17]. Two types of current controllers are implemented: a PI control in the synchronous reference frame and a P+Resonant (PR) control in the stationary reference frame. The PI current control block diagram is given in Figure.10 and the PR current control with harmonic compensation block diagram in shown in Figure 11 [13].

PI Controller:

The block diagram of the PI regulator is depicted in Figure 10 and the transfer function is the one in (13), [1, 5, 22].

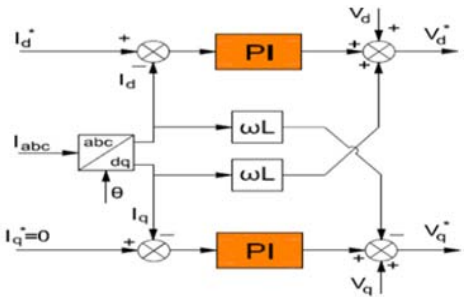

Figure 10. Block Diagram of PI Regulator

$$G_{PI}(s) = K_p + \frac{K_i}{s} \tag{13}$$

The d and q control loops have the same dynamics, so the tuning of the PI parameters for the current control is done only for the d axis.For the q axis the parameters are assumed to be the same. As it can be seen from the current control block diagram in Figure 10, the voltage feed forward and the decoupling between the d and q axes has been neglected as they are considered as disturbances. The block diagram of the PR regulator with Harmonic Compensation is depicted in Figure 11, [1, 5, 23].

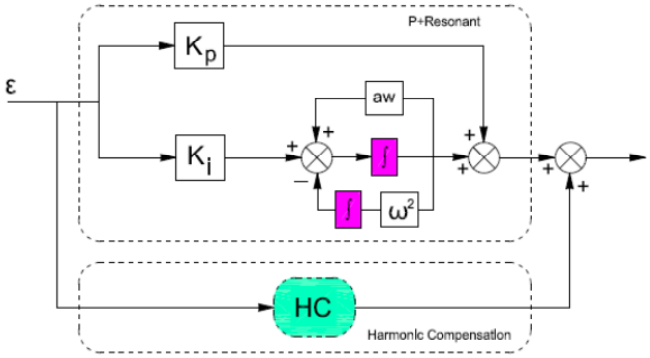

Figure 11. Block Diagram of PR Regulator

The transfer function of the PR controller is:

$$G_{PI}(s) = K_p + K_i \frac{s}{S^2 + \omega^2} \tag{14}$$

Where aw is the anti-windup function implemented as:

$$a\omega = \begin{cases} y_{\max} - y, y \rhd y_{\max} \\ y - y_{\max}, y \lhd -y_{\max} \end{cases} \tag{15}$$

The transfer function of the Harmonic Compensator is [21].

$$G_{HC}(s) = \sum K_{Ih} \frac{s}{s^2 + (\omega.h)^2}, h = 3,5,7 \quad (16)$$

The most important harmonics in the current spectrum are the 3rd, the 5th and the 7th. So the harmonic compensator is designed to compensate these three selected harmonics. In order to perform the discrete analysis on the PR current control, the initial values calculated with the optimal modulus method for the PI control are used for the PR control to begin with. Using the root locus method, the proportional gain K_p is selected so that the dominant poles have a damping factor of 0.7. As it can be seen in the Figure 12. with a Kp value of 0.78, the damping of the resonant poles reaches the value of 0.7. An integral gain Ki of 300 has been chosen as a tradeoff between a good noise rejection and good dynamics [21].

3. Results and Analysis

The research paper presents the closed loop control system for a single-phase transformer-less PV system. It is observed in Figure 7 that an effective power calculation method in terms of fast dynamic response and accurate computation, together with an advanced synchronization unit, can contribute to the Low Voltage PV Inveter performance of the entire system. In this paper, the Second Order Generalized Integrator based Phase Locked Loop has been selected as the synchronization unit because of its robustness [9], [24-25].

The average power calculations are based on the Discrete Fourier Transformation (DFT). Since the DFT uses a running window to do the calculation, it naturally will introduce a delay [22-23]. Now we design project scheme in MATLAB Simulation see Figure 12. FB inverter with DC Byppas and AC Bypass connected in grid system with 50hz frequency and single phase AC voltage out put Voltage and current wave form mention Figure 13. In this project we design controller and PI+ PR controller are design in PLL control scheme are mention out put gating signal in Figure 14 SPWM Signal for FB Inverter and AC, DC Bypass, in Figure 15 is mention FB Inverter Output Voltage. Using AC bypass and LCL filter topology we controlled output current waveform and removed un necessary harmonic waveform is sawn in Figure 16 L-C-L Filter Output Voltage and current Waveform.

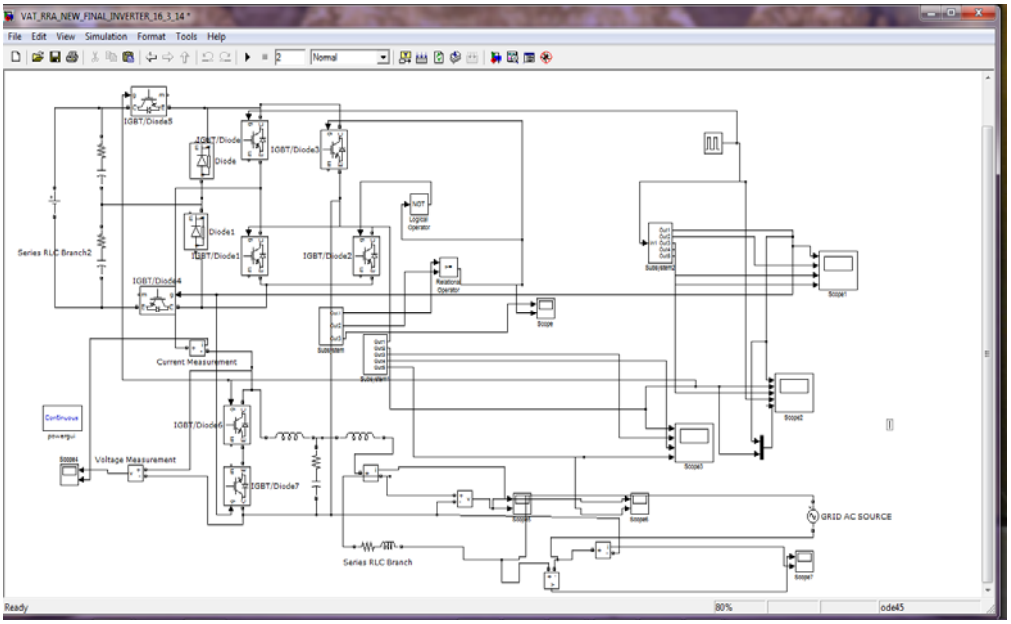

Figure 12. MATLAB Simulation Project Diagram

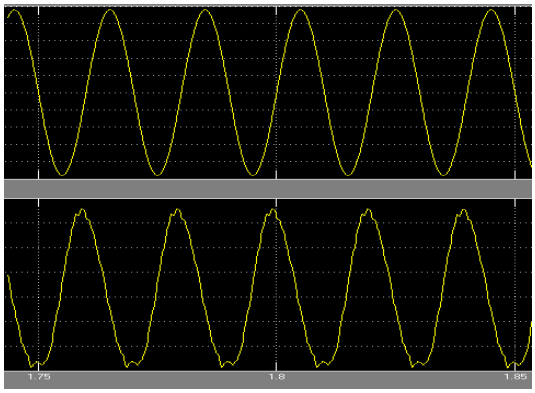

Figure 13. FB Inverter with DC Bypass and AC Bypass Connected Grid System Output Voltage and Current Wave Form

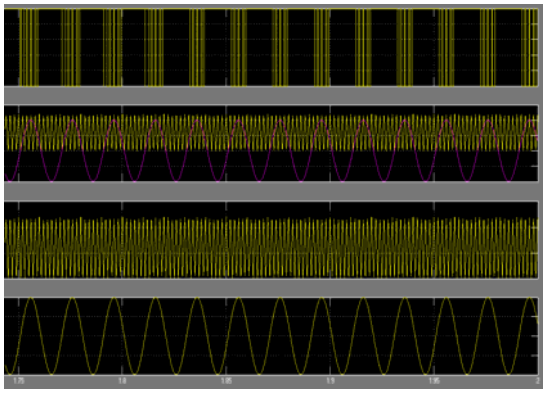

Figure 14. SPWM Signal for FB Inverter and AC, DC Bypass

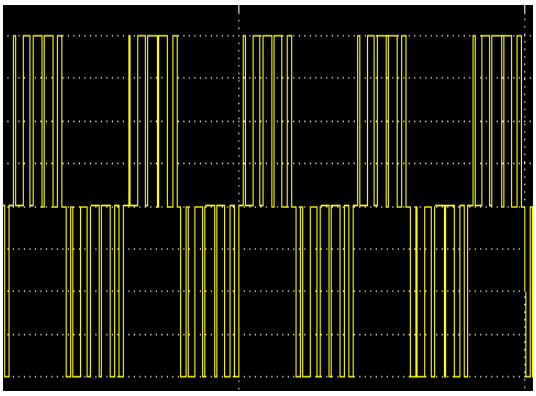

Figure 15. FB Inverter Output Voltage

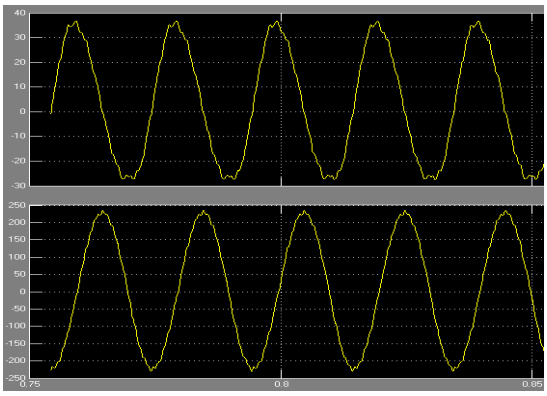

Figure 16. L-C-L Filter Output Voltage and Current Waveform

4. Conclusion

The results show that the HERIC inverter can achieve a high efficiency, but it cannot be used in the next generation PV systems with Low Voltage capability or reactive power injection. For this inverter, a possible way to ride-through voltage fault is to modify the modulation scheme during Low Voltage FB Inverter but at the cost of reducing efficiency. The performance of a Full-Bridge inverter with DC bypass topology (FB-DCBP) is satisfactory under Low Voltage FB Inverter operation. It can achieve a slightly higher efficiency compared to full-bridge inverter with bipolar modulation. However, in Low Voltage operation, a varying common mode voltage appears in the FB-DCBP inverter, the test results have verified the effectiveness of the PQ control method and the constant peak current strategy for reactive power injection. Moreover, due to the high switching frequency for the extra devices of the FB-DCBP, high current stresses might appear and further introduce failures to the whole system. Never the less, for different applications.

References

[1] Rajendra Aparnathi, Ved Vyas Dwivedi, L-C-L Filter for 3-Ø Inverter - Lambert Academic Pub. Germany, ISBN-978-3-659-26001-8. 2012

[2] Meinhardt M, Cramer G, Burger B, Zacharias P. Multi-String-Converter with Reduced Specific Costs and Enhanced Functionality. *Solar Energy*. 2001; 69(Suppl. 6): 217–227.

[3] Lopez O, Teodorescu R, Freijedo F, DovalGandoy J. *Leakage Current Evaluation of a Single-Phase Transformerless PV Inverter Connected to the Grid*. InApplied Power Electronics Conference, APEC Twenty Second Annual IEEE. 2007: 907–912.

[4] Mcmurray W. Inverter Circuits. US Patent 3207974. 1965.
[5] Lai RS, Ngo KDT. A PWM Method for Reduction of Switching Loss in a Full-Bridge Inverter. *IEEE Transactions on Power Electronics*. 1995; 10(3): 326–332
[6] Victor M, et al. US Patent Application, Publication Number US 2005/0286281 A1. 2005.
[7] Schmid H, et al.US Patent 7046534. 2006.
[8] Hantschel J. German Patent Application, Publication Number DE102006010694 A11. 2007.
[9] Gonzalez S, R.et al. International Patent Application, Publication Number WO2008015298. 2007.
[10] Gonzalez R, Lopez Sachis p, Marroyo L. Transformerless Inverter for Single-Phase Photovoltaic System. *IEE Transactions and Power Electronics.* 2007; 22(2): 693-697.
[11] Kerekes T, Teodorescu R, Rodriguez P, Vazquez G, Aldabas E. A New High-Efficiency Single-Phase Transformerless PV Inverter Topology. *IEEE Transactions on Industrial Electronics.* 2010.
[12] Nabae A, Magi H, Takahashi I. A New Neutral-Point-Clamped PWM Inverter. *IEEE Transactions on Industry Applications.* IA-17(5). 1981; 518–523.
[13] Knaup P. International Patent Application. Publication Number WO 2007/048420 A1. 2007.
[14] Calais M, Agelidis VG, Meinhardt M. Multilevel Converters for Single-Phase Grid Connected Photovoltaic Systems: An Overview. *Solar Energy*. 1999; 66(5): 325–335.
[15] Mohan N, Undeland T, Robbins PW. Power Electronics. Converters, Applications and Design, John Wiley & Sons, Ltd, Chichester. 2003. ISBN 0471226939.
[16] Kerekes T, Teodorescu R, Klumpner C, Sumner M, Floricau D, Rodriguez P. *Evaluation of ThreePhase Transformerless Photovoltaic Inverter Topologies*. Power Electronics and Applications. European Conference. 2007; 1–10.
[17] Burger B, Schmidt H*. 25 Years Transformerless Inverters.* Proceedings of PVSEC, 2007.
[18] REN21. Renewables 2013: Global Status Report (GSR). Available: http://www.ren21.net/, Jun. 2013.
[19] KO Kovanen. Photovoltaics and power distribution. *Renewable Energy Focus.* 2013; 14(3): 20-21.
[20] Y Xue, KC Divya, G Griepentrog, M Liviu, S Suresh, M Manjrekar. *Towards next generation photovoltaic inverters.* Proc. of ECCE'11. 2011; 2467-2474.
[21] SM Chen, TJ Liang, KR Hu. Design, analysis, and implementation of solar power optimizer for DC distribution system. IEEE Trans. *Power Electron.,* 2013; 28(4): 1764-1772.
[22] PS Shenoy, KA Kim, BB Johnson, PT Krein. Differential power processing for increased energy production and reliability of photovoltaic systems. *IEEE Trans. Power Electron*., 2013; 28(6): 2968-2979.
[23] E Koutroulis, F Blaabjerg. Design optimization of transformerless grid-connected PV inverters including reliability. *IEEE Trans.Power Electron.,* 2013; 28(1): 325-335.
[24] Rajendra Aparnathi, Ved Vyas Dwivedi. Power Filter Design to improve Power System Engineering. ISBN978-3-659-27435-0 -Lambert Academic Pub. Germany. 2012.
[25] Rajendra Aparnathi, Ved Vyas Dwivedi. Electrical Machine and Drive (Introduce Advance Control). Lulu Engineering academic Publication-USA. ISBN: 978-1-304-50491-3. 2013.