Indonesian Journal of Electrical Engineering and Computer Science
Vol. 34, No. 2, May 2024, pp. 756~767
ISSN: 2502-4752, DOI: 10.11591/ijeecs.v34.i2.pp756-767

Multilevel inverter: harmonic analysis with and without filters for RL load using SPWM techniques

Champa Patanegere Nagarajappa[1], Abhay Anandarao Deshpande[2]
[1]Department of Electrical and Electronics Engineering, Faculty of Electrical and Electronics Engineering Bhageerathi Bai Narayana Rao Maanay Institute of Technology, Bangalore, India
[2]Department of Electronics and Communication Engineering, Faculty of Electronics and Communication Engineering, Rashtreeya Vidyalaya College of Engineering, Bangalore, India

Article Info

Article history:

Received Dec 16, 2023
Revised Feb 6, 2024
Accepted Feb 9, 2024

Keywords:

Cascaded H-bridge
Filter
Lower order harmonics
PsD
Pulse width modulation

ABSTRACT

Multilevel inverter (MLI) gains more attraction compared to conventional inverter as it generates a staircase output voltage that mimics sine waves of desired output voltage. Cascaded H-bridge (CHB) topology is taken into consideration owing to several benefits over conventional inverters. Various levels of CHB (3 and 5 level) inverters are compared on diverse parameters. In this paper level shift sinusoidal pulse width modulation technique is considered resulting in reduced lower order harmonic (LOH) distortion and improve the quality of output current and voltage depending on the load. Since, the LOH are too dangerous for power electronic circuits. An attempt to shift all the LOH above 50th order depending on the modulation technique with analogy for selecting an appropriate switching frequency is highlighted. The effect of change in switching frequency and modulation index (MI) on RMS output voltage, % voltage total harmonic distortion (VTHD), output power factor with different modulation techniques such as phase disposition pulse width modulation (PsD PWM), phase opposite disposition (POD PWM), alternative phase opposition disposition (APOD PWM) is portrayed in the paper. Further, to boost the performance a unique filter circuits with optimal design values of Inductance and capacitance driven with IEEE 519-2022 standards. The effectiveness in terms of with and without filter is verified and validated using MATLAB.

Corresponding Author:

Champa Patanegere Nagarajappa
Department of Electrical and Electronics Engineering, Faculty of Electrical and Electronics Engineering
Bhageerathi Bai Narayana Rao Maanay Institute of Technology
Bangalore, India
Email: champapn@bnmit.in, champa.pn@gmail.com

1. INTRODUCTION

With the present emphasis on environmentally friendly and sustainable power generation renewable sources are becoming increasingly significant. Photovoltaic (PV) generation is the key player in this revolution that is currently in progress. However, solar energy needs other parts in addition to the actual solar cells. In a power system where, alternating current supports the distribution and transmission system, direct current (DC) generating PV systems need inverters to connect their output to the grid; therefore, enhancing the quality of inverters circuits is crucial to surge its efficiency [1]. However, various components involved in designing the inverter such as switching devices to withstand the necessary output voltage involve added hassles and complexity in itself. This also leads to the question of inverter efficiency and its cost. To overcome the challenges faced by conventional two-level inverters such as increase in % total harmonic

distortion (THD) at the output, dv/dt stress on the semiconductor devices, losses at high switching frequencies and to improve the quality of the output power optimization becomes a pivotal point. The ongoing study seeks the attention towards the multilevel inverter (MLI) with modern architecture as a solution. Focus of the optimization proposed in this paper is two folds: improving the quality of output power by shifting the lower order harmonics (3^{rd},5^{th},7^{th}…) and further improvement with suitable filter circuits. These multilevel inverters are classified as diode/neutral point clamped MLI, flying capacitor MLI, cascaded H-bridge MLI [1]. Among these cascaded H-bridge MLI is considered due to the H-bridge topology with reduced components (such as diodes, capacitor, and Dc link), circuit complexity and equal load sharing among all the switches. A dual cascaded H-bridge MLI with voltage boosting capacity is chosen over the other two topologies shown in Figure 1 with symmetrical DC sources. Due to its modularity the faulty section can be easily identified, replaced, and also easily manufactured. MLI has staircase waveform with improved power quality over the two-level inverter topology, reduced problems of electromagnetic compatibility (EMC) [1], low THD that are suitable for motor drive, solar panel, fuel cells or battery. The level shift PWM technique (phase disposition (PsD), phase opposite disposition (POD), alternative phase opposition disposition (APOD)) is considered for analysis with an optimized switching frequency. A comprehensive analysis for selecting an optimized switching frequency is discussed by shifting all the triplen lower order harmonics to higher order under section 3.

Designing an appropriate filter circuit is also discussed by considering L, LC, and LC with damping resistance for the proposed dual H-bridge inverter. Korde *et al.* [2] suggested that LCL filters are preferable for multilevel inverters with increasing levels. Reliability predictions for full-bridge inverters with various coupling filters are presented by comparing L filters with combination stages and LCL filters [3]. A comparative discussion of the conventional passive filter with proposed filter is presented and evaluated using experiments performed on a 110 V, 1 kW inverter with five-level grid connection [4]. A new filter structure with improved power quality and low snubber power loss is proposed [5] for a five-level CHB inverter used in grid-connected applications.

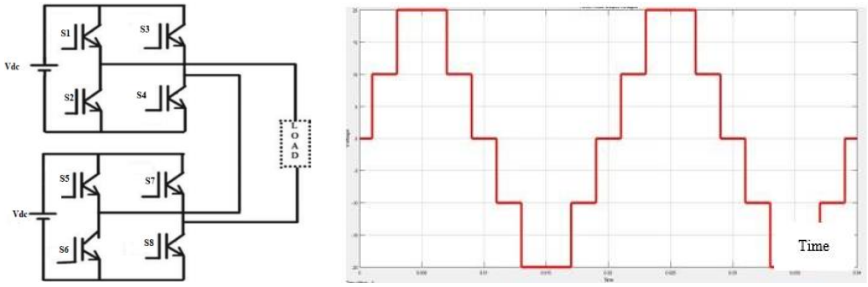


Figure 1. Circuit model of five level multilevel inverter with voltage levels

Shanono *et al.* [6] four passive filters i.e., LC, LCL, and LCL with series and parallel resistance is compared for nine level inverters to obtain THD less than 5%. This problem of poor stability margin was addressed by connecting an appropriate resistance value in either series or parallel to the filter capacitance [7] the size of the filter is reduced by decreasing dv/dt stress. Therefore, the discussion suggested that there is an ample of scope for researchers in the field of cascaded H-bridge MLI. Optimization becomes a critical element thus, the scope of the paper includes three level single and five level cascaded dual H-bridge inverters are considered for evaluating the performance with change in modulation index on its diverse parameters such as power factor, RMS output/load voltage and current, effect of increase in the number of levels with decrease in %THD is discussed. Furthermore, to mend its performance optimal designing of the filter circuits for cascaded dual H-bridge is considered. This paper is divided into following sections control technique, proposed topologies with and without filter design is described in section 2; results and discussions with change in MI and change in switching frequencies, analysis of CHB MLI with and without filter are described in section 3; finally concluded in section 4.

2. METHOD

2.1. Control techniques of multilevel inverter

To tailor the Industrial requirements there are various methods of control schemes available centered on the design of the inverter for improving the quality of the output obtained can be enumerated as peripheral control schemes and internal control schemes [8]. In the external control, additional auxiliary

elements are required but, in the internal control without making the circuit bulky, a medium or high-frequency PWM mechanism can be incorporated which is discussed in detail in this section. The carrier/triangular wave is at a high frequency compared to the reference signal at 50 Hz. Multi-carrier denotes the control strategy of PWM that consists of more than one carrier. If the carrier is one, then it is said to be a single carrier-based SPWM [9] which is normally used for generating two levels of voltages.

Nowadays, PWM technique has been in great demand. Since many PWM strategies are not suitable for high-power applications. So, to deal with these problems, multicarrier-based SPWM is usually preferred over other strategies. These are effective in reducing switching losses and harmonic contents. This PWM is also known as the sub-harmonic or sub-oscillation method [9]. The control strategy uses in this paper includes (m-1) carriers for m-levels to produce the desired multilevel AC output voltages. Triangular-shaped carriers are compared with the sinusoidal signal at every instant and when both the signals get intersected pulses are obtained. For any level m, (m-1)/2 carrier signals are applied across the positive and negative half cycle. When the sinusoidal wave is more than the carrier signal then there are positive voltage levels generated and (m-1)/2 carriers are generated above the reference levels [10]. When the carrier signal is more than the sinusoidal signal, negative voltage levels are generated. Pulses are generated for positive half cycles. (m-1)/2 carriers are produced below the reference level which means negative carriers of (m-1)/2 levels are generated below the zero level. Pulses will be generated for the negative cycle. Khalif *et al.* [11], a simple formula to calculate the required inductance of an LC filter with unipolar switching arrangement is discussed.

For different types of multi-carrier PWM methods discussed in Figure 2, the equation of modulation ratio varies. The value of the modulation index lies between 0 and 1. If this value exceeds 1 then there is the occurrence of over-modulation which means the desired output waveform is just like a square wave in the case of the 2-level inverter [12]. The shape of the waveform remains no longer sinusoidal. The reference signal frequency (f_m) indicates the output fundamental frequency that is 50 Hz. The ratio of the carrier frequency (f_c) to the reference wave frequency (f_m) is called frequency ratio.

$$M_f = \frac{f_o}{f_m}$$

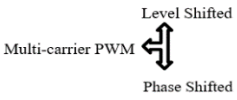


Figure 2. Types of multicarrier PWM techniques

2.1.1. Level-shifted SPWM scheme

This paper discusses on LSCPWM which is used as utmost switching technique for voltage boosting [13]. For k-level MLI, (k-1) carriers are considered that are continuous. These pulses are generated at the same frequency [14] and amplitude as the carrier triangular signal compared with the reference sinusoidal signal generated at fundamental frequency which is simplified PWM technique [15]. Level-shifted MCPWM generates [16] a better quality of output voltage by reducing distortion and power losses compared to Phase-shifted MCPWM by increasing its prominence [17]. Level-shifted MCPWM can be further classified as three types with the same frequency and amplitude of carrier and reference signal. In this PsD technique, a reference signal at 50 Hz is compared with a (K-1) carrier signal for an optimized H-bridge [18] at the same frequency displayed in Figure 3. The switching pattern produced by considering this scheme for a symmetrical topology of H-bridge is graphically represented in Figures 4 and 5 respectively [19], [20].

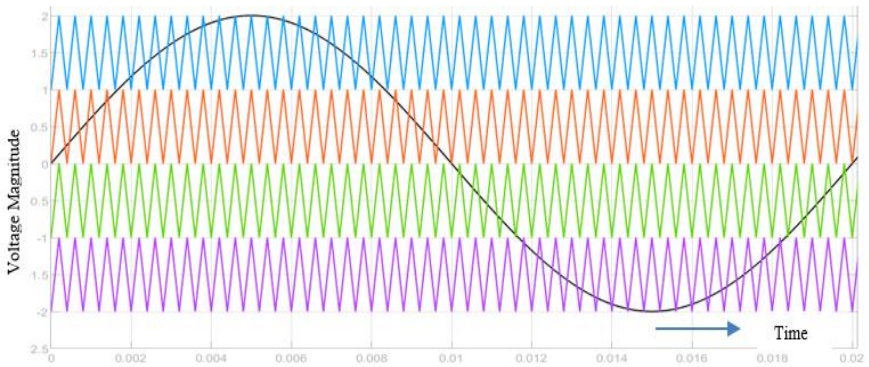


Figure 3. Carrier and modulating signals of PsD PWM technique

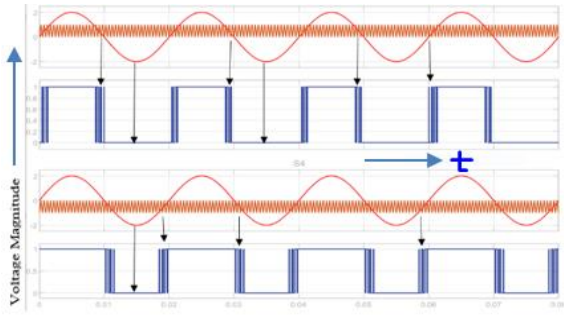


Figure 4. Switching pattern of S1, S4

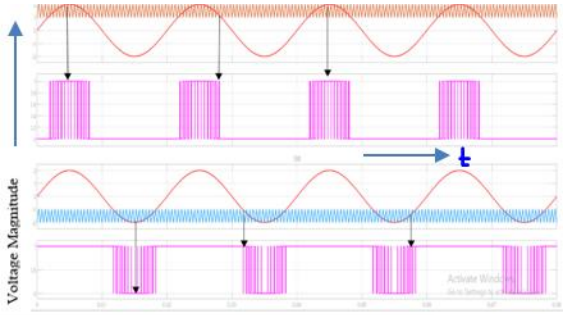


Figure 5. Switching pattern of S5, S8

2.2. MATLAB simulation of five-level inverter with PsD PWM technique

The cascaded 5-level single phase CHB MLI used for this implementation has two dc sources and eight switches in Figure 6. The main advantage of this type of arrangement is its simplicity and improvement of the output voltage resolution without any diode and capacitor. Simulink model of suggested modulation techniques for comparison of 3 level with five level CHB MLI is carried out using MATLAB/Simulink and the following parameters were used: Vdc1= Vdc2 =150 V, fc= 2.5 kHz and fm= 50 Hz, Ro=530 Ω, Lo=0.8H, Ma=1.0.

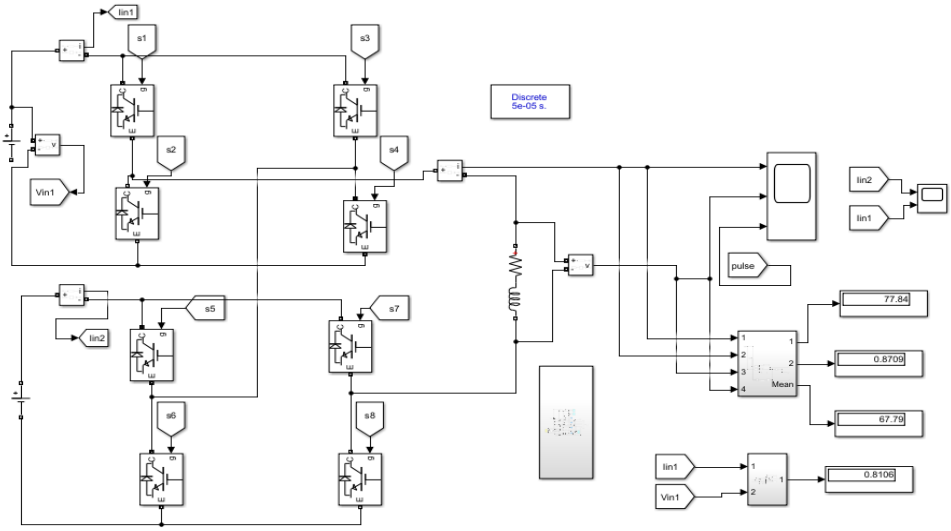


Figure 6. Simulation circuit of five level multilevel inverter

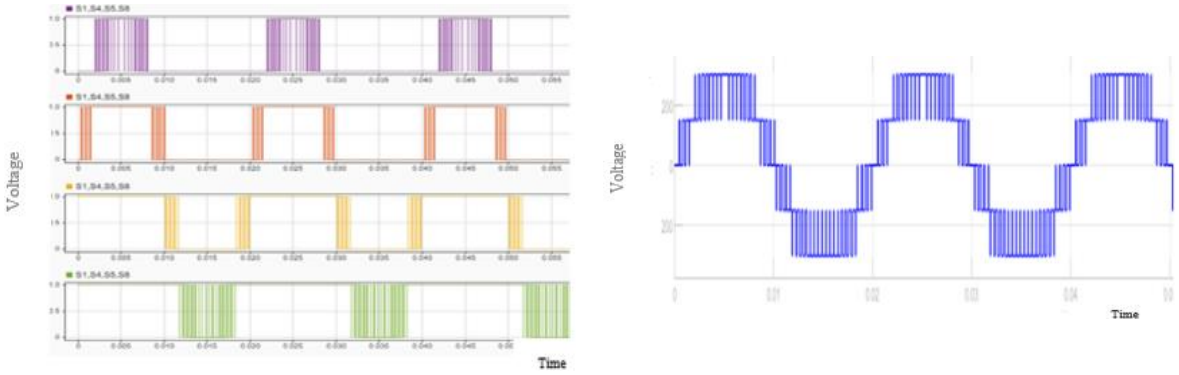
In an individual H-bridge, the output/load voltage is positive voltage (+V*dc*), zero voltage (0V*dc*) and negative voltage (-V*dc*). Hence, the desired voltage levels for five-level CHB MLI are ±2 V, ±1 V, and 0 V represented in Table 1. The output voltage boosting of Five-level MLI is observed in Figure 7 with the PWM pulses and the voltage generated in Figure 7(a) and Figure 7(b) respectively. Similarly, consider the simulation results of 3-level CHB MLI with PsD PWM as shown Figure 8 at same load and switching frequency simulated at V_{dc}=230 V to generate the single-phase AC supply voltage of 230 V, 50 Hz across the RL load. The PWM pulses generated by three-level CHB MLI in depicted in Figure 8(a) and the corresponding output voltage is shown in Figure 8(b). Comparing both 3-level CHB MLI and 5-level CHB MLI for overall %THD generated is 33.92% for 3-level and 5-level inverter is 22.99% represented in Figures 9 and 10. Harmonic up to 100th order is considered for simulation. As the main aim of the research is to shift all the triplen harmonics above 50th order so that a high-quality output voltage is generated in the grid.

From the plots it's obvious that the predominance of lower order odd harmonics (LOH) or triplen harmonics ranging from V1, V3 to V11 for 3-level inverter is more represented in Figure 9 compared to 5-level inverter in Figure 10. Due to this reason a large filter is used at load end to reduce these triplen harmonics in terms of its line current, load voltage, and load current for 3-level inverter where as in 5 level inverter all the harmonics are shifted beyond the 50th order resulting in smaller filters at load side to reduce

harmonics in line current and load voltage and current. So, this waveform in Figure 10 highlights the position of the harmonics in the harmonic spectrum resulting in reduced size of filter circuit with fewer components, and improved harmonic profiles Similarly, in Figure 11 the quality of ouput power is improved for a 5-level inverter [21], there is a significant increase in output PF compared to 3-level inverters.

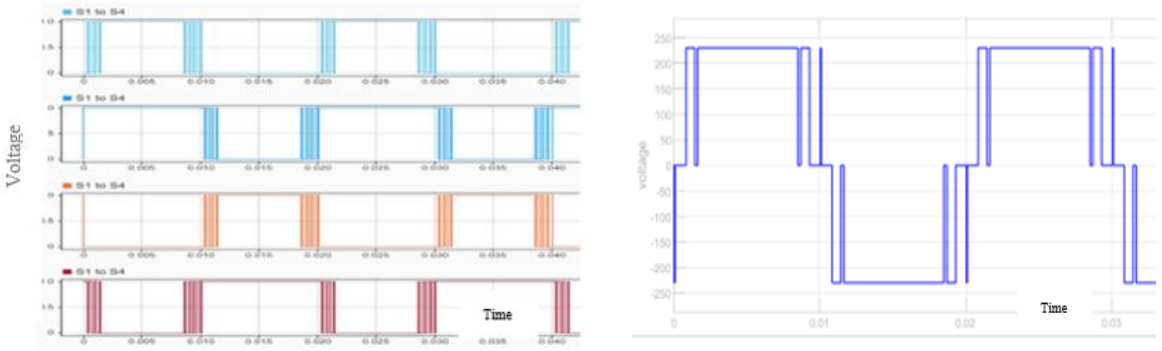
Table 1. Switching sequence of five level multilevel inverter

S1	S2	S3	S4	S5	S6	S7	S8	Voltage level
1	1	0	0	1	1	0	0	$+2V_{DC}$
1	1	0	0	0	0	0	0	$+V_{DC}$
0	0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	0	$- V_{DC}$
0	0	1	1	0	0	1	1	$-2V_{DC}$



(a) (b)

Figure 7. Five-level MLI (a) PWM pulses and (b) output voltage



(a) (b)

Figure 8. Three-level CHB MLI with PsD PWM (a) PWM pulses and (b) output voltage

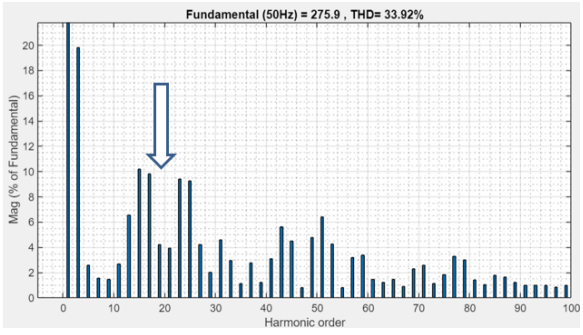


Figure 9. % V_{THD} analysis of 3-level inverter

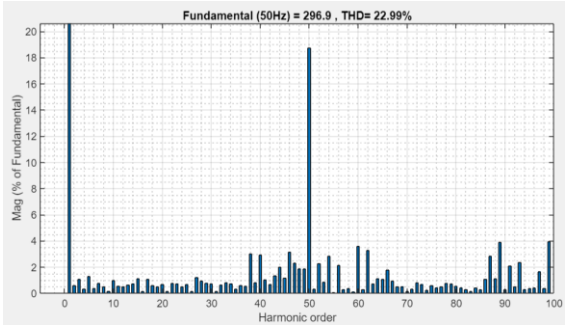


Figure 10. % V_{THD} analysis of 5-level inverter

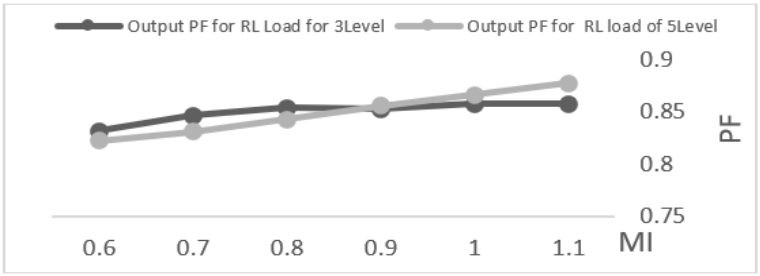


Figure 11. PF verses MI (3 level and 5 level) of CHB MLI with PsD PWM

2.3. Filter design: analysis of L, LC, and LC with damping resistance

The loads in a grid-connected system are getting increased day by day to accommodate the demand-supply equilibrium. With the increase in the loads, the faults and other phenomena which affect the stability are rapidly increasing. To mitigate these problems between the converter and the grid, filters are connected between them. These filters limit the current harmonics even in the worst conditions and cannot pass them to the grid directly.

2.3.1. L filter

Single-tuned shunt L filters are simple, less expensive, and normally preferred for voltage source converters. These filters provide the least impedance path to the harmonics of a particular frequency. But, due to larger value of L that makes the circuit bulky and costly. The value of inductance preferred should be below 21% during normal operation [22]. The current ripple can be found as in (1).

$$I_{ripple} = \frac{0.2\sqrt{2}\,\mathrm{P}}{3\frac{Vl}{\sqrt{3}}} \quad (1)$$

The following traits are considered for the L filter: low-pass filter (first-order), cut-off frequency of ωL = R/L, resonance frequency f_{res} (10 times higher), network frequency (f_o) (10 times higher), switching frequency (f_{sw}) and the filter inductance is given by (3).

$$10fo \leq fres \leq fsw \quad (2)$$

$$L_i = \frac{\left(Vdc - \frac{Vdc}{2}\right)}{4.f_{sw}\, I_{ripple}} \quad (3)$$

2.3.2. LC filter

LC filter is a low pass filter (second order) which has better-damping behavior compared to L filter. This is adept at attenuating most of the lower harmonics [LOH] in the output voltage waveform. Both 'L' and 'C' are energy storage components. The L is connected in series and the capacitor is in parallel to the load. This LC filter has a noteworthy impression on the performance that reduces the distortions at high frequency by controlling the switching current. Considering the ripple current [22] designed in an L filter with a 20% deviation, the resonance frequencies are calculated at each switching frequency. The resonance frequency is administered by the (4).

$$10Fo \leq F\ res \leq F\ sw \quad (4)$$

The F_{res} is calculated by considering the maximum and minimum values of resonating frequency as (5),

$$F\ res = F\ res(min) + 0.5\ F\ res(max) \quad (5)$$

where $F_{res}(min) = 10F_o$ and $F_{res}(max) = 0.5\ f_{sw}$. F_o - reference voltage frequency (50 Hz), F_{sw} - switching frequency and F_{res}- filter cut-off frequency.

$$F_{res} = \frac{1}{2\pi\sqrt{LC}} \quad (6)$$

2.3.3. LC filter with damping resistance

Up till now L and LC filters have been preferred for the inverters but owing to the various factors discussed in the above sections under the same conditions L and LC filters are designed at resonating frequency F_o and switching frequency F_{sw}. Now, we will consider a damping resistance connected along the capacitor circuit which is parallel to inverter circuit results in much lesser THD compared to the L and LC filter. The L and C parameters are considered same as listed in Table 2 i.e., L=4 mH, C=5µF at 3,500 switching frequency that generates a less THD, by adding damping resistance there is a drastic decrease in THD that is calculated using (1) from literature. The calculated values (approximately) are,

$$R = \frac{\sqrt{\frac{L}{C}}}{Q} \quad \text{where Q is quality factor } 20<Q<100 \tag{7}$$

the range of quality factor for a single tuned filter is considered as 20, R=1.41Ω.

3. RESULTS AND DISCUSSION

With a thorough discussion on the types of filters available in literature for designing it in this paper we consider (6) as listed in Table 2 are designed at different switching frequencies (F_{sw}) with 1.5 KHz [23] intervals along with maximum (F_{res}(max)), minimum (F_{res}(min)) and resonant frequency (F_{res}). With capacitor value chosen arbitrarily as C=5µF the waveform of current is nearly equal to the sine wave as conferred in the subsection 3.4 effect of change in % V_{THD} and V_{RMS} with change in switching frequency (with and without filter). The electromagnetic interference problems can also be eliminated by placing a properly designed low-pass LC filter. Further, the performance analysis of three-level and five-level inverters are also extended to investigate different parameters described in Table 2.

Table 2. Filter inductance design at different switching frequencies

F_{SW}	F_{res}(min)	F_{res}(max)	F_{res}	L(mH)
1,500	500	750	625	12.9
2,500	500	1,250	875	6.6
3,500	500	1,750	1,125	4.0
4,500	500	2,250	1,375	2.67

3.1. Effect of change in the fundamental RMS output voltage and current in FFT analysis

Figures 12 and 13 illustrate the V_{RMS} and I_{RMS} as a function of modulation index (MI) varying from 0.6 to 1.1 for 3-level (3L) and 5-level (5L) multilevel inverters with switching frequencies of 2.5 KHz. It is analyzed from the plot that the RMS voltage [V_{RMS}] is increased from 125.6 V to 225.3 V by increasing the modulation index from 0.6 to 1.1 without using any filter elements.

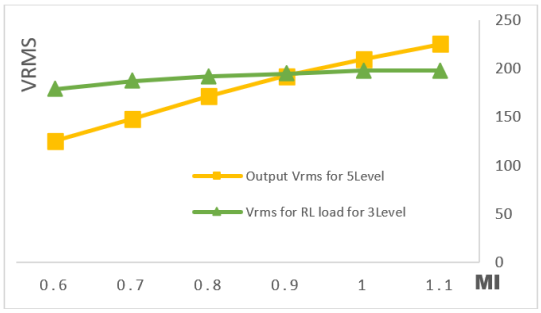


Figure 12. V_{RMS} for 3 and 5 level CHB MLI w.r.t MI

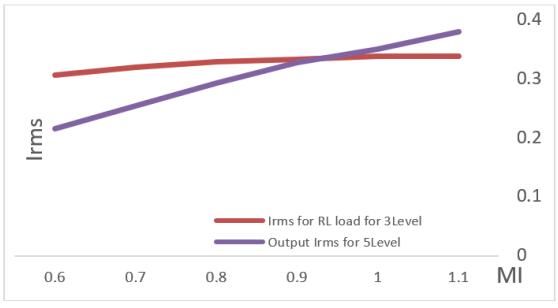


Figure 13. I_{RMS} for 3 and 5 level CHB MLI w.r.t MI

3.2. Effect of change in the % V_{THD} [24]

The visual evidence indicates a substantial reduction in %THD by varying the MI from 0.6 to 1.1 in Figure 14. If the MI<0.6 the 5-level inverter generates a 3-level output voltage and the 3-level inverter generates a 2-level output voltage because of which the harmonic analysis is limited to 0.6 modulation index. Figure 14 shows the harmonics generated for 3-level and 5-level CHB MLI where it is witnessed that the

harmonics generated by 3 levels are high about 33.15% compared with the 5-level inverter which is 22.99% with a modulation index 1. The V_{THD} of five-level CHB MLI is reduced from 33.15 % to 22.99% by shifting all the lower order harmonics to the 50th order shown in Figure 10 which satisfies the condition of IEEE STD 519-2022. Further, with the MI from 0.6 to 1.1 the harmonics generated are also reduced to five levels than three level inverters.

3.3. Effect of change in number of levels (with PDPWM), change in switching frequency (with PD, POD, and APOD PWM) versus % V_{THD} and V_{RMS}

With the staircase waveform exhibits better quality and a better harmonic profile. Hence, the filter requirement can be drastically reduced. Figure 15 elaborates the idea of increasing the output voltage levels the overall percentage harmonics generated by 3, 5, 7 level inverter gradually decreased.

Suppose Fc is the carrier frequency at 3.5 KHz and Fr is the modulating frequency of 50 Hz then the modulation index (Mf) is ratio of carrier frequency to modulating waveform. So, Mf=70, the harmonics in sinusoidal PWM resides at Mf, 2* Mf, 3* Mf times the fundamental in harmonic spectrum and so on. But, apart from this main harmonic that exists we also have side bands that exists at (j* Mf±k) where j=1 then k=2, 4, 6 and if j=2 then k=1, 3, 5 which means if j=odd, k=even and vice versa. From Table 3 the PsD PWM and POD PWM results are similar from 1.5 KHz to 4.5 KHz later a drastic change in %THD and Vrms illustrated in Figures 16 and 17 respectively. By simulating the five-level inverter at different switching frequencies in this paper we conclude that with 1.5 KHz the lower order harmonics [LOH] generated in PsD PWM resides at a side band range around 30th order as discussed above with %THD-23.85% compared to the frequencies at 2.5 KHz at 50th with %THD-22.99%, 3.5 KHz at 70th with %THD-21.84% and 4.5 KHz at 90th with %THD-19.42% as shown in Figure 18. So, the main harmonics resides at 30th, 50th, 70th, and 90th order for five level inverters.

Table 3. Mathematical modeling and analysis of five level inverter with PD, POD, APOD PWM of LSPWM

Switching Frequency (KHz)	% V THD (PsD PWM)	% V THD (POD PWM)	% V THD (APOD PWM)	Output Vrms (PsD PWM)	Output Vrms (POD PWM)	Output Vrms (APOD PWM)
1.5	23.85	23.18	23.66	213.1	214.4	214.6
2.5	22.99	22.84	22.69	210	210	209.5
3.5	21.84	21.81	21.99	209.6	208.8	209.2
4.5	19.42	20.7	20.6	214.1	212.1	212.3

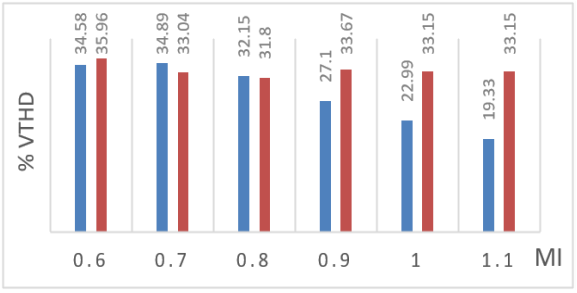


Figure 14. % V_{THD} of 3 level and 5 level inverters

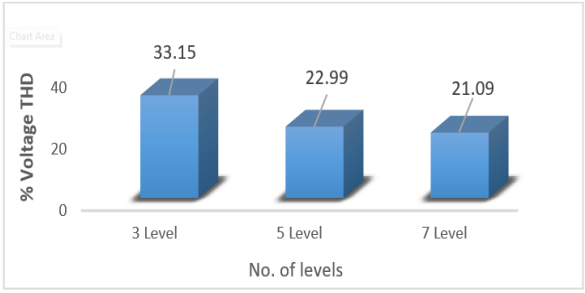


Figure 15. %V_{THD} v/s no. of levels (PDPWM)

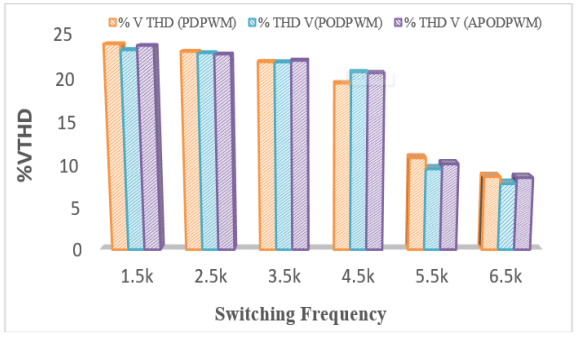


Figure 16. %V_{THD} verses switching frequency

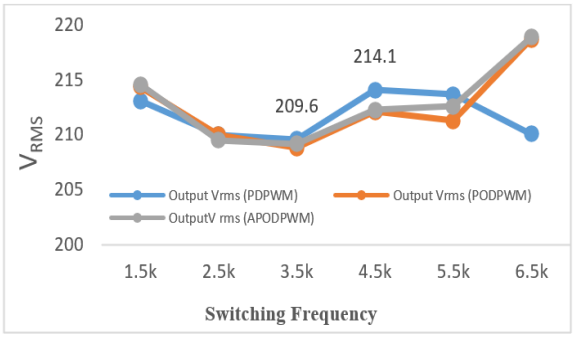


Figure 17. V_{RMS} versus switching frequency

By increase in switching frequency (Fsw) of carrier signals it is possible to eliminate lower-order triplen harmonics shown in Figure 18. What is important here is to see the position of harmonics because this one of the factors considered for designing a filter. It is also necessary to observe the point of corner frequency of the filter. Thus, the waveform in Figure 18(a) at 1.5 KHz harmonics resides at 30th order followed by 2.5 KHz at 50th order in Figure 18(b), 3.5 KHz at 70th order and 4.5KHz at 90th order represented in Figure 18(c) and Figure 18(d) respectively. Thus, shift in position of harmonic order in harmonic spectrum resulting in reduced size of filter circuit with fewer components, and improved harmonic profiles. The filter corner frequency of harmonics can be shifted if switching frequency of converter is increased. From the harmonic and filter point of view, value of Mf should be very large. Larger the value of Mf, smaller will be the size of filter. This noteworthy enhancement validates the efficacy of adopting this analogy to improve the performance. On the contrary, the increased value of Mf causes more losses in the converter because more number of switching happening in the converter. So, usually for low power rating, within 5 KW switching frequency of 20 or 40 KHz is quite acceptable. But, with high power applications say in MW level, switching frequency of converter has to be sufficiently low. Thus, consider the converter with less switching frequency around 200-300 Hz, but that will impose a lot of restriction on the filter design because the filter will then become very bulky. So, if we choose the corner frequency in an optimized way, then for all the harmonics considered here, the filter gain is 0. This arrangement provides boosting voltages along with enhancing the power quality [25]. For further analysis, the PsD PWM approach at a switching frequency of 3.5 KHz is taken into consideration.

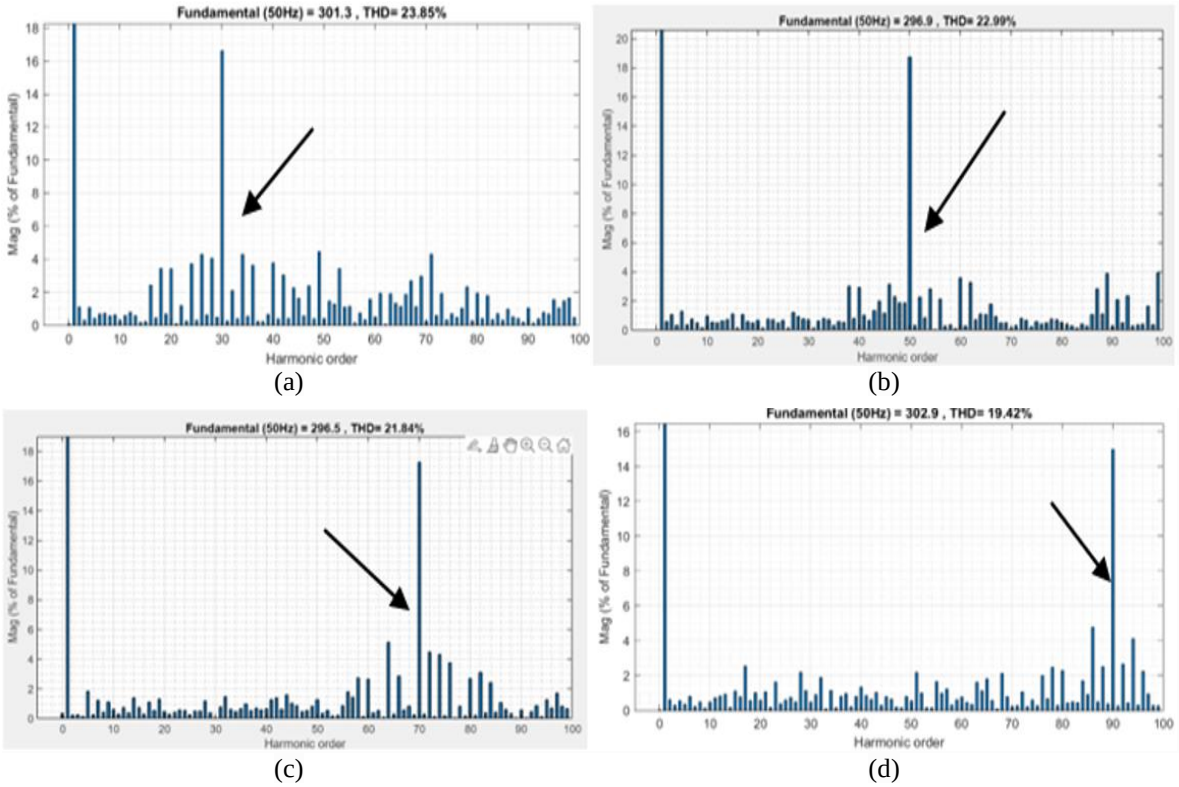


Figure 18. Shifting the position of harmonics by changing the Fsw; (a) 1.5 KHz, (b) 2.5 KHz, (c) 3.5 KHz, and (d) 4.5 KHz

3.4. Effect of change in % V_{THD} and V_{RMS} with and without filter at 3.5 KHz

The proposed 5-level CHB MLI is simulated in MATLAB Simulink with C=5µF and L=4 mH at different switching frequency as depicted in Table 4. Among all switching frequency the optimized performance is observed at 3.5 KHz with better quality and reduced harmonic in harmonic spectrum and increase in RMS value of output voltage is attained. Figure 19 also illustrates the improvement in power quality in-terms of rms value of output current and output voltage with and without filter elements operated at optimized frequency of 3.5 KHz that is derived from subsection 3.3 shown in Figures 19(a) and 19(b).

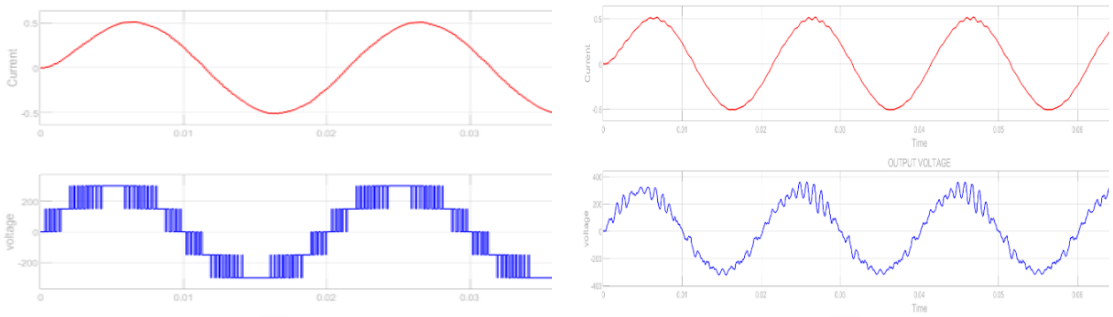
THD is much less for the CHB MLI at 3,500 Hz which points out that CHB with filter (LC) can spawn a better quality of sine signal. Because of the nonlinearity in CHB configuration resulting from body diode that generates a few voltage levels. Figure 19(b), exemplifies the brief idea about the better performance of 5-level CHB MLI that is more suitable based on operating frequencies with filter when compared to without filter in Figure 19(a). The voltage waveform of an inverter without a filter is typically a square wave or a staircase waveform with very high ripple current not suitable for most applications. Thus, with filter elements the quality is improved compared to without filter that results in reducing the EMI and increase the life of the switches. Furthermore, the %THD of phase voltage is 21.84% with a peak-peak fundamental voltage of 296.5 V. The dominant harmonics are situated at 70th order without any filter circuit with a THD of 21.84% but, with LC filter designed in this paper the harmonics is reduced to 14.72% with dominant harmonics residing at 25th order which is less that 8% as shown in Figure 20. Additionally, LC filter with damping resistance in Figure 21 elaborates that the harmonics are further reduced to 11.48% where all the subharmonics in the side band range can be neglected as it satisfies the IEEE standards. With an appropriate filter element design, as shown in Table 5 and covered in detail under sections 3 and 4, we can obtain a lower percentage of THD from the level shift PsD PWM technique when comparing the results obtained from proposed MLI in this paper to some of recent papers in the literature.

Table 4. RMS voltage, harmonics with and without filter elements for PsD PWM

Fsw (KHz)	% VTHD with filter	% VTHD without filter	Vrms without filter	Vrms with filter
1.5	20.72	23.85	213.1	214.1
2.5	21.04	22.99	210	210.6
3.5	14.72	21.84	209.6	210.1
4.5	25.98	19.42	214.1	213.4

Table 5. Compared to some recent studies published in the literature, the suggested inverter

Ref/Year	1/2023	24/2022	15/2020	22/2019	2/2022	Without filter	LC filter	LC damping resistance
%THD[V]	30.26	34.64	24.12	80.43	20.60	21.84	14.72	11.48



(a) (b)

Figure 19. Vrms and Irms of 5-level CHB MLI (a) without filter and (b) with filter

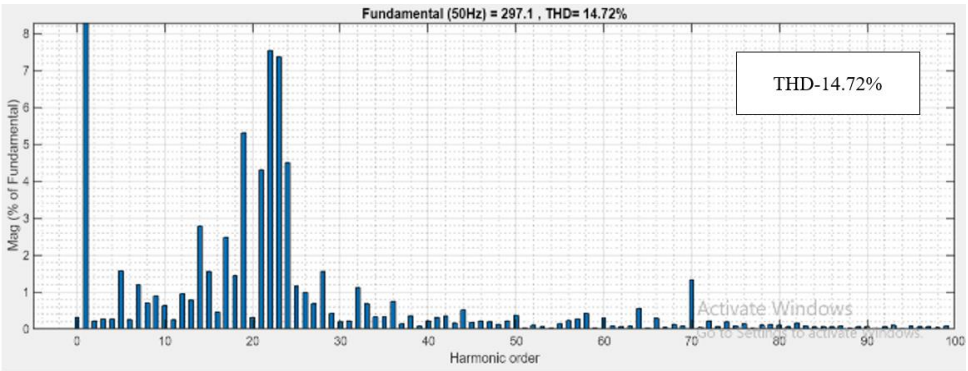


Figure 20. FFT analysis with filter

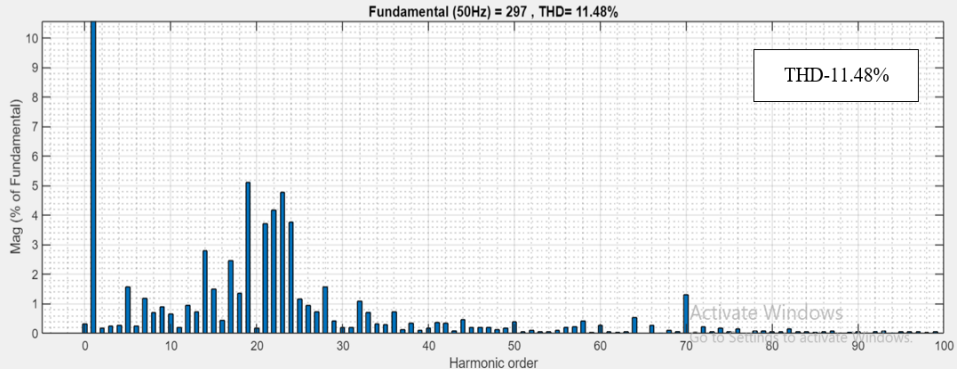


Figure 21. FFT analysis LC damping resistance

4. CONCLUSION

In this paper, 3-level and 5-level inverters are compared to determine the various performance parameters with level shift PsD PWM technique compared to the other technique as it resulted in noteworthy enhancement in shifting of all the lower order odd harmonics above 50^{th}-70^{th} order thereby improving the quality of output power with increase in the switching frequency. Thus, the optimized switching frequency of 3.5 KHz is obtained. As the number of levels increases the quality of the power is also improved by decreasing the %THD. The effect of change in the MI and designing inverter at optimal switching frequency to improve RMS output voltage is discussed in detail. This papers also compares the significance of lower odd harmonics generated in three and five level inverters to determine corner frequency of the filter, depending on the position of harmonics. The filter corner frequency of harmonics can be shifted if switching frequency of the converter is increased that makes a way to design a large filter circuit that is bulky. Filters designed with LC and LC with a damping resistance at optimal switching frequency of 3.5 KHz demonstrates that without filter though harmonics resides at 70^{th} (17%) order but the overall %THD is 21.84,that is reduced when compared to LC filter where harmonics resides at 23^{rd} and 25^{th} order (peak value <8% including all individual subharmonics also in the side band) with the absence of lower order triplen harmonics (3^{rd}, 5^{th}, 7^{th} …) with overall %THD 14.72 and further to enhance the quality LC with a damping resistance filters are used with overall %THD 11.48 harmonics residing at 19^{th}, 23^{rd}, and 25^{th} order which is less than 5% that satisfies the IEEE STD 519-2022 including the side bands subharmonics also. Thus, quality of power is improved for proposed multilevel inverter with LC filter and LC damping resistance filter.

REFERENCES

[1] M. H. Ali, E. A. Mainul, T. Rahman, M. S. Hossen, M. K. A. Khan, and M. O. Rahman, "Five-level cascaded H-bridge inverter for renewable energy applications," *Indonesian Journal of Electrical Engineering and Computer Science (IJEECS)*, vol. 31, no. 1, pp. 44–53, Jul. 2023, doi: 10.11591/ijeecs.v31.i1.pp44-53.

[2] V. Korde, N. Sute, V. B. Borghate, and V. M. Korde, "Analysis of control techniques and filter design of multilevel inverter," 2022, pp. 571–588.

[3] I. Villanueva, N. Vázquez, J. Vaquero, C. Hernández, H. López, and R. Osorio, "L vs. LCL filter for photovoltaic grid-connected inverter: a reliability study," *International Journal of Photoenergy*, vol. 2020, pp. 1–10, Jan. 2020, doi: 10.1155/2020/7872916.

[4] S. Shuvo, E. Hossain, T. Islam, A. Akib, S. Padmanaban, and M. Z. R. Khan, "Design and hardware implementation considerations of modified multilevel cascaded H-bridge inverter for photovoltaic system," *IEEE Access*, vol. 7, pp. 16504–16524, 2019, doi: 10.1109/ACCESS.2019.2894757.

[5] M. Jayaraman and V. T. Sreedevi, "Power quality improvement in a cascaded multilevel inverter interfaced grid connected system using a modified inductive-capacitive-inductive filter with reduced power loss and improved harmonic attenuation," *Energies*, vol. 10, no. 11, p. 1834, Nov. 2017, doi: 10.3390/en10111834.

[6] I. H. Shanono, N. R. H. Abdullah, and A. Muhammad, "Filter design for a nine level voltage source inverter for renewable energy applications," in *Lecture Notes in Electrical Engineering*, vol. 538, 2019, pp. 571–585.

[7] R. Palanisamy, S. S. Dey, A. Rana, D. Karthikeyan, and D. Selvabharathi, "Simulation of novel 9-level inverter topology with reduced number of switches," *International Journal of Electrical Engineering and Technology*, vol. 11, no. 3, pp. 58–65, 2020.

[8] K. Selvakumar and P. D. Patel, "Single phase five-level inverter topology with reduced number of switches for PV application," *Materials Today: Proceedings*, vol. 45, pp. 2730–2736, 2021, doi: 10.1016/j.matpr.2020.11.598.

[9] S. Maurya, D. Mishra, K. Singh, A. K. Mishra, and Y. Pandey, "An efficient technique to reduce total harmonics distortion in cascaded h- bridge multilevel inverter," in *Proceedings of 2019 3rd IEEE International Conference on Electrical, Computer and Communication Technologies, ICECCT 2019*, Feb. 2019, pp. 1–5, doi: 10.1109/ICECCT.2019.8869424.

[10] "Cascaded multilevel inverter topology with SPWM and selective harmonic elimination modular techniques-a review," 2020, doi: 01.1617/vol7/iss11/pid48253.

[11] H. A. Khalif, J. K. Abed, and A. J. Mahdi, "A comparative Analysis of Multi-Level Inverters Supplied by Photovoltaic Panels based on THD and Filter Size by using POD-SPWM Technique," *IOP Conference Series: Materials Science and Engineering*, vol. 1105, no. 1, p. 012011, Jun. 2021, doi: 10.1088/1757-899x/1105/1/012011.

[12] K. Fernand Koffi, A. Raoule, D. Landry, G. Loum, and O. Asseu, "New method of sizing a filter (Rl-C) for an inverter with spwm control in medium voltage alternating," *International Journal of Advanced Research*, vol. 9, no. 04, pp. 34–43, Apr. 2021, doi: 10.21474/ijar01/12654.
[13] M. J. Sathik and D. J. Almakhles, "Common ground type five level inverter with voltage boosting for PV applications," *Scientific Reports*, vol. 12, no. 1, p. 4924, Mar. 2022, doi: 10.1038/s41598-022-09008-z.
[14] U. P. Yagnik and M. D. Solanki, "Comparison of L, LC & LCL filter for grid connected converter," in *Proceedings - International Conference on Trends in Electronics and Informatics, ICEI 2017*, May 2017, vol. 2018-January, pp. 455–458, doi: 10.1109/ICOEI.2017.8300968.
[15] P. N. Champa, A. Abhay Deshpande, and K. Venkatesha, "Comparative analysis of five level cascaded multilevel inverter by level shift & phase shift PWM techniques," in *2023 5th International Conference on Electrical, Computer and Communication Technologies, ICECCT 2023*, Feb. 2023, pp. 1–7, doi: 10.1109/ICECCT56650.2023.10179647.
[16] P. S. Chavali, P. V. R. Rao, and M. U. Vani, "A novel multilevel inverter with reduced number of switches using simplified PWM technique," *Journal of The Institution of Engineers (India): Series B*, vol. 101, no. 3, pp. 203–216, Jun. 2020, doi: 10.1007/s40031-020-00446-9.
[17] M. Büyük, A. Tan, M. Tümay, and K. Ç. Bayindir, "Topologies, generalized designs, passive and active damping methods of switching ripple filters for voltage source inverter: a comprehensive review," *Renewable and Sustainable Energy Reviews*, vol. 62, pp. 46–69, Sep. 2016, doi: 10.1016/j.rser.2016.04.006.
[18] S. S. Barah and S. Behera, "An optimize configuration of H-bridge multilevel inverter," in *ICPEE 2021 - 2021 1st International Conference on Power Electronics and Energy*, Jan. 2021, pp. 1–4, doi: 10.1109/ICPEE50452.2021.9358533.
[19] K. Muralikumar and P. Ponnambalam, "Analysis of cascaded multilevel inverter with a reduced number of switches for reduction of total harmonic distortion," *IETE Journal of Research*, vol. 69, no. 1, pp. 295–308, Jan. 2023, doi: 10.1080/03772063.2020.1819450.
[20] D. Kumar, R. A. Raj, R. K. Nema, and S. Nema, "A novel higher level symmetrical and asymmetrical multilevel inverter for solar energy environment," *IETE Journal of Research*, vol. 68, no. 5, pp. 3670–3682, Sep. 2022, doi: 10.1080/03772063.2020.1774429.
[21] S. Swathy, N. Niveditha, and K. S. Chandragupta Mauryan, "Design of five-level cascaded H-bridge multilevel inverter," in *Lecture Notes in Electrical Engineering*, vol. 626, 2020, pp. 65–80.
[22] A. Khoshkbar-Sadigh, V. Dargahi, K. Lakhera, and K. Corzine, "Analytical design of LC filter inductance for two-level inverters based on maximum ripple current," *IECON Proceedings (Industrial Electronics Conference)*, vol. 2019-October, pp. 1621–1626, 2019, doi: 10.1109/IECON.2019.8926919.
[23] I. M. Al-Adwan and Y. A. Al Shiboul, "Effect of the modulation index and the carrier frequency on the output vol tage waveform of the spwm voltage source inverter," in *Proceedings of the 17th International Multi-Conference on Systems, Signals and Devices, SSD 2020*, Jul. 2020, pp. 960–968, doi: 10.1109/SSD49366.2020.9364104.
[24] A. Chappa, S. Gupta, L. K. Sahu, S. P. Gautam, and K. K. Gupta, "Symmetrical and asymmetrical reduced device multilevel inverter topology," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 1, pp. 885–896, Feb. 2021, doi: 10.1109/JESTPE.2019.2955279.
[25] K. Chenchireddy and V. Jegathesan, "CHB multilevel inverter with sliding mode controller for DSTATCOM applications," *International Journal of Power Electronics and Drive Systems (IJPEDS)*, vol. 14, no. 4, pp. 2195–2203, 2023, doi: 10.11591/ijpeds.v14.i4.pp2195-2203.

BIOGRAPHIES OF AUTHORS

Champa Patanegere Nagarajappa is currently undergoing a Ph.D. in Power Electronics from Visvesvaraya Technological University, Belgaum. She is an Assistant Professor at the Department of Electrical and Electronics Engineering, BNM Institute of Technology, Bangalore. Her research interests include power converters, Industrial Drives application and renewable energy. She has also received a design patent for guiding a project on "A smart solar bench". She can be contacted at email: champapn@bnmit.in.

Dr. Abhay Anandarao Deshpande holds a Ph.D. in Robotics from Visvesvaraya Technological University, Belgaum He is working as Associate Professor in the Department of Electronics and Communication Engineering, RVCE, Bangalore. His research interest includes power electronics, robotics. He has also received patent grants for his projects on "Electronic nose system for food applications", and "A handheld hidden camera detecting device". He can be contacted at email: abhayadeshpande@rvce.edu.in.