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Dual tri-isolated DC H-6 inverter with minimal power components design

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ABSTRACT

Multilevel inverters have been forecasted in recent years for industrial and renewable energy applications due to its inherent characteristics of shaping the output voltage nearer to sinusoidal shape through concatenating several two/three level inverters using isolated DC sources or DC-link capacitors. However, the classical topologies used for synthesizing stepped voltage have several outwards like more number of DC sources or DC-link capacitors and switching devices used. In this paper, an effort has been sighted to bring a new topology for generating stepped voltage to overcome the above mentioned demerits. In addition to this, a new digital pulse width modulation (PWM) strategy is developed in-line with a new topology to eliminate the use of carrier and reference signals. The performance of the proposed topology and developed control strategy are evaluated in MATLAB/ Simulink platform and an laboratory prototype is constructed for experimental investigations to accord the simulation results.

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1. INTRODUCTION

The multilevel inverters (MLIs) basically originate from the three level neutral point clamped inverter and find extensive use for utility applications that include reactive power compensation and variable speed drives. The other MLI variants include flying capacitor and cascaded H-Bridge inverters [1]. A transformer based single source MLI using conventional three phase two level inverters and two single phase cascaded H-Bridge inverters requires transformers to feed input voltage using a single DC source [2]. The main advantage relates to the use of a single DC source, but suffers with a need to handle the inductor current with proper design [3]. The attempt owes to introduce a H-6 inverter type topology for a single phase MLI with two voltage generation modules and generate a large number of voltage levels. It envisages assembling the voltage generation module in order that that it produces the desirable number of voltage levels with reduced switches in the current conduction path. A new single-source high step-up asymmetrical MLI topology using voltage multiplier circuits is developed in [4]. The developed converter employs a single DC source and a high-frequency AC inverter to charge a series of capacitors, iterating multiple times based on the input DC voltage.

Tran *et al.* [5], a novel switched capacitor topology is proposed to synthesize a 6-step voltage at the load terminals. This approach addresses capacitor balancing challenges by directly charging from the input voltage source [6]. Proposing an H-shaped DC source connection to reduce switching devices for higher

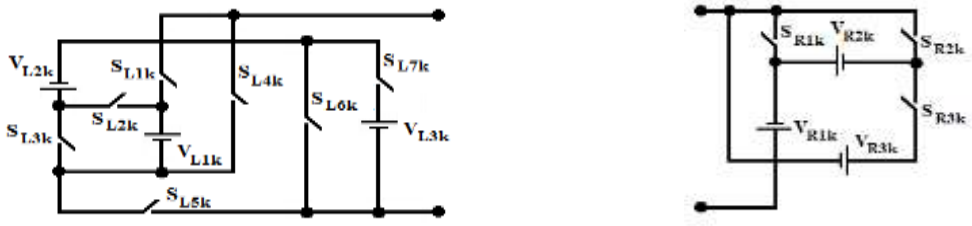
voltage. Yet, the structure seems complex and lacks fault tolerance [7]. Four DC sources linked back-to-back via an H-6 inverter cut total power components. The topology appears simple; one DC source isolates, enhancing efficiency [8]. The new varieties of MLI topologies for renewable energy interface have been introduced in [9] which require capacitor voltage balancing techniques for balancing the output voltage. A dual H-Bridge with voltage ratio 1:3 is connected in star connection for three phase topology is developed to offer more number of voltage levels with reduced switching devices [10]. A single voltage source and capacitor switched module to generate 5- level and several voltage module are added further to increase the voltage levels is formulated in [11]. The topology appears simple, needing six switches vs. traditional H-Bridge inverters. A dual DC source in an H-shape generates more voltage levels, with added structures for expansion. This design reduces conducting devices while elevating voltage levels [12]. An 11-level inverter for PV applications is developed using flying capacitors and it looks free from unbalancing capacitor voltage problems [13]. A series of three phase inverters with coupling transformers is introduced to generate large number of voltage levels. The topology is derived from single phase inverter structure and suitable for grid connected systems [14]. A series of H-Bridge inverters with single DC source and capacitors to formulate asymmetrical MLI topology for three phase circuits and the topology requires separate control for capacitor voltage balancing [15]. A cluster of H-Bridge inverters with output transformers and charged by a single DC source for MLI structure to produce good quality output voltage. The developed topology is operated in asymmetrical configurations and requires output transformers for isolating the H-bridges for synthesizing the voltage levels [16]. T-type switches for multilevel boost in PV face voltage imbalance, needing balancing [17]. Hybrid 9-level inverter for grid integration minimizes switches, enhances control, incorporates innovative capacitor balancing, and achieves filter-less operation with output-coupled inductors [18]. A 7-level compact module for synthesizing stepped voltage waveform is developed in [19] which comprises of 3 isolated DC sources and several bi-directional switches. Inverter extended for more voltage levels with simple structure. Cascaded switched-diode isolated DC sources form MLI, requiring high-blocking devices at the H-bridge [20]. Modify ring-connected multilevel voltage source inverter for improved fault tolerance [21]. Capacitor-assisted MLI needs dependent control for voltage balancing [22]. Dual DC sources with H-6-bridge inverter synthesize stepped voltage efficiently [23]. Developed PSO-based optimization to remove output voltage harmonics in cascaded H-Bridge [24]. Novel pulse width modulation (PWM) minimizes CMV via zero CMV vectors in space-carrier methods [25].

This paper has two folds, a fresh topology based on two voltage generation modules and H-6 inverter is developed with a view to generate large number of voltage levels and a digital PWM strategy is formulated for minimizing lower order harmonic magnitudes with desired fundamental output voltage and lesser THD. The voltage generation module is assembled in such a way that it produces voltage levels with reduced switches in current conduction path. Three mathematical equations are formulated to operate the developed topology in asymmetrical configuration to synthesize various values of output voltage levels. The developed topology is investigated with MATLAB based simulated response and a laboratory prototype for experimental results.

2. DEVELOPED TOPOLOGY

The main objective of developing MLI topologies is to acquire load voltage with lesser harmonic distortion and it follows the path of sinusoidal nature. Several MLI topologies are originated to meet the above specific requirements and however it has several disadvantages like more switching devices and DC sources in its structure. The MLI topology is assembled with the help of two voltage generation modules and an H- Bridge inverter is shown in Figure 1. The voltage generation module shown in Figure 1(a) is comprised of three voltage sources (VL1k- VL3k) and the switching devices (SL1k-SL7k) for connecting the DC source (VL2 and VL3) in adding/opposing direction with the voltage source (VL1) for generating the voltage levels. The switches (SL1k and SL5k) are used for connecting the voltage source (VL1k), while the switch (SL4k) for bypassing the voltage source (VL1k) with the load. The developed voltage module can be operated in symmetrical and asymmetrical modes that generate 15- level in the output voltage. Similarly, the symmetrical topology depicted in Figure 1(b) is configured with three voltage sources (VR1k-VR3k) and the switches (SR1k-SR3k) for synthesizing 7- level in the output voltage. Figures 2 and 3 portrait the proposed 15- and 7-level inverter using the developed voltage generation module. Figure 4 envisages 33-level inverter using developed voltage generation module on either side of H-Bridge inverter. The Table 1 tabulates the switching sequence for possible combinations of voltage levels using the voltage sources (VL1k-VL3k) and (VR1k-VR3k) respectively. A developed voltage generation modules on either side of H-6 inverter produces all possible combinations of VL1, where ’P’ and ‘N’ denotes switches to be turn ON in positive and negative cycles respectively. If ‘k’ is the number of developed inverter shown in Figure 4, then the number of voltage levels and switching devices are [(32×k)+1] and (16×k) respectively. The blocking voltage across the each switch in the developed MLI is:

$V_{S_{L1k}} = V_{dc}$ $V_{S_{L2k}} = (3 \times V_{dc})$ $V_{S_{L3k}} = (3 \times V_{dc})$ $V_{S_{L4k}} = V_{dc}$ $V_{S_{L5k}} = (6 \times V_{dc})$ $V_{S_{L6k}} = (3 \times V_{dc})$ $V_{S_{L7k}} = (3 \times V_{dc})$ $V_{S_{R1k}} = V_{S_{R2k}} = V_{S_{R3k}} = (6 \times V_{dc})$ $V_{S_{1k}} = V_{S_{4k}} = (7 \times V_{dc})$ $V_{S_{2k}} = V_{S_{3k}} = (9 \times V_{dc})$ $V_{S_{5k}} = V_{S_{6k}} = (16 \times V_{dc})$



(a) (b)

Figure 1. Proposed voltage generation module comprised of three voltage sources (a) asymmetrical modes that generate 15- level and (b) symmetrical topology for 7- level

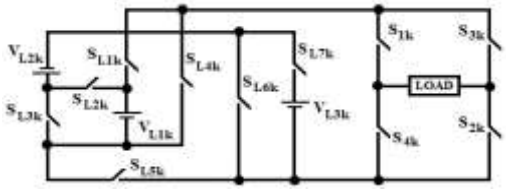


Figure 2. Proposed 15- level inverter

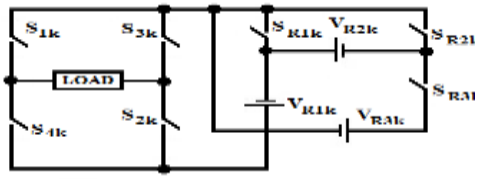


Figure 3. Proposed 7-level inverter

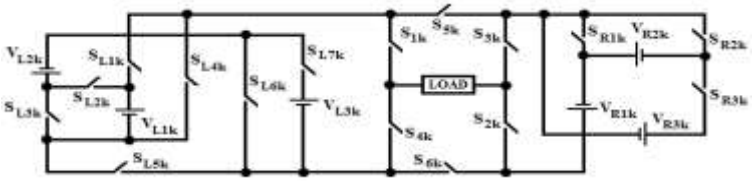


Figure 4. Proposed 33-level inverter

Table 1. Switching patterns for possible combinations of voltage source (V_{L1k})

Voltage level	S_{L1k}	S_{L2k}	S_{L3k}	S_{L4k}	S_{L5k}	S_{L6k}	S_{L7k}	S_{R1k}	S_{R2k}	S_{R3k}	S_{1k}	S_{2k}	S_{3k}	S_{4k}	S_{5k}	S_{6k}
V_{L1k}	√				√						P	P	N	N	N	P
V_{L2k}- V_{L1k}		√		√		√					P	P	N	N	N	P
V_{L2k}			√	√		√					P	P	N	N	N	P
V_{L2k}+V_{L1k}		√		√			√				P	P	N	N	N	P
(V_{L3k}+ V_{L2k}) - V_{L1k}			√	√			√				P	P	N	N	N	P
(V_{L3k}+ V_{L2k})	√		√				√				P	P	N	N	N	P
(V_{L3k}+ V_{L2k}+V_{L1k})		√		√			√				P	N	P	N	N	P
(V_{L3k}+ V_{L2k}+ V_{R1k})-V_{L1k}		√		√		√	√	√			P	N	P	N	N	P
(V_{L3k}+ V_{L2k}+ V_{R1k})			√	√		√	√	√			P	N	P	N	N	P
(V_{L3k}+ V_{L2k}+ V_{R1k})+ V_{L1k}	√		√			√	√	√			P	N	P	N	N	P
(V_{L3k}+ V_{L2k}+ V_{R1k}+ V_{R2k})- V_{L1k}		√		√			√		√		P	N	P	N	N	P
(V_{L3k}+ V_{L2k}+ V_{R1k}+ V_{R2k})			√	√			√		√		P	N	P	N	N	P
(V_{L3k}+ V_{L2k}+ V_{R1k}+ V_{R2k})+ V_{L1k}	√		√				√		√		P	N	P	N	N	P
(V_{L3k}+ V_{L2k}+ V_{R1k}+ V_{R2k}+ V_{R3k})- V_{L1k}		√		√			√			√	P	N	P	N	N	P
(V_{L3k}+ V_{L2k}+ V_{R1k}+ V_{R2k}+ V_{R3k})			√	√						√	P	N	P	N	N	P
(V_{L3k}+ V_{L2k}+ V_{R1k}+ V_{R2k}+ V_{R3k})+ V_{L1k}	√		√				√			√	P	N	P	N	N	P

3. OPTIMAL VOLTAGE MAGNITUDE SELECTION AND ITS EFFECT ON VOLTAGE LEVEL CONFIGURATION

It is worthwhile noted that the developed topology can be operated with various values of DC voltage magnitudes in DC sources to produce more number of voltage levels with minimal switching devices. Therefore, seven methods are formulated to obtain the value of DC sources in asymmetrical configuration for the topology portrayed in Figure 4. Table 2 emphasizes the mathematical equations required to attain the DC source magnitudes. Table 2 explores the methodology to determine the number of voltage levels using the proposed hex-DC sources MLI. Each method has its own merits in generating multistep voltage waveform with constant total voltage blocking devices. The magnitude of voltage sources used in the proposed MLI is arranged with different values to operate in symmetrical topology. There are seven voltage determination algorithms have been presented to project the merits of proposed topology in asymmetrical configuration is represented in Figure 5. The sixth algorithm in Table 2 portraits higher voltage levels with reduced number of switches is evident from Figure 6. On the other hand, the DC voltage sources with different voltage magnitude plays a typical role in selection of power rating of the devices. Increasing in power rating of the devices that leads rise in cost and however, reducing the current conducting devices in conduction path that improves efficiency with higher number of voltage levels.

Table 2. Mathematical relations to calculate DC source voltage

Method	Magnitude of DC voltage sources	Number of voltage levels (m)	Maximum peak output voltage (V)	Total blocking voltage (V)
I	$VL1k = Vdc$; $V_{L2k}= V_{L3k}= V_{R1k}= V_{R2k}= V_{R3k}=(2\times V_{dc})$	[(22×k)+1]	(11×k)×V_{dc}	(70×k)×V_{dc}
II	$V_{L1k}= V_{dc}$; $V_{L2k}= V_{L3k}=(2\times V_{dc})$; $V_{R1k}= V_{R2k}= V_{R3k}=(4\times V_{dc})$	[(34×k)+1]	(17×k)×V_{dc}	(116×k)×V_{dc}
III	$V_{L1k}= V_{dc}$; $V_{L2k}= V_{L3k}=(3\times V_{dc})$; $V_{R1k}= V_{R2k}= V_{R3k}=(6\times V_{dc})$	[(50×k)+1]	(25×k)×V_{dc}	(156×k)×V_{dc}
IV	$V_{L1k}= V_{dc}$; $V_{L2k}= V_{L3k}=(3\times V_{dc})$; $V_{R1k}= V_{R2k}= V_{R3k}=(5\times V_{dc})$	[(44×k)+1]	(22×k)×V_{dc}	(138×k)×V_{dc}
V	$V_{L1k}= V_{dc}$; $V_{L2k}=(2\times V_{dc})$; $V_{L3k}=(3\times V_{dc})$; $V_{R1k}= V_{R2k}= V_{R3k}=(7\times V_{dc})$	[(54×k)+1]	(27×k)×V_{dc}	(168×k)×V_{dc}
VI	$V_{L11}= V_{dc}$; $V_{L21}= V_{L31}=(3\times V_{dc})$; $V_{R11}= V_{R21}= V_{R31}=(6\times V_{dc})$; $V_{L1k}=(2\times V_{dc})$; $V_{L2k}= V_{L3k}=(6\times V_{dc})$; $V_{R1k}= V_{R2k}= V_{R3k}=(12\times V_{dc})$	[50×[(2×k)-1]+1]	25×[(2×k)-1] ×V_{dc}	156×[(2×k)-1] ×V_{dc}
VII	$V_{L11}= V_{dc}$; $V_{L21}= V_{L31}=(2\times V_{dc})$; $V_{R11}= V_{R21}= V_{R31}=(4\times V_{dc})$; $V_{L1k}=(2\times V_{dc})$; $V_{L2k}= V_{L3k}=(4\times V_{dc})$; $V_{R1k}= V_{R2k}= V_{R3k}=(8\times V_{dc})$	[34×[(2×k)-1]+1]	17×[(2×k)-1] ×V_{dc}	116×[(2×k)-1] ×V_{dc}

Figure 7 shows the variation of total blocking voltage against different levels for 'k'= 2. The sixth algorithm have slightly higher value in total blocking voltage compared with other algorithms, however it impacts drastic improvement in voltage levels profile. It is important to compare the developed MLI and other recent topologies to put forth its capabilities for various applications in terms of device count and current conducting switching devices for various voltage levels. If the current conducting devices are low in number, then the developed topology has lesser power loss which increases the efficiency.

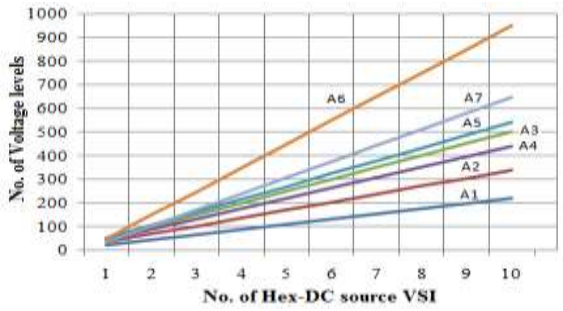


Figure 5. Variation of 'k' against voltage levels

Figure 6. Variation of voltage levels with different k= 2

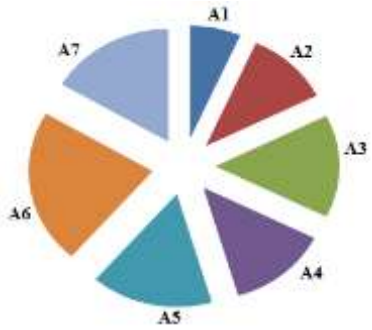


Figure 7. Variation of total voltage blocking standing magnitude for k=10

The topology needs several bidirectional and unidirectional switches to formulate its structure and for 33- level inverter it needs 30 switches and 9 DC sources, while the proposed topology requires 16 switches and 6 DC sources respectively. The topology requires several bi-directional switches and an H-Bridge inverter with unidirectional switches. The topology claims its novelty in terms of asymmetrical operation over the conventional topology. However, the topology requires more bidirectional switches compared with developed topology. Both the topologies require more switching devices in contrast with the proposed topology is evident from Figure 8. The total power loss in the proposed topology is decided by the number of switching devices in current conduction path. The proposed topology needs only a minimum switches in current conduction path compared with the recent topologies and it is evident from Figure 9. The total standing voltage of the switches decides the total cost of the inverter and therefore it is necessary to calculate the total standing voltage of the switches between the developed and recent topologies.

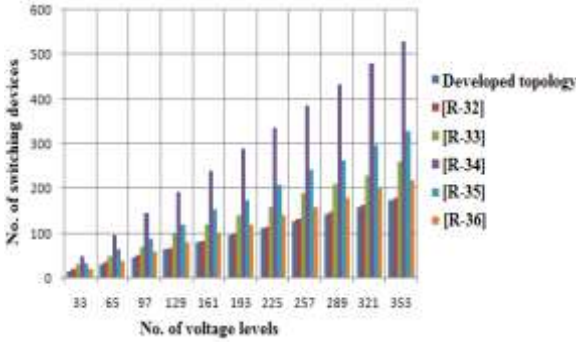


Figure 8. Variation of switching devices against different voltage level

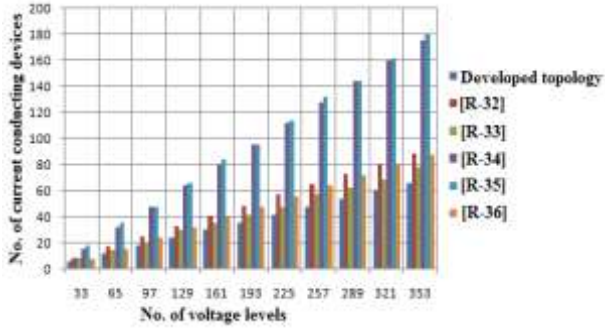


Figure 9. Variation of current conducting different voltage levels

4. SIMULATION AND EXPERIMENTAL RESULTS

The developed topology is simulated in MATLAB/Simulink environment with two voltage generation modules. The voltage generation modules produce 7 and 15- level in the output voltage when connected with an H-Bridge inverter individually. The input parameters considered for simulation study are V_{L1}= 40 V, V_{L2}=V_{L3}=120 V and V_{R1}=V_{R2}=V_{R3}= 100 V, RL load of 150 Ω and 100 mH respectively. The developed topology avails proposed fundamental switching frequency pulse generation method to synthesize the required voltage levels. The switching angles are (θ_1, θ_2, θ_3, θ_4, θ_5, θ_6, θ_7= 4.1, 12.38, 20.95, 30.04, 40.08, 51.95, 69.43) and (θ_1, θ_2, θ_3= 9.64, 30.21, 58.26), while the developed topology combining these 2 modules generate 33-level with an input voltage of V_{L1}= 20 V, V_{L2}=V_{L3}= V_{R1}=V_{R2}=V_{R3}= 60 V using same switching method. The switching angles are (θ_1, θ_2, θ_3, θ_4, θ_5, θ_6, θ_7, θ_8, θ_9, θ_{10}, θ_{11}, θ_{12}, θ_{13}, θ_{14}, θ_{15}, θ_{16}=1.79, 5.38, 8.99, 12.64, 16.34, 20.11, 23.97, 27.96, 32.10, 36.43, 41.03, 45.97, 51.41,57.59, 65.11, 76.45). The 7- level inverter using motor control pulse width modulator (MCPWM) gives an output peak fundamental voltage of 295.9 V and THD of 18.97%. The Figures 10-15 shows the output voltage with harmonic spectra and inductive load current for 7, 15 and 33-level inverters using the developed topology. The proposed topology produces its output voltage nearer to sinusoidal shape while increasing the number of voltage levels and the

THD for 7, 15 and 33- level inverter varies in the range of 12.56%, 5.57%, and 2.48% respectively. It is observed that the proposed control strategy proves its merit in terms of reduced THD for a target fundamental voltage compared with traditional MCPWM.

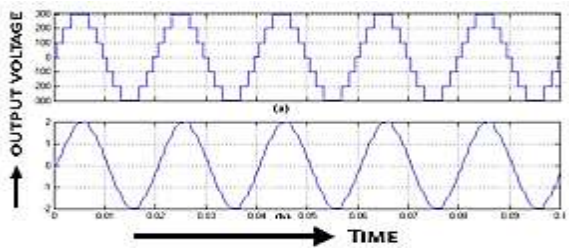


Figure 10. Output voltage and inductive load current-7 level inverter

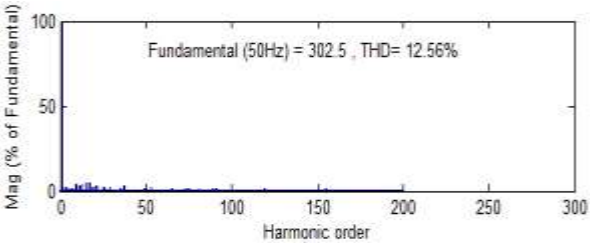


Figure 11. Voltage spectrum-7 level inverter

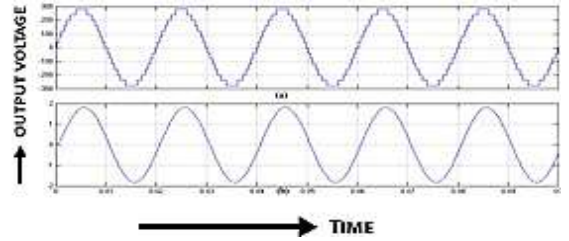


Figure 12. Output voltage and inductive load current-15 level inverter

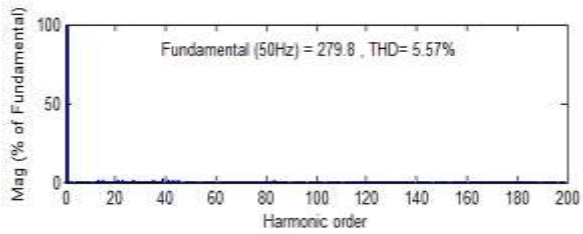


Figure 13. voltage spectrum-15 level inverter

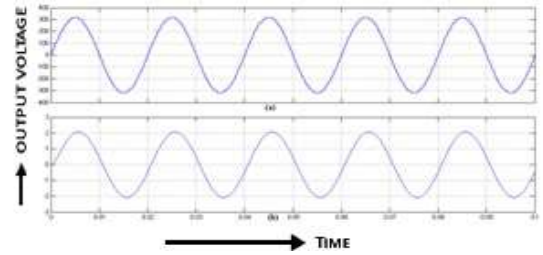


Figure 14. Output voltage and inductive load current-33 level inverter

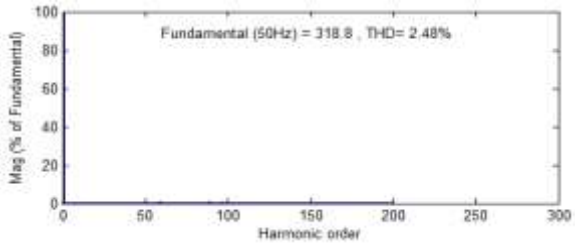


Figure 15. Voltage spectrum-33 level inverter

4.1. Experimental investigation for 7-level inverter and 15- level inverter

The experimental circuit for 7- level inverter is obtained using the circuit shown in Figure 3. The circuit uses 3 DC sources (V_{R1}, V_{R2}, V_{R3}), 6 unidirectional switching devices (S_{11}-S_{14}, S_{R1}, S_{R3}) and one bidirectional device (S_{R2}) to generate 7- level output voltage. The bi-directional switch is realized by connecting 2 nos of IRFP 460 MOSFETs in common source direction to allow current in both direction with single gate driver unit. The switching angles are calculated in off-line and form as LUTs. The experimental output voltage, inductive load current and voltage spectrum are acquired using Tektronix TPS 2024 DSO with same simulation specifications. The Figures 16 and 17 represents the experimental response obtained using the experimental prototype. The 7-level inverter produces an output voltage of 207V (rms) and THD of 12.5%. The experimental arrangement for 15-level inverter is configured using the circuit portrayed in Figure 2. with IRFP 460 MOSFETs and 6N137 opto-isolator gate driver circuits. The circuit uses 3 voltage sources (V_{L1}, V_{L2}, V_{L3}), 9 unidirectional switches and 2 bidirectional switches. The voltage values are arranged in the ratio of 1:3 (V_{L1}=40V and V_{L2}=V_{L3}= 120V) and RL load of 150Ω and 100mH respectively. Figures 18 and 19 represent output voltage, inductive load current and voltage spectrum which proved its capability to operate for higher voltage levels. The output has THD value of 6.30%. The control strategy shows reduction in THD retaining fundamental voltage while increasing the number of voltage levels.

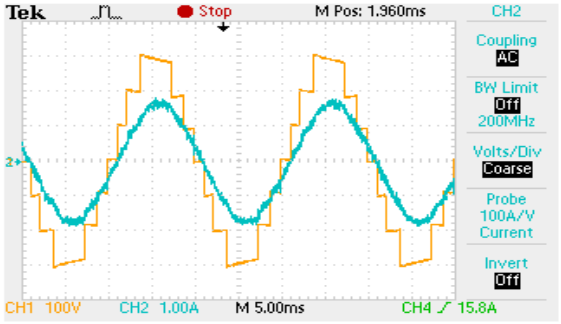


Figure 16. Output voltage and inductive load current for 7-level inverter

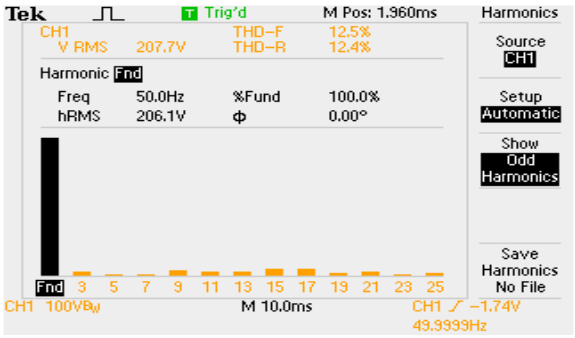


Figure 17. Voltage spectrum for 7-level inverter

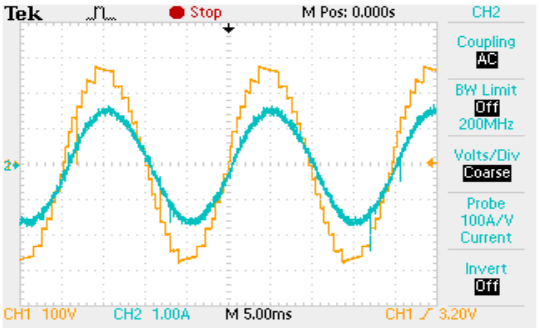


Figure 18. Output voltage and inductive load current for 15-level inverter

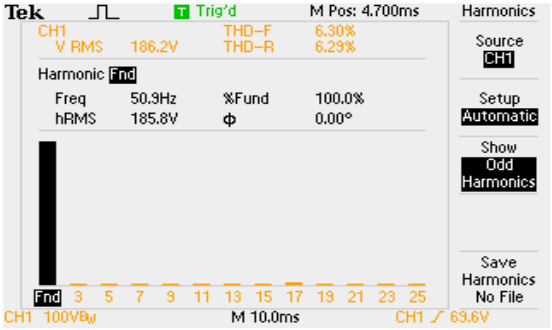


Figure 19. Voltage spectrum for 15-level inverter

5 CONCLUSION

In this paper, an attempt has been made to devise a new topology using tri-DC sources module with a view to reduce total number of power components and devices in current conduction path. The triple-DC source modules have two variants to operate in symmetrical and asymmetrical configurations to project more number of voltage levels. The feasibility of the proposed topology in terms of total component count, switches in current conduction path and total standing voltage are low compared with recent topologies. The topology is experimentally verified using a laboratory prototype to authenticate its merits in renewable energy applications. The formulation of fresh triple voltage source modules is to bring further structural enhancement in MLI topologies.

REFERENCES

[1] B. N. Rao, Y. Suresh, A. K. Panda, B. S. Naik, and V. Jammala, "Development of cascaded multilevel inverter based active power filter with reduced transformers," *in CPSS Transactions on Power Electronics and Applications*, vol. 5, no. 2, pp. 147-157, June 2020, doi: 10.24295/CPSSTPEA.2020.00013.

[2] T. Qanbari and B. Tousi, "Single-source three-phase multilevel inverter assembled by three-phase two-level inverter and two single-phase cascaded h-bridge inverters," *in IEEE Transactions on Power Electronics*, vol. 36, no. 5, pp. 5204-5212, May 2021, doi: 10.1109/TPEL.2020.3029870.

[3] M. Chen, Y. Yang, X. Liu, P. C. Loh, and F. Blaabjerg, "Single-source cascaded multilevel inverter with voltage-boost submodule and continuous input current for photovoltaic applications," in *IEEE Transactions on Power Electronics*, vol. 37, no. 1, pp. 955-970, Jan. 2022, doi: 10.1109/TPEL.2021.3098015.

[4] M. Mohsenzadeh, M. Rezanejad, and J. Adabi, "Marxiplier: An innovative marx-based single-source multilevel inverter with voltage multiplying capability," *in IEEE Transactions on Industrial Electronics*, vol. 69, no. 1, pp. 357-364, Jan. 2022, doi: 10.1109/TIE.2021.3051549.

[5] T. -T. Tran, M. -K. Nguyen, T. -D. Duong, Y. -C. Lim, and J. -H. Choi, "A switched-capacitor-based six-level inverter," in *IEEE Transactions on Power Electronics*, vol. 37, no. 4, pp. 4804-4816, April 2022, doi: 10.1109/TPEL.2021.3127440.

[6] E. Lee and K. Lee, "Performance improvement of cascaded H-bridge multilevel inverters with modified modulation scheme," *Journal of Power Electronics*, vol. 21, no. 3, pp. 541-552, 2021. DOI: 10.1007/s43236-020-00200-w.

[7] S. R. Khasim and C. Dhanamjayulu, "Design and implementation of asymmetrical multilevel inverter with reduced components and low voltage stress," in *IEEE Access*, vol. 10, pp. 3495-3511, 2022, doi: 10.1109/ACCESS.2022.3140354.

[8] M. A. Hosseinzadeh, M. Sarebanzadeh, E. Babaei, M. Rivera, and P. Wheeler, "A switched-DC source sub-module multilevel inverter topology for renewable energy source applications," in *IEEE Access*, vol. 9, pp. 135964-135982, 2021, doi: 10.1109/ACCESS.2021.3115660.
[9] M. Sarebanzadeh, M. A. Hosseinzadeh, C. Garcia, E. Babaei, S. Islam, and J. Rodriguez, "Reduced switch multilevel inverter topologies for renewable energy sources," in *IEEE Access*, vol. 9, pp. 120580-120595, 2021, doi: 10.1109/ACCESS.2021.3105832.
[10] R. Vasu, S. K. Chattopadhyay, and C. Chakraborty, "Three-phase trinary asymmetric multilevel inverter with single DC source and open-loop control," in *IEEE Open Journal of Industry Applications*, vol. 2, pp. 259-277, 2021, doi: 10.1109/OJIA.2021.3105605.
[11] A. Isazadeh, J. Adabi, M. Rezanejad, and M. E. Adabi, "Operation and control of a grid-connected asymmetrical cascaded multilevel inverter," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 2, pp. 1614-1623, April 2021, doi: 10.1109/JESTPE.2020.2991385.
[12] S. Yousofi-Darmian and S. M. Barakati, "A new asymmetric multilevel inverter with reduced number of components," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 4, pp. 4333-4342, Dec. 2020, doi: 10.1109/JESTPE.2019.2945757.
[13] X. Zhu, H. Wang, W. Zhang, H. Wang, X. Deng, and X. Yue, "A novel single-phase five-level transformer-less photovoltaic (PV) inverter," in *CES Transactions on Electrical Machines and Systems*, vol. 4, no. 4, pp. 329-338, Dec. 2020, doi: 10.30941/CESTEMS.2020.00040.
[14] B. N. Rao, Y. Suresh, A. K. Panda, B. S. Naik, and V. Jammala, "Development of cascaded multilevel inverter based active power filter with reduced transformers," in *CPSS Transactions on Power Electronics and Applications*, vol. 5, no. 2, pp. 147-157, June 2020, doi: 10.24295/CPSSTPEA.2020.00013.
[15] R. Vasu, S. K. Chattopadhyay, and C. Chakraborty, "Asymmetric cascaded H-Bridge multilevel inverter with single DC source per phase," in *IEEE Transactions on Industrial Electronics*, vol. 67, no. 7, pp. 5398-5409, July 2020, doi: 10.1109/TIE.2019.2934080.
[16] O. Lopez-Santos, C. A. Jacanamejoy-Jamioy, D. F. Salazar-D'Antonio, J. R. Corredor-Ramírez, G. Garcia, and L. Martinez-Salamero, "A single-phase transformer-based cascaded asymmetric multilevel inverter with balanced power distribution," in *IEEE Access*, vol. 7, pp. 98182-98196, 2019, doi: 10.1109/ACCESS.2019.2930230.
[17] A. Sheir, M. Z. Youssef, and M. Orabi, "A novel bidirectional T-Type multilevel inverter for electric vehicle applications," in *IEEE Transactions on Power Electronics*, vol. 34, no. 7, pp. 6648-6658, July 2019, doi: 10.1109/TPEL.2018.2871624.
[18] C. Phanikumar, J. Roy, and V. Agarwal, "A hybrid nine-level, 1-φ grid connected multilevel inverter with low switch count and innovative voltage regulation techniques across auxiliary capacitor," in *IEEE Transactions on Power Electronics*, vol. 34, no. 3, pp. 2159-2170, March 2019, doi: 10.1109/TPEL.2018.2846628.
[19] S. S. Lee, M. Sidorov, N. R. N. Idris, and Y. E. Heng, "A symmetrical cascaded compact-module multilevel inverter (CCM-MLI) with pulsewidth modulation," in *IEEE Transactions on Industrial Electronics*, vol. 65, no. 6, pp. 4631-4639, June 2018, doi: 10.1109/TIE.2017.2772209.
[20] L. Wang, Q. H. Wu, and W. Tang, "Novel cascaded switched-diode multilevel inverter for renewable energy integration," in *IEEE Transactions on Energy Conversion*, vol. 32, no. 4, pp. 1574-1582, Dec. 2017, doi: 10.1109/TEC.2017.2710352.
[21] R. Samanbakhsh, F. M. Ibanez, P. Koohi and F. Martin, "A New Asymmetric Cascaded Multilevel Converter Topology With Reduced Voltage Stress and Number of Switches," *in IEEE Access*, vol. 9, pp. 92276-92287, 2021, doi: 10.1109/ACCESS.2021.3092691.
[22] M. D. Siddique, S. Mekhilef, A. Sarwar, A. Alam, and N. M. Shah, "Dual asymmetrical dc voltage source based switched capacitor boost multilevel inverter topology," *IET Power Electronics*, vol. 13, no. 7, p. 1481-1486, 2020, doi: 10.1049/iet-pel.2019.1567, https://digital-library.theiet.org/content/journals/10.1049/iet-pel.2019.1567.
[23] M. N. Hamidi, D. Ishak, M. A. A. M. Zainuri, and C. A. Ooi, "Multilevel inverter with improved basic unit structure for symmetric and asymmetric source configuration," *IET Power Electronics*, vol. 13, no. 7, p. 1445-1455, 2020, doi: 10.1049/iet-pel.2019.0916, https://digital-library.theiet.org/content/journals/10.1049/iet-pel.2019.0916.
[24] S. S. Kumar, M. W. Iruthayarajan, and T. Sivakumar, "Evolutionary algorithm based selective harmonic elimination for three-phase cascaded H-bridge multilevel inverters with optimized input sources," *Journal of Power Electronics*, vol. 20, no. 5, pp. 1172-1183, 2020, doi: 10.1007/s43236-020-00112-9.
[25] K. Pham and N. Nguyen, "Pulse-width modulation strategy for common mode voltage elimination with reduced common mode voltage spikes in multilevel inverters with extension to over-modulation mode," *Journal of Power Electronics*, vol. 19, no. 3, pp. 727-743, 2019, doi: 10.6113/JPE.2019.19.3.727.

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