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Impact of high-*k* insulators on electrical properties of junctionless double gate strained transistor

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ABSTRACT

High-*k* dielectric insulators are required to reduce leakage and increase transistor performance. They are able to impact the mobility of carriers in transistors positively, leading to better device performance in advanced transistor architecture. Nevertheless, an in-depth analysis of how high-*k* dielectric insulators influence transistor characteristics must be carried out to determine their suitability. The objective of this study is to investigate the impact of high-*k* insulators towards electrical properties of junctionless double gate strained transistor. The simulation works is done using process/device simulator Silvaco Athena/Atlas. Based on the retrieved results, the magnitude of I_{ON}, on-off ratio, g_m, and C_{int} for TiO_2-based device are approximately 63%, 99%, 62%, and 89% respectively higher than the lowest permittivity material-based device. The TiO_2-based device also exhibits the lowest magnitude in I_{OFF} and SS compared to others. However, a significant degradation in f_T magnitude have been observed for TiO_2-based device significantly due to its large capacitances.

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1. INTRODUCTION

During the preceding decade, the architecture of transistors depends crucially on junction configuration. The prominence of junctions is merely for halting and enabling the flow of current as potential is exerted [1], [2]. In most cases, these p-n junctions are created by placing two semiconductor regions of opposing polarity next to one another. The reduced thermal budget procedure provides vital to increase implant gradient junction without harming transistor functionality [3]-[5]. However, the junctionless design offers an alternate way of transistor construction that avoids the aforementioned complex production procedure. On October 22, 1925, Julius Edgar Lilienfield, an Austrian-Hungarian physicist, patented the first junctionless transistor [6]. When gate bias depletes the transistor's thin semiconductor layer, it serves as a resistor, enabling carriers to flow through it [7], [8]. An ultrathin silicon (Si) body is used to fabricate a junctionless transistor, allowing the majority carriers in the channel to be totally drained when the device is in a state of active use [9]-[11]. It also needs to be extensively implanted with dopants to facilitate sufficient flow of current to switch the transistor on. Recent study by Ajay [12] has mentioned that junctionless FinFET contributes significant

improvement in drain current and RF characteristics compared to silicon-on-insulator (SOI) type. Shukla *et al.* [13] proposed a novel design for a planar junctionless field-effect transistor (FET) aimed at highly sensitive and multiplexed immunosensors for peptidomics and proteomics. This design is considered advantageous for immunosensing platforms due to its simplicity, responsiveness to chemical stimuli, and long-term operational stability. The transistor demonstrated a significant current sensitivity in relation to pH, calculated to be 38.9 ± 2.1 nA/pH. It also showed a wide range of current responses, from 50 to 400 nA. This range suggests the capability of the device to operate between nearly complete depletion and full conduction of the channel.

Oproglidis *et al.* [7] highlighted that in the p-type triple-gate junctionless transistors, the high series resistance had a more pronounced effect on the dgm/dVg behavior than the short-channel effects. This finding is significant as it underlines the importance of considering series resistance in the design and analysis of such transistors. Shokri and Amirmazlaghani [14] designed and simulated an inverter logic gate based on field-effect bipolar junction transistor. They presented both static and dynamic assessment criteria for this logic gate and compared these characteristics with other technologies. The study calculated several key performance metrics for the designed device. The maximum frequency was found to be 0.25 THz, the power-delay product (PDP) was 38×10-17 J, the dynamic power was measured at 94 μW, and the ring frequency was determined to be 85 GHz. These metrics indicate a high level of performance for Field-Effect Bipolar Junction Transistor in digital circuit applications. Short channel effects (SCE), impact ionizations, and gate leakage have all been raised by aggressive transistor scaling [15]-[17]. To address these obstacles, channel engineering approaches have been widely proposed [18], [19]. Technology based on high-k/metal-gate (HKMG) stacks is one of the most frequently used methods for leakage mitigation [20]. Strained technology also could help alleviating the scalability limit of transistors [21], [22]. Silicon-germanium (SiGe) on silicon film has been proven to significantly improve transistor analogue and RF characteristics while retaining CMOS compliance [23]-[25]. The attachment of HKMG to the stressed channel potentially optimize carriers transportation while diminishing power leakage [26], [27]. Ghosh and Nelapati [28] demonstrated that the steep on-off switching and the sub-threshold slope profile of the high-*k* stacked dual gate junctionless MOSFET are heavily dependent on temperature variations. It confirmed that the transistor electrostatics improve at lower temperatures.

There has been an explosion in the need for low-cost, high-performance RF solutions in recent years, and high-*k* insulators have an important role to play in transistor performance. Work function engineering in CMOS technology necessitates the use of HKMG materials from a variety of types. The appropriate selection of HKMG properties is very important in gaining better analogue and RF performance from a transistor [20]. To this objective, the authors conduct a thorough analysis of the influence of high-*k* insulators on the analogue and RF performance of junctionless double gate strained transistor in the present work. The following is the structure of the work provided in this paper: Silvaco Athena and Atlas modules are used to simulate the device structure, which is explained in detail in section 2. A thorough investigation of the effect of high-*k* insulators on the analogue and RF performance of the junctionless double gate strained transistor is presented in section 3. Section 4 concludes with a brief discussion of the results and directions for further research.

2. METHOD

The simulation works for this experimental study are divided into two parts: process simulation via Athena Silvaco and Device simulation via Atlas Silvaco. The primary purpose of this simulation works is to investigate the impact of different materials of high-*k* dielectric towards the electrical properties of n-channel junctionless double-gate strained transistor. The selected electrical properties include on-current (I_{ON}), off-current (I_{OFF}), on-off ratio, subthreshold swing (SS), transconductance (g_m), intrinsic capacitances (C_{int}) and unity-gain frequency (f_t). The following subsections describes the process and device simulation for the respective study. As mentioned earlier, the process simulation for the device was conducted via Athena Silvaco TCAD. Athena module offers numerous facilities for virtual platform that emulates costly real industrial fabrication.

Figure 1 show the process simulation flow for the device. The process simulation was initiated with the deposition of the main substrate which was SiGe with 8nm of thickness. The ultrathin Si layer (1 nm) was then deposited on the top of SiGe body for making the Si lattice tensely stretched as the SiGe atoms attempting to form alignment with the Si atoms [29]. The strained channel was highly doped with $1x10^{17}cm^{-3}$ of arsenic dopant to form n^+ region. The gate material was tungsten silicide (WSi_x) mainly opted due to its workfunction (WF) tunability [3], [30]. Normally, WSi_x gate was paired with high-*k* dielectric materials in order to prevent the insulator/gate boundaries from being defected due to voltage pinning. Selecting a suitable high-*k* dielectric as the insulator is very crucial in getting the best electrical properties of the device. In this simulation works, four different high-*k* dielectric materials knownly as silicon nitride (Si_3N_4), aluminum oxide (Al_2O_3), hafium dioxide (HfO_2) and titanium dioxide (TiO_2) were extensively explored. Next, the source/drain (S/D) regions of the device were doped with the same dopant type as the channel region but with much lower concentration

($1x10^{13}$ cm^{-3}). Thus, the junctionless formation (n-n^+-n) was eventually formed beneath the HKMG structure. The separate contacts for source, drain and gate electrode were then fomed by sputtering and etching the aluminum layer. Lastly, the completed structure of the device was reflected in both x and y directions. The contour mode of the completed device is shown in Figure 2 in which the channel length (L_{ch}) was scaled at 8nm. The device simulation was performed via Atlas Silvaco TCAD.

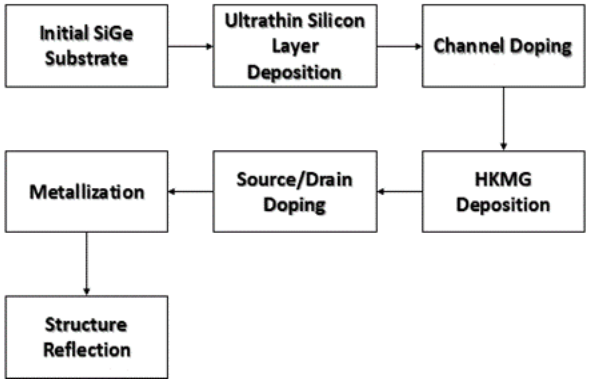

Figure 1. Process simulation flow

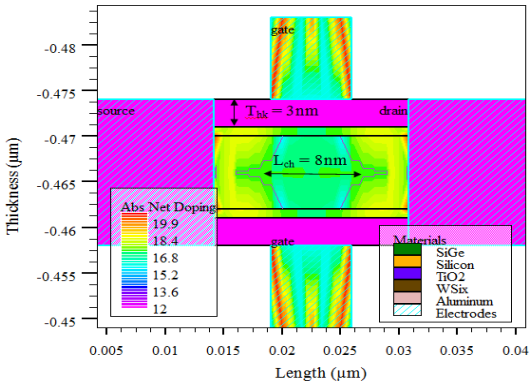

Figure 2. Device layout in contour mode

The Atlas module is a physically based 2D/3D device simulator that capable of predicting the electrical properties of semiconductor devices. It basically provides a comprehensive insight of internal physical structure associated with the device operation. Based on the output structure file generated from the previous Athena simulation, the I_{ds}-V_{gs} transfer characteristics was plotted. The device was simulated in accordance to the bias conditons and the I_{ds}-V_{gs} curve was plotted in both linear and log mode. The device simulation involved numerical models like drift diffusion (DD), shockley-read-hall (SRH) recombination and Lombardi CVT. The device simulation was carried out by utilizing different high-*k* dielectric materials (i.e. Si_3N_4, Al_2O_3, HfO_2 and TiO_2) as the insulator. The equivalent oxide thickness (EOT) of the insulator are totally depended on the thickness of the high-*k* materials (T_{hk}) and the permittivity of the high-*k* dielectrics (ε_{hk}) as relationally described as [31], [32]:

$$EOT = \frac{\varepsilon_{SiO_2}}{\varepsilon_{hk}} T_{hk} \quad (1)$$

where ε_{SiO2} is the permittivity of silicon dioxide (SiO_2). The high-*k* dielectric permittivity for each material were defined in the Atlas simulator as listed in Table 1. The overlay I_{ds}-V_{gs} transfer characteristics were plotted based on the respective types of high-*k* dielectric. The investigated electrical properties for different high-*k* materials can be extracted and calculated from the generated I_{ds}-V_{gs} curves.

Table 1. Permittivity of high-*k* dielectric materials

Material	Permittivity (ε_{hk})
Si_3N_4	7
Al_2O_3	9
HfO_2	25
TiO_2	85

3. RESULTS AND DISCUSSION

This section will comprehensively describe the impact of different high-*k* materials towards I_{ON}, I_{OFF}, on-off ratio, SS, g_m, $C_{int,}$ and f_t of the device. The I_{ds}-V_{gs} curve for different high-*k* dielectrics were generated by shifting the gate-to-source voltage (V_{gs}) from 0 V to 1 V at a constant drain-to-source (V_{ds}) of 0.5 V. For a fairly comparative analysis, the threshold voltage (V_{TH}) magnitudes of the device for different high-*k* dielectrics were tuned and fixed at 0.2 V. The overlay I_{ds}-V_{gs} curve was plotted for all types of high-*k* dielectric materials under this study as depicted in Figure 3. It is found that the TiO_2 material exhibits the highest I_{ON} at maximum V_{gs} compared to other high-*k* materials. The I_{ds} initiates to accelerate after hitting threshold limit, then its magnitude peaks higher than the other high-*k* materials as the V_{gs} is shifted towards the maximum magnitude.

The prime reason behinds this occurrence is the high permittivity of TiO_2 as an insulator that offers a very effective coupling gate fringing in channel region. The magnitude of the electric field in the channel region significantly increases as higher permittivity of high-*k* dielectric is applied. The significance of high electric field lead to the formation of inversion layer which subsequently increase the channel volume. The magnitudes of I_{ON} for the device with different high-*k* materials are summarized in Figure 4. It is shown that the device with TiO_2 based insulator demonstrate a tremendous improvement in I_{ON} magnitude by approximately 63% compared to the device with Si_3N_4 based insulator.

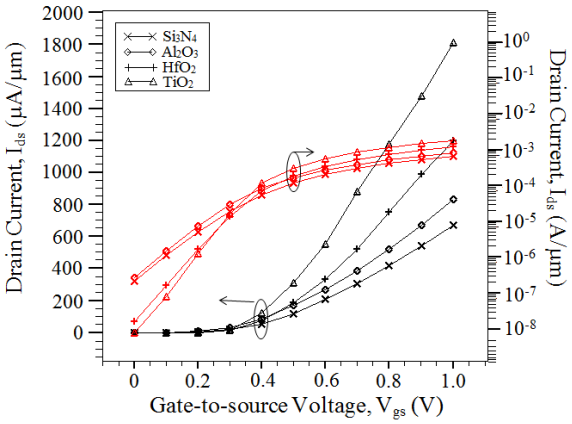

Figure 3. Overlay plot of I_{ds}-V_{gs} curves in linear and log scales for different high-*k* dielectrics

Figure 5 shows the bar graph indicating the extracted I_{OFF} magnitudes for the device with different high-*k* materials. It is shown that the devices with much higher magnitude of dielectric permittivity such as HfO_2 and TiO_2 effectively suppress the drain-to-source current at V_{gs} = 0 V (off-state). It is predominantly due to the conduction band is much higher in off-state condition for lower high-*k* permittivity. However, the I_{OFF} magnitude also depends on the effective channel length in which larger leakage is often demonstrated by the device with lower effective channel length. The I_{OFF} characteristic is also regarded as an important figure of merit to determine the power consumption of the transistor normally measured by the magnitude of on-off ratio. The higher on-off ratio implies the device has better power consumption in which lesser V_{gs} is required for the device to reach saturation mode. The magnitude of on-off ratio for the device can be measured as follows:

$$On-off\ ratio = \frac{I_{ON}(I_{ds}\ when\ V_G=1V)}{I_{Off}(I_{ds}\ when\ V_G=0V)} \quad (2)$$

Figure 6 shows the bar graph of on-off ratio for different high-*k* materials. It is observed that the on-off ratio is quite low for the device with lower dielectric permittivity like Si_3N_4 and Al_2O_3 materials. However, the on-off ratio increases as higher dielectric permittivity materials such as HfO_2 and TiO_2 are employed. The device with TiO_2 based insulator exhibits approximately 65% higher on-off ratio compared to the device with TiO_2 based insulator mainly due to its higher dielectric permittivity. Although the TiO_2-based device shows dramatic improvement in I_{ON}, I_{OFF} and on-off ratio, yet it experiences fabrication obstacles and large capacitances [33]-[37]. In the subthreshold region, the I_{ds} behavior emulates the exponentially lowering current in a basic forward biased diode. Hence, it is essential to determine how much the V_{gs} required to increase one decade of I_{ds}. This can be measured by taking the inverse magnitude of the linear slope of the subthreshold (log mode) I_{ds}-V_{gs} curve mathematically described as:

$$SS = \left[\frac{d(log_{10}\, I_{ds})}{dV_{gs}}\right]^{-1} \quad (3)$$

A transistor with steeper/lower subthreshold swing (SS) implies a faster switching transition between on-state (high I_{ds}) and off-state (low I_{ds}) or vice versa. Figure 7 shows the bar graph of the SS magnitude for different high-*k* materials. It is observed that the device with TiO_2 based insulator exhibits approximately 49% steeper SS compared to the device with the lowest dielectric permittivity.

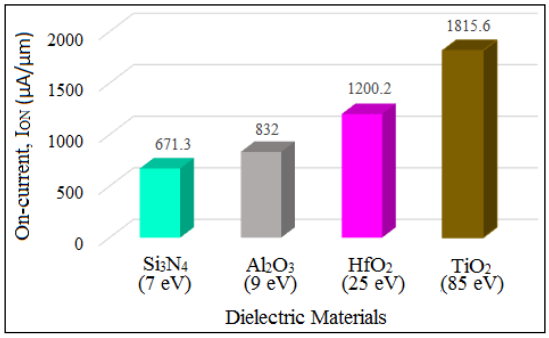

Figure 4. Bar graph of I_{ON} for different high-*k* materials

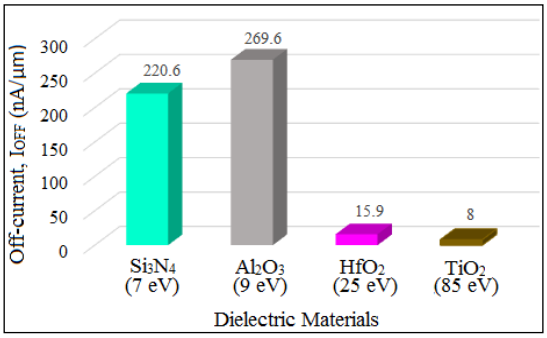

Figure 5. Bar graph of I_{OFF} for different high-*k* materials

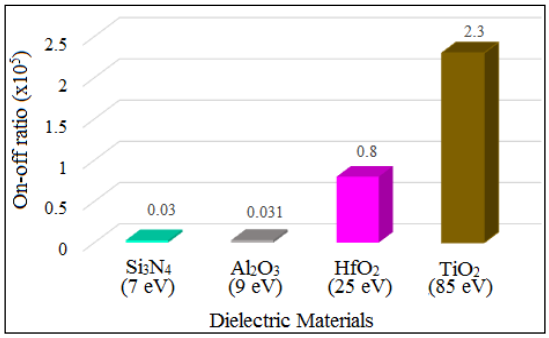

Figure 6. Bar graph of on-off ratio for different high-*k* materials

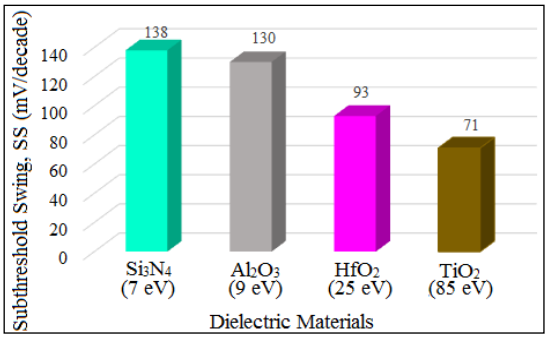

Figure 7. Bar graph of SS for different high-*k* materials

This shows that the SS magnitude becomes steeper as higher permittivity dielectric is employed. This is physically due to the increase of effective channel length that consequently increase the total intrinsic capacitances. Thus, the I_{ds} in subthreshold region is improved and the device can be turned-on with minimum changes in gate bias. The device with steeper SS also can be turned-off rapidly as the amount of V_{gs} required to decrease the I_{ds} magnitude by one decade are reduced. A decade represents 10 times increase or decrease of the I_{ds} of the device. Another important parameter that should be considered in transistor's design is transconductance (g_m). The magnitude of g_m is very crucial to measure the transistor's efficiency of converting a voltage to a current. Thus, the magnitude of g_m is used to evaluate the analogue performance can be computed as:

$$g_{\mathrm{m}} = \frac{\partial I_{ds}}{\partial V_{gs}} \tag{4}$$

Figure 8 shows an overlay of the tranconductance (g_m) vs. V_{gs} transfer characteristic at a constant V_{ds}=0.5 V for the device with different high-*k* dielectric materials. It is observed that the magnitude of g_m is directly proportional with the magnitude of dielectric permittivity in which the g_m magnitude increases as the material with higher dielectric permittivity is employed. The TiO_2 based device exhibits approximately 62% higher g_m magnitude at maximum V_{gs} compared to the Si_3N_4-based device. High permittivity of TiO_2 material triggers high electron tunneling with minimal leakage for higher I_{ds} which obviously resulting in higher g_m magnitude. Thus, high channel volume and g_m of the TiO_2-based device provides better transport efficiency which is very desirable for analog applications. For the purpose of RF analysis, 1 MHz of AC frequency (f) has been supplied to the gate terminal as the V_{gs} is biased from 0 V to 1 V. This is done in order to extract the magnitude of intrinsic capacitances which are very important for calculating the unity-gain frequency (f_t) of the device. The intrinsic capacitances (C_{int}) is the sum of the gate-to-source capacitance (C_{gs}) and gate-to-drain capacitance (C_{gd}) which can be calculated by:

$$C_{\mathrm{int}} = C_{\mathrm{gs}} + C_{\mathrm{gd}} \tag{5}$$

The magnitudes for both C_{gs} and C_{gd} are heavily relies on the device geometry and the material types. Figure 9 shows an overlay plot of the C_{int}-V_{gs} transfer characteristic at a constant V_{ds}=0.5 V for different high-*k* dielectric materials. From the plot, it is clearly shown that the TiO_2-based device exhibits larger C_{int} magnitude compared to the others. The C_{int} magnitude demonstrated by TiO_2-based device instigate to peak after reaching 0.8V of V_{gs} and it is continually increasing as the gate bias is further increased. This indicates that the high permittivity dielectric like TiO_2 material does cause a large variation on the C_{int} magnitude as the V_{gs} approaching its maximum value. The rest of the materials like HfO_2, Al_2O_3, and Si_3N_4 do not cause much significant variation in C_{int} magnitude of the device as the V_{gs} is shifted to higher positive magnitude. The TiO_2-based device demonstrates approximately 73% higher C_{int} magnitude than HfO_2-based device.

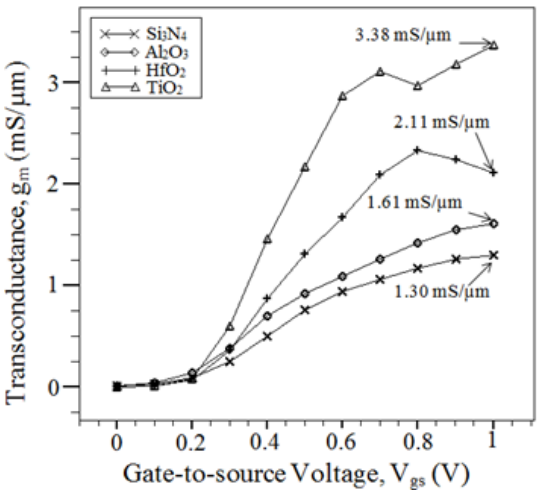

Figure 8. Overlay plot of g_m-V_{gs} curve in linear mode for different high-*k* dielectrics

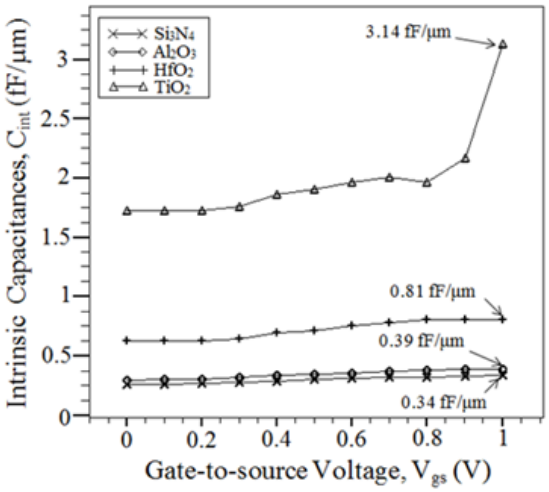

Figure 9. Overlay plot of C_{int}-V_{gs} curve in linear mode for different high-*k* dielectrics

High C_{int} magnitude is pretty much desirable for transistors, but without deteriorating the electric field. Thus, selecting an appropriate high-*k* material without having to reduce its thickness is very crucial in order to maintain tolerable electrical performance especially at nano-scale dimension. The magnitude of C_{int} is then used to measure f_t of the device. The f_t is very important figure of merit used to measure the device performance as an amplifier. It can be derived from the high frequency model the device. The f_T is defined as a frequency at which magnitude of the short circuit current gain of the common-source configuration becomes unity. It is used to determine how fast the transistor can operate in high frequency. Figure 10 depicts the high-frequency model of the device.

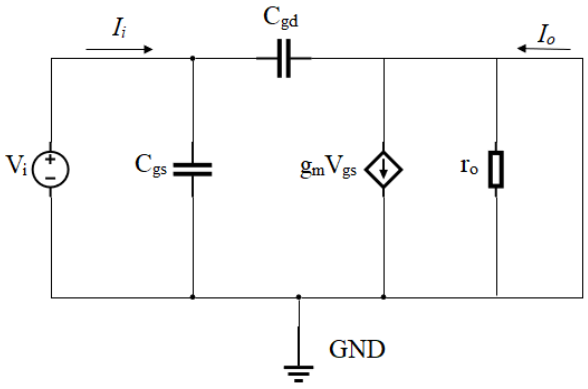

Figure 10. Small-signal high frequency model

Since the value of r_o is relatively small, its effects on the high frequency model can be totally neglected. Based on the model, the current gain (I_o/I_i) of the device can be derived as:

$$\frac{I_o}{I_i} = \frac{g_m}{j\omega(C_{gd}+C_{gs})} \quad (6)$$

Thus, as the current gain is becoming unity, the (7) can be written as:

$$\omega = \frac{g_m}{C_{gd}+C_{gs}} for \left|\frac{I_o}{I_i}\right| \quad (7)$$

Since $\omega=2\pi f$, the unity-gain frequency (f_T) can be rewritten as:

$$f_T = \frac{g_m}{2\pi(C_{gs}+C_{gd})} \approx \frac{g_m}{2\pi C_{int}} \quad (8)$$

Figure 11 shows an overlay f_T-V_{gs} transfer characteristic at a constant V_{ds}=0.5 V for the device with different high-*k* dielectric materials. The magnitude of f_t becomes lower as a higher permittivity dielectric material is employed as the gate insulator. The f_T magnitude of TiO_2-based device has been tremendously deteriorated by 74% and 72% compared to Al_2O_3-based device and Si_3N_4-based device respectively. This is reasonably due to the larger C_{int} magnitude of the TiO_2-based device that dominantly governs the f_T magnitude over the g_m magnitude. Thus, higher g_m magnitude exhibited by the TiO_2-based device do not contribute any significant increase on f_T magnitude. High f_T magnitude is very desirable for designing RF high frequency amplifiers, however, other device characteristics such as I_{ON}, I_{OFF} and SS should be also considered for more balanced performance. Hence, the types of high-*k* material need to be properly selected based on their impact on electrostatic, analog and RF performance. Table 2 summarizes all the investigated electrical properties for different high-*k* dielectric materials.

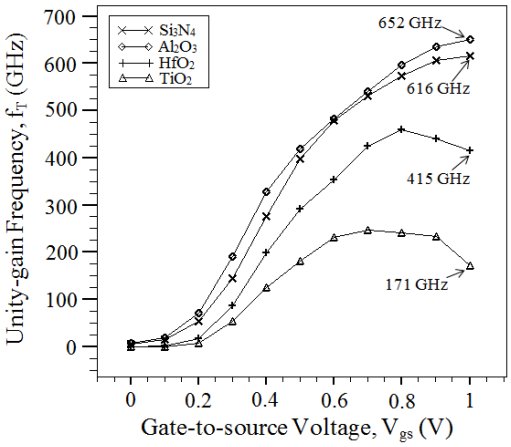

Figure 11. Overlay plot of f_T-V_{gs} curve in linear mode for different high-*k* dielectrics

Table 2. Electrical properties for different high-*k* dielectric materials

Materials	Units	Si_3N_4	Al_2O_3	HfO_2	TiO_2
I_{ON}	µA/µm	671.3	832	1200.2	1815.6
I_{OFF}	nA/µm	220.6	269.6	15.9	8
On-off ratio	x10^5	0.03	0.031	0.8	2.3
SS	mV/decade	138	130	93	71
g_m	mS/µm	1.3	1.61	2.11	3.38
C_{int}	fF/µm	0.34	0.39	0.81	3.14
f_T	GHz	616	652	415	171

Table 3 displays our work's comparison with other junctionless transistor types. Our research exhibits superior on-current and satisfactory unity-gain frequency compared to most junctionless transistor types. Additionally, we focus on reducing the physical gate length to 6nm while maintaining acceptable transistor

performance. The utilization of high-*k* gate dielectrics with strain technology is among several approaches aimed at facilitating the ongoing miniaturization of microelectronic components, a concept akin to extending Moore's Law. Transitioning to novel transistor technologies poses challenges, and supply timelines for nanosheet transistors differ among foundries.

Table 3. Performances benchmark with other junctionless transistor types

Junctionless transistor type	Year published	Gate length (nm)	On-current (μA/μm)	Transconductance (mS/μm)	Unity-gain frequnecy (GHz)
Gate underlapped double gate [38]	2019	12	250	0.39	369
Dual material double gate [39]	2020	20	1500	4	795
Double gate material floating gate [40]	2021	20	123.1	1.23	100
Multi-fin SOI [41]	2021	18	59.7	0.9	450
Gate all around [42]	2021	30	10	4	546.54
Surrounded gate [43]	2022	30	226.8	0.23	536
Gate all around [44]	2022	30	44	0.069	44
Cylindrical gate-all-around [45]	2023	30	20	n/a	n/a
Hetero-structure corner space high-k [46]	2024	40	330	n/a	n/a
Double gate strained with HfO_2 high-*k*	Current work	6	1200.2	2.11	415

Besides the variability in high-*k* materials causing random parameter fluctuations in transistor operation, it is imperative to examine the effects of design parameters. These consist of implant concentration, physical thickness, and gate workfunction, necessitating further investigation. In addition, the application of optimization approaches [17], [27], [47]-[49] could be deployed by considering the types of high-*k* material along with other geometrical and process parameters for optimal junctionless double gate strained transistor.

4. CONCLUSION

The impact of different high-*k* materials on the junctionless double gate strained transistor upon I_{ON}), I_{OFF}, on-off ratio, SS, g_m, $C_{int,}$ and f_t have been comprehensively investigated using 2D simulation tools. Based on the results, the magnitude of I_{ON}, on-off ratio, g_m, and C_{int} for TiO_2-based device are approximately 63%, 99%, 62%, and 89% respectively higher than the lowest permittivity material-based device. This concludes that the permittivity level of high-*k* materials is directly proportional with the magnitude of I_{ON}, on-off ratio, g_m, and C_{int} of the device. In contrast, the SS magnitude of the device is inversely proportional with the permittivity level of high-*k* materials in which its magnitude is lowering as higher permittivity material is applied as gate insulator. The TiO_2-based device also demonstrates approximately 50% lower I_{OFF} than the device with HfO_2-based insulator mainly due to better suppression of leakage during off-state condition. Lastly, the TiO_2-based device demonstrates the lowest f_T mainly due to its large intrinsic capacitances that dominantly governs the f_T magnitude over the drain current.

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