Indonesian Journal of Electrical Engineering and Computer Science
Vol. 34, No. 3, June 2024, pp. 1879~1892
ISSN: 2502-4752, DOI: 10.11591/ijeecs.v34.i3.pp1879-1892

Random access memory page caching: a strategy for enhancing shared virtual memory multicomputer systems performance

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Article Info

Article history:

Received Nov 19, 2023
Revised Feb 13, 2024
Accepted Mar 4, 2024

Keywords:

Boolean
Combinatorial space
Data caching
Random access memory
Systems with shared virtual memory
Working set

ABSTRACT

This study examines a modified approach to optimizing the performance of support vector machine (SVM)-type multicomputer systems through a distinct type of caching method that allocates space in the random access memory (RAM) of a computing node for caching pages. The article extensively describes research on enhancing the performance of the SVM system through memory page caching in RAM at the hardware level by implementing the SVM system based on field-programmable gate arrays (FPGA). A systematic comparative evaluation highlights a discernible enhancement in system performance relative to systems not equipped with the revised caching algorithm. These findings could prove instrumental for subsequent studies focused on optimizing the performance of SVM systems, providing empirical data to inform future investigations and potential applications in multicomputer system performance enhancement.

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1. INTRODUCTION

Recently, with an increase in the volume of data and the complexity of algorithms, computational performance has become one of the main criteria for the effectiveness of computing systems with virtual memory, for example the support vector machine (SVM) type [1], [2]. Virtual memory, a widely used memory management concept, extends beyond the conventional memory structure found in desktop PCs and multicomputer systems, including shared virtual memory (SVM) systems. Additionally, it acts as a bridge between the CPU and GPU, as illustrated in the compute unified device architecture (CUDA) [3].

Currently, one of the main areas of research in the field of improving the performance of SVM-type systems is restructuring [4]-[15] and refactoring [16]-[24] of programs. But there are other areas of research in this area, for example [25], [26]. Another approach using the cluster concept, based on Zhuravlev's approach to classification [27]-[30], was proposed in [31]-[34] and is associated with the construction of a special algebra over cluster algorithms. Then the main problem reduces to the solvability of the special operator equation. Our approach is based and developed from another idea [33] and also comes from the field of classical discrete extremal problems. Here, we can say, the approach of extremal problems is a very advantageous tool for optimizing or improving the behavior of systems [35]-[40] and is a natural step in the development of research.

It is also worth noting that one of the ways to increase performance is data caching. However, this method has both advantages and disadvantages. The advantages of this method include the speed of operation, and the disadvantages are the small cache size. Due to the development of technology in recent years, the speed of accessing RAM has become as close as possible to the speed of accessing the cache, and at the same time, the size of the memory in RAM is an order of magnitude larger. If earlier, due to the low speed of RAM, it was not effective to use it as a cache and RAM was used mainly for temporary data storage, then with an increase in the speed of processor access to RAM, it became possible to allocate additional space in RAM for caching and, as a result, the caching method has a new stage of development.

It is worth noting that in distributed virtual memory (SVM) systems, when data is accessed over the network, caching can be implemented at the node level, which can significantly speed up data access and improve overall system performance. However, to cache any data, storage space is required, and this article proposes using part of the RAM to cache virtual memory pages. Directly comparing the results of restructuring and refactoring with caching is quite difficult because these are completely different approaches, each of them has its own pros and cons, but caching is the main way to improve the performance of any system. Caching works no matter how well the program is made and can be used in conjunction with other approaches to improve performance. The advantage of caching in RAM on computing nodes is also influenced by the fact that RAM performance has been actively increasing in recent years, for example [41]-[44].

Currently, there is a wide range of caching algorithms, and this article presents research based on the working set strategy set), which consists of caching only those pages that are actively used by the application at a given time. This strategy can significantly reduce the amount of cached data and increase caching efficiency. Research results on the working set strategy for memory management were described in [45].

The main goal and distinctive feature of this work is to study the possibilities of using page caching in the RAM of computing nodes in multicomputer systems such as SVM using a working set strategy based on the mathematical model described in [46] and improved by us in [47], in order to increase the performance of this system as a whole, both in software and and at hardware levels. Further in this paper, briefly proposes a caching model, which will be discussed in section 2. Analysis and experimental results are depicted in section 3. Finally, section 4 draws the conclusions.

2. MATERIALS AND METHODS

Consider a program composed of n interacting blocks, denoted as $b_1, b_2, \dots, b_n$ (abbreviated 1,2,… ,n), distributed across p pages of virtual memory, labeled as $S_{g_1}, S_{g_2}, \dots, S_{g_p}$, which we'll simplify as $S_1, S_2, \dots, S_p$. The execution of this code can lead to issues stemming from a high occurrence of page faults, significantly impacting system performance. These issues arise from unclear code structure, resulting in diminished performance for both the code itself and the overall system. This undesirable behavior may also be attributed to code segments written by different authors belonging to different programming groups and created at various points in time. In one scenario, any reference made during code execution from the resident set must point to only one block among $\{b_1, b_2, \dots, b_n\}$, while in another scenario, this constraint may not be obligatory.

Let us denote $v_r$by the length of the rth page $r = 1,2, \dots, p$and $l_i$by the length of the block $i = 1,2, \dots, n$. This notation suggests that the system accommodates multi-dimensional page sizes. In this context, blocks denote various components of the code, such as subroutines, linear code segments, independent interacting programs, and application data blocks. Block distribution$b_1, b_2, \dots, b_n$ between pages $S_1, S_2, \dots, S_p$is predetermined and represented through a logical matrix $x = (x_{ri})_{p\times n}$, where the element is $x_{ri} = 1$if the block $i$belongs to the page $r$and $x_{ri} = 0$otherwise. Let us denote all such matrices by X. In Figure 1, blocks are displayed on the corresponding pages in the form of vertical columns with their numbers and lengths, for example, a page S_{g_1}contains blocks$b_{j_1 1}, b_{j_2 1}, \dots, b_{j_{\lambda_1} 1}$ with lengths$l_{j_1 1}, l_{j_2 1}, \dots, l_{j_{\lambda_1} 1}$ accordingly.

Recall that some variants of the problem of moving program blocks (code) across pages$S_1, S_2, \dots, S_p$ with the goal of minimizing the cost functional are known as NP -hard problems. The problem in our case has its own specifics and does not yet have a final solution, which is already quite enough for research. Therefore, the main impetus for research remains the fundamental aspect of the problem, which intensifies efforts and can become the main motivation for research.

Returning to our problem, it's important to remember that the random data, represented by D={θ}, as well as the permutation strategy, have an impact on the functional value. Suppose that after running the code with a specific value θ∈D, a reference line of blocks (pages) corresponding to it, denoted by θ, is available. In this paper, the permutation strategy selected is the working set (WS) strategy. The resident set of R pages in RAM at any given moment during program operation aligns with the working set of pages at that

moment, denoted by the commonly used notation W(k,t) [4]. We regard the block analogy of the working set as the control state (cs) of the code (program), utilizing q cs as the appropriate notation. In Figure 1 the control state q there isq=(i_1,i_2,…,i_(m(q))), wherei_j the number of the block (j=1,2,…,m(q)) that belongs to q, and any of them are marked as. In Figure 1 for some moment t, cs q=(i_1,i_5,i_6,i_7, 〖i_10,i_15,i〗 _(m(q))) marked with the symbol⊗ and means any block (or its number) that does not belong to, q, a belongs to the corresponding page of the resident setR and is present in RAM. In Figure 1 as a resident set R shows the working set R(q,x) that is generated by cs q and matrix. Of course, link to cs q to the block that is marked as ⊗ or ∘ in Figure 1, does not give a page fault, unlike references to blocks that are outside R(q,x). In any case, you need to correctly determine whether a page fault occurs or not.

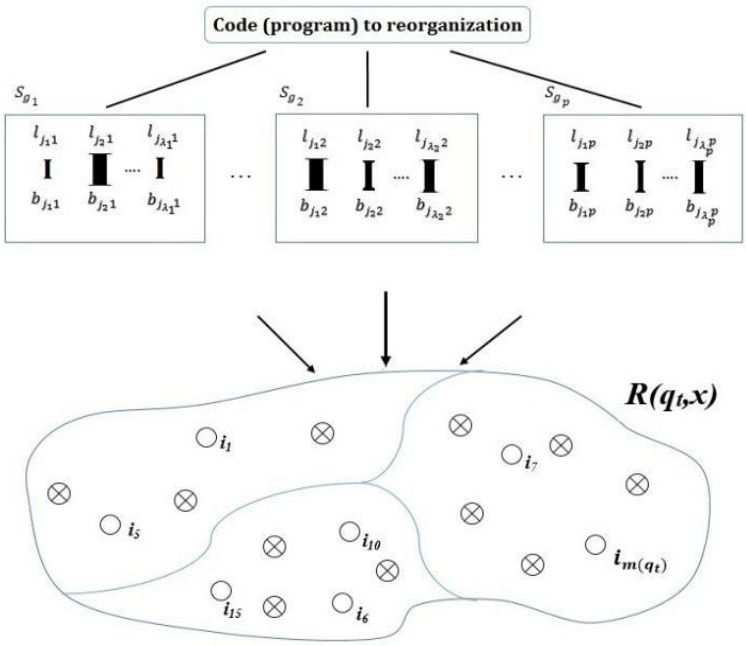


Figure 1. Code (program) reorganization scheme

It's crucial to emphasize that the matrix $x \in X$, is subject to inherent constraints (a)-(c), which we conceptually delineate in [47]. Functionals: For the primary optimization problem, the functional under consideration is the mathematical expectation of the page fault count per program (code) execution. As for an auxiliary objective, the functional represents the average page fault rate over h≥1 program (code) executions.

Note that this kind of functional is standard, for example, for stochastic programming and pattern recognition patterns and takes into account the random nature of the processes involved in the consideration, just like ours. In practical approaches, namely, in our understanding, the second functional is usually taken as a functional of the cost of code restructuring. However, an important question arises here: how$h \geq 1$ individual points in a data field span the entire infinite data field. In other words, the question is: how good is the solution to a problem with auxiliary functionality for the main task? Taking into account this kind of reasoning, we took as the functional of the main optimization problem the mathematical expectation of the number of page faults per one run of the program (code) instead of the average value functional, making an adjustment for the traditional interpretation of the formulation of the restructuring problem [16]-[24].

Constraint (a): this condition ensures that the combined length of blocks assigned to any page does not surpass the page's length.

Constraint (b): this restriction dictates that each program block (code) is assigned to only one page within the program (code).

Constraint (c): this requirement mandates that the cumulative length of any working set generated during program (code) execution does not surpass a predetermined system constant.

Keep in mind that these constraints (a)-(c) are established by the matrix $x = (x_{ri})_{p \times n}$ which dictates how blocks $b_1, b_2, \dots, b_n$ are distributed across pages $S_1, S_2, \dots, S_p$. Despite the wealth of literature dedicated to program restructuring, especially concerning our approach to the problem [4]-[15]. There is still no

definitive solution or appropriate reorganization model capable of achieving precise (optimal) solutions with the specified functionality.

2.1. Monitor the state of the program. Working set generated by control state q and matrix $x = (x_{ri})_{p\times n}$. Set of control states q

Let us recall some definitions. The working set W (k, t) with parameter k (window size) of program (code) pages in RAM at time t of program execution is the set of program pages that were accessed in the last k moments before t during program (code) execution. When discussing the concept of a working set, we typically refer to two related notations outlined by P. Denning: $W(t-\tau,t)$ with window size τ and $W(t-\tau,t)$ with parameter k. In the latter scenario, the integer k≥1 can also be seen as the window size. In the former case, the working set encompasses the program pages referenced within the interval [t- τ,t) of virtual time. In our context, we've adopted the W(k,t) option as the working set. Regarding the control state (cs) qt of the program at time t, we define it as a collection of program blocks referenced in the last k instances before time t. Consequently, the control state (cs) of a program (code) at time t essentially mirrors the working set of pages at that same time, but in terms of blocks.

It's crucial to highlight the significance of the Boolean matrix $x = (x_{ri})_{p\times n}$, which, as previously mentioned, plays a pivotal role in determining the program's structure, specifically how blocks $b_1, b_2, \dots, b_n$ are distributed across pages $S_1, S_2, \dots, S_p$. As established, this matrix x must adhere to constraints (a)-(c), and the collective set of all matrices of this type constitutes X. Ultimately, the objective is to identify an optimal matrix from the set X that delineates the most effective structure for the code (program) based on the aforementioned criteria.

2.1.1. Reference lines to pages and blocks. Control state q_t. Working set $R(q_t, x)$

While observing the reference line for a single program run and its associated frame, segmented into k cells below it, which progressively moves from left to right along the time axis t, it is essential to also consider Figure 2 simultaneously. In Figures 2 and 3, the instances t1, t2, t3 ,… , tγ represent time points sampled from t0 to tγ , which marks the conclusion of the run with random data θ ∈ D. In Figure 2, the labels St along the time axis t, where t=1, 2,3,… ,γ indicate the pages (or their identifiers) accessed during program execution for a specific θ ∈ D, with k=4 and fixed x ∈ X. For Figure 3 designations i(t_j), j=1,2,…,tγ denote block numbers corresponding to page numbers in Figure 2, accessed during program execution for the same θ ∈ D, with k = 4, and the same x ∈ X.

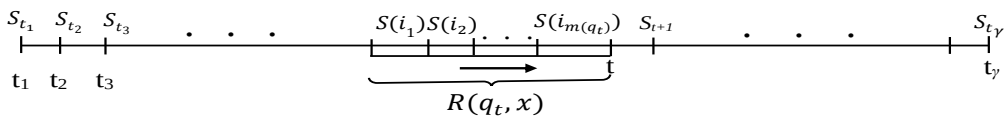


Figure 2. The line of reference to the program pages for one run of the program, where the working set R(q_t, x) is output, corresponds to W(4, t) with k=4 at t = t1, t2,…, tγ

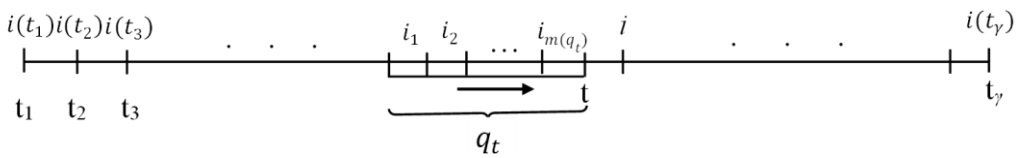


Figure 3. A string of program block references for one program run, where cs is printed for any t process q_t

The frame contents depicted in Figure 3 consist of blocks, which may include repetitions, constituting the control state (cs) $q_t$at time t. Meanwhile, the contents of the frame in Figure 2 comprise page numbers, also potentially with repetitions, which constitute the working set generated $R(q_t, x)$ by the coordinate system qt and the matrix $x = (x_{ri})_{p\times n}$ at time t. Each page $S(i_j)$in the frame contains a block i_j cs q_t, where $j = 1,2, \dots, m(q_t)$.

An important requirement for $R(q_t, x)$, is that each page within it must contain at least one block from the control state q_t. In our scenario, no other type of working set is considered. Hence, we have $\{S(i_1), S(i_2), \dots, S(i_{m(q_t)}\}$, as a multiset $R(q_t, x)$, but the actual working set $R(q_t, x)$ corresponding to it

should not include duplicate pages. Let's denote $R(q,x)$ as the working set without page repetitions corresponding to $R(q_t,x)$. Note that this conversion is easy to do by eliminating the repetition in qt to go from $R(q_t,x)$to $R(q,x)$. Based on Figure 3 it is easy to see that the next cs . q_{t+1} forms like $q_t \cup \{i\}$,i.e. $q_{t+1} = \{i_2, i_3, \dots, i_{m(q_t)}, i\}$. T such an event, i.e. link from cs q_t per block i which we can denote as $q_t \to i$ and number$i$ becomes available towards the end of cs processing q_t.

As shown in Figure 4, which contains a string of references to program at certain times, at the initial moment t_0 we do not have a line of links to pages and blocks, and as a result we have an empty frame. Despite this, for our convenience we have written down the block numbers in advance $i(t_1)$, $i(t_2)$, $i(t_3)$ above the t axis as shown in Figure 4(a), which will appear at the appropriate moments. Note that the block $i(t_1)$ is accessed just before the frame is reached $i(t_1)$ and instantly the number $i(t_1)$ falls into the rightmost cell of the frame as shown in Figure 4(b) and the same thing happens at time t_2 as shown in Figure 4(c).

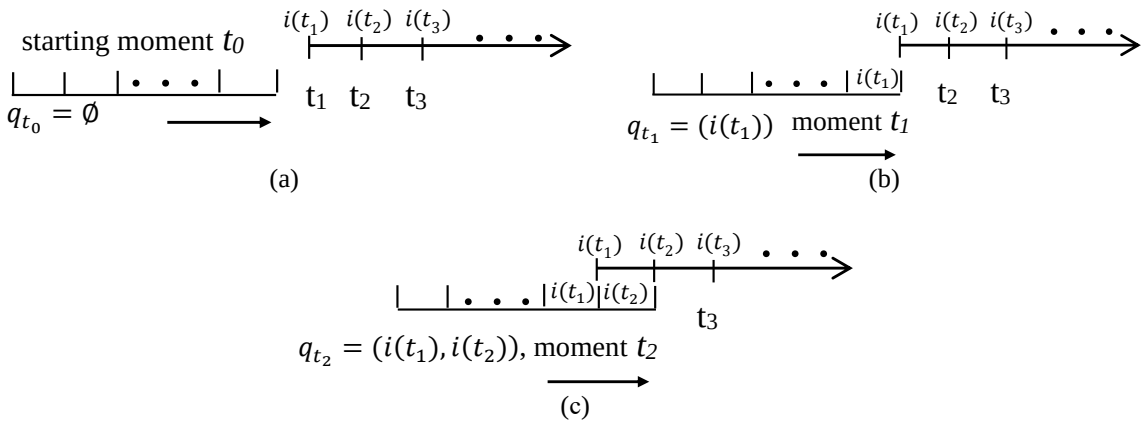


Figure 4. String of references to program at time: (a) t =0, (b) t = 1, and (c) t=2

Thus, as we see, the content of the frame at any moment t with repetitions of block numbers coincides with the control state (cs) of the program at moment t, the designation for it $q_t = \{i_1, i_2, \dots, i_{m(q_t)}\}$ as shown in Figure 3, in contrast to the corresponding designation for cs without repetitions, $q = (i_1, i_2, \dots, i_{m(q)})$ i.e. In addition, we can omit the index t q_t because for us there is no difference between $\{i_1, i_2, i_3\}$ and $\{i_2, i_1, i_3\}$ or $\{i_3, i_1, i_2\}$. And instead of all of them we will write an ordered entry (i_1, i_2, i_3), where $i_1 < i_2 < i_3$. And also for cs $q = (i_1, i_2, \dots, i_{m(q)})$ there is a relation: $i_1 < i_2 < \dots < i_{m(q)}$, where in there $q$are no longer blocked repetitions. By moving the frame along the chain of links to the blocks from left to right, we get the cs part. But it is possible that most of them are multisets, and we consider both of them, i.e. a multiset and its corresponding set without repetitions, as one and the same set. Despite this, for q_t, in contrast to q, a separate clarification of the notation has been introduced, namely, $q_t = \{i_1, i_2, \dots, i_{m(q_t)}\}$ it is treated q_t as a multiset. Having excluded from the found q_t repetitions of block numbers and then, if q_t new, then this one checks the comparison path q_t with q from the set $Q = \{q\}$ formed at the current moment t, q_t must include in it Q as new q. Thus, in the order of a new run of the program (code), little by little we enrich a situation where the set Q does not change. And finally, the set $Q = \{q\}$ consists of different blocks q,, where none of them q have block repetitions and Q does not change even after $\lambda \geq 1$ additional runs.

Here in Figure 5 set $\left\{q_\theta^1, q_\theta^2, \dots, q_\theta^{\mu(\theta)}\right\}$ represents a multiset of control states obtained during a single execution of the code, each corresponding to a distinct $\theta \in D$, and any new state, without repetition, is added to the set Q during subsequent runs, gradually approaching the stable condition depicted as "Is Q stable?" in Figure 5. When answered affirmatively for the first time, it signifies that Q was unstable in previous iterations but has now stabilized in the current iteration, exhibiting no deviation from the previous iteration's Q. If υ is less than or equal to λ, the process follows the top line, updating θ and continuing with the established pattern. The set J consists of blocks labeled with numbers i that emerge during the transition q_t→i as the frame progresses along the time axis in Figure 3. Following at least λ additional runs and reassigning new numbers from 1 to n to elements from J, we form a set of blocks requiring restructuring, which is suitable for further investigation.

However, a question emerges: what if, even after conducting λ or more additional runs, a new control state emerges? This indicates that the initial choice of λ was overly optimistic and necessitates

re-evaluating λ, leading to a requirement to restart the process. The scenario outlined above pertains to both the primary and auxiliary optimization problems. However, in the auxiliary problem, the set J is disregarded. It's important to highlight that in the auxiliary problem, the set J is predetermined.

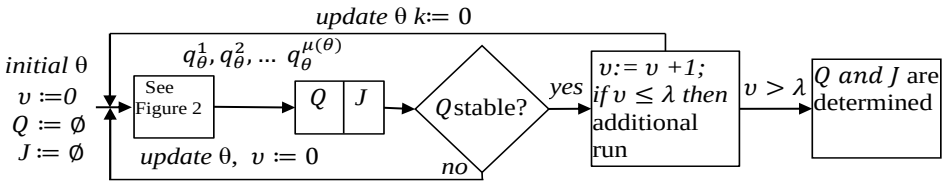


Figure 5. Q and J generation kits

2.1.2. Correlations between cs q_t and cs q_{t+1}

Here cs q_{t+1} as shown in Figure 3 is formed from a subset q_t, including the case itself q_t, which must be connected with $\{i\}$ and then the following relations hold: $q_{t+1} \subset q_t$ or $q_t \subset q_{t+1}$, or $q_{t+1} = q_t$. Indeed, cs $q_t = \{i_1, i_2, \dots, i_{m(q_t)}\}$ and $q_{t+1} = \{i_2, i_3, \dots, i_{m(q_t)}, i\}$ (see middle fragment of Figure 3), then we have several steps to continue:

Step I. If $i_1 \in q_{t+1} = \{i_2, i_3, \dots, i_{m(q_t)}, i\}$ and $i \notin \{i_2, i_3, \dots, i_{m(q_t)}\}$, then $q_t \subset q_{t+1}$, as shown in Figure 6(a).

Next situation

Step II. if $i_1 \in q_{t+1}$ and $i \in \{i_2, i_3, \dots, i_{m(q_t)}\}$ then $q_t = q_{t+1}$ as shown in Figure 6(b).

And further,

Step III. if $i_1 \notin \{i_2, i_3, \dots, i_{m(q_t)}\}$ and $i \notin \{i_1, i_2, \dots, i_{m(q_t)}\}$ then $q_t \nsubseteq q_{t+1}$ as shown in Figure 6(c). Here $q_t = \{i_1, i_2, \dots, i_{m(q_t)}\}$ and $q_{t+1} = \{i_2, i_3, \dots, i_{m(q_t)}, i\}$

Step IV. If $i_1 \notin \{i_2, i_3, \dots, i_{m(q_t)}\}$ and $i \in \{i_2, i_3, \dots, i_{m(q_t)}\}$ then $q_{t+1} \subset q_t$ as shown in Figure 6(d), where $q_t = \{i_1, i_2, \dots, i_{m(q_t)}\}, q_{t+1} = \{i_2, i_3, \dots, i_{m(q_t)}\}$

Steps I, II, IV are standard, but for step III we can assume that while the intermediate node q is going through the process, the time instant is t+1/2 as shown in Figure 6(c). In fragments of Figure 6 one can notice an arc (q_t, q_{t+1}), and an arc $(q_t, q_{t+1/2})$ and an arc $(q_{t+1/2}, q_t)$, each of which has a weight $(\pm i, \beta)$ where $\beta \in \{0,1\}$. Here $\pm i$ this refers to the movement up or down, which either enriches the cs q_t as shown in Figure 6(a), with i moving up or depletes cs q_t as shown in Figure 6(b), by i_1 (downward movement) or sequentially both of them as shown in Figure 6(c). Number i without a sign (Figure 6(d)) means that $q_t = q_{t+1}$ the situation β parameter equal to 1 or 0 and refers to the event when a page fault occurs or not on the corresponding transition from cs q_t to cs q_{t+1}.

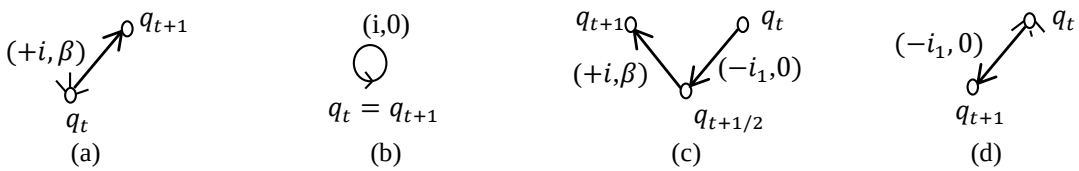


Figure 6. Options for movement in bipolar combinatorial space; (a) step I, (b) step II, (c) step III, and (d) step IV

2.1.3. Final notices for defining a set of control states Q

After conducting multiple executions of the program with various values of θ from the set D and repeated determination of cs q_t, once we encounter a situation where the set Q remains unchanged, and after at least λ≥1 additional executions where the set Q stays the same, we will consider the set Q to be defined. Initially, let's designate a special cs. $q_0 = \emptyset$ for the set Q, representing the starting point of the process. This initial state q_0, can also occur later if the program is unexpectedly evicted from main memory and later reactivated, essentially starting from scratch (cold start). Another scenario is a warm start, where the system ensures that the computing process, including control state, is restored to the state just before the program was evicted, allowing it to resume from where it left off without being affected by timeouts in secondary memory.

3. RESULTS AND DISCUSSION

SVM system built on 10 field-programmable gate arrays (FPGAs) forming a multi-computer system of the SVM type based on [48]. To study the effectiveness of caching in this system, the same memory access algorithms were run, which are the worst possible options for any type of caching. Namely, access to a random memory address. It is worth noting that the FPGA implements a high-frequency timer counter that measures the time it takes to receive the desired page. This approach allows you to obtain the time of not only medium and long-time page faults, but also short ones. Also, to minimize the error in measurements, a logging module similar to the methods presented in [49] was implemented on each of the FPGAs, the task of which was only to output data via USB-TTL to a separate computer. This data exchange method is widely used in many works, for example in [50].

The hardware part of this system is the DE2-115 development boards from Terasic, which include 2 network cards and all the necessary components, which made it possible to connect the devices into a local network using a ring topology. Conventionally, research on an FPGA system can be divided into 2 types as shown in Figure 7. Without RAM overflow and with RAM overflow of the computing node. In the first case, it is assumed that we have a reserve of memory in RAM on the computing nodes, which is not used by the system and is allocated for caching. And in the second case, memory is allocated by reducing the data currently located on the computing node.

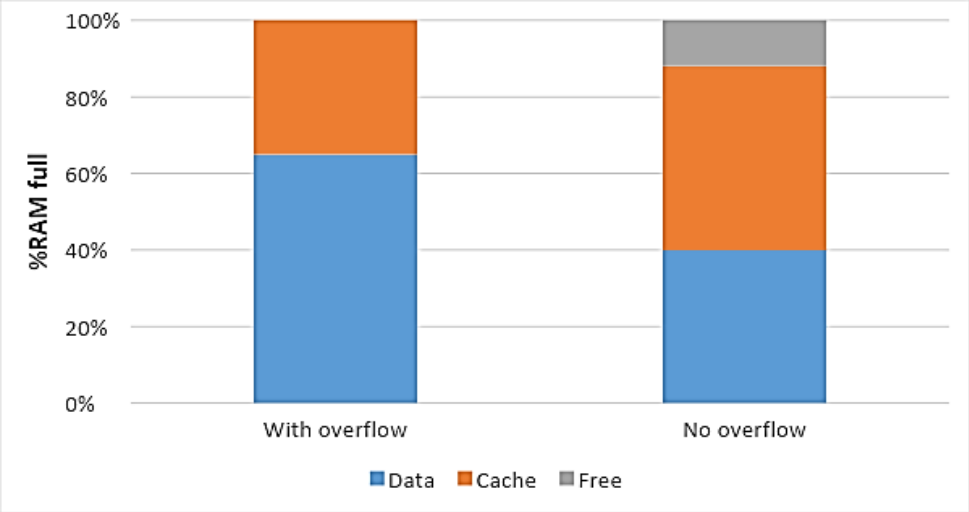
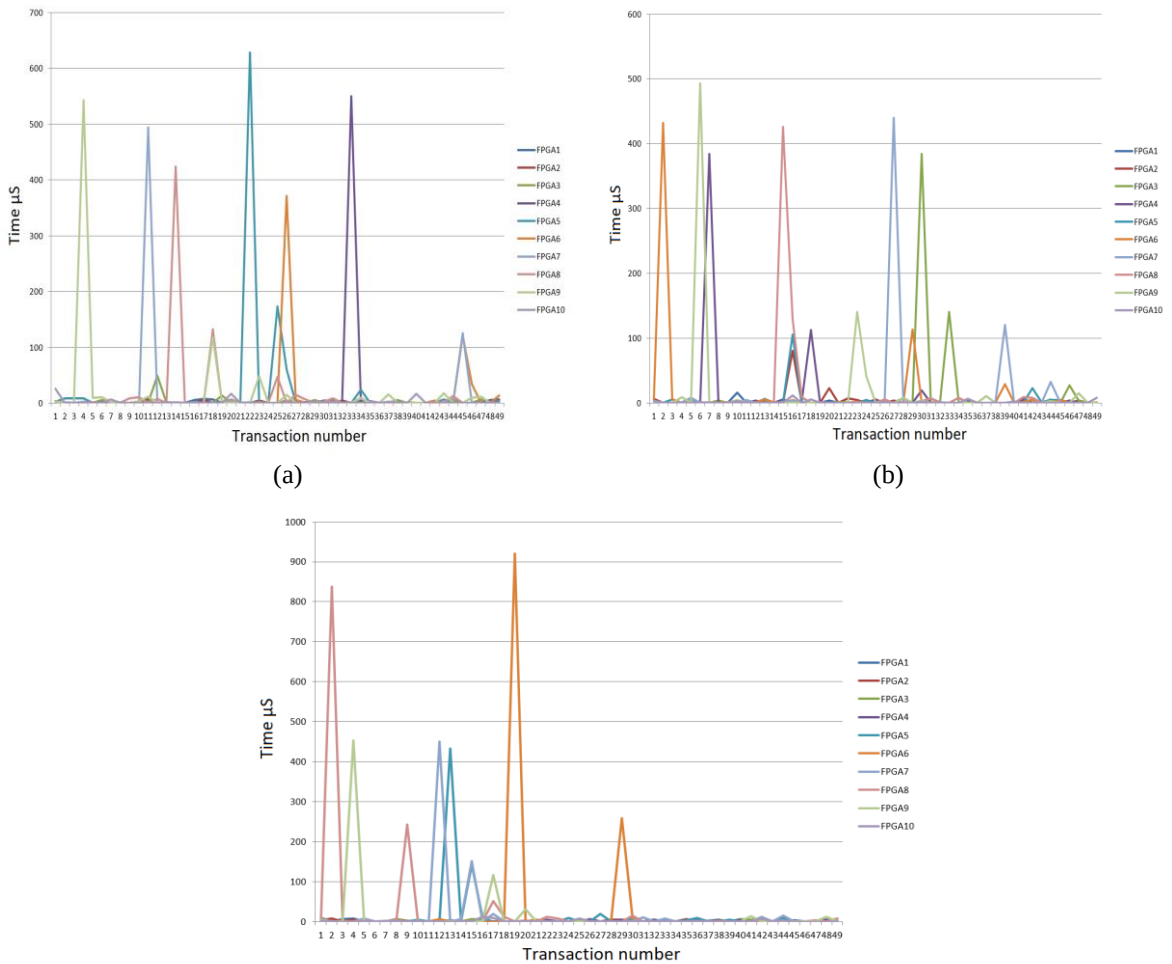


Figure 7. RAM distribution

Due to the fact that the implementation of caching on the FPGA is hardware, and the measurements are output via a serial port to another computer for further analysis. It becomes possible to investigate page faults of each of the computing nodes without reducing system performance. Page fault data was measured at each compute node at 1 MHz.

Consider the following option: a computational program is given in which 80% of the calculations occur in the memory allocated for a specific node and 20% of the data is requested from other nodes. Each computing node must perform 100,000 operations. In this case, in one case, 5% of the memory for the cache is taken from free space in RAM, and in the second, from the main memory available for data.

In Figure 8 we can see how much time it took each of the computing nodes to perform each operation at the busiest moment for the switching network, namely the beginning of calculations. It is at this moment that the largest flow of data occurs, both for caching and for obtaining the initial data pages. For example, without adding caching as shown in Figure 8(a), the duration of long page faults reached 630 microseconds, and the average time of long page faults is about 500 microseconds. After adding 5% cache from free memory as shown in Figure 8(b), long-time page faults decreased to an average of 400 microseconds. And after adding 5% cache from the data memory as shown in Figure 8(c), you can see that extremely long page faults appeared, but at the same time, both the number of long page faults and the duration, which in most cases did not reach 450 microseconds, decrease.



(a) (b)

(c)

Figure 8. Measuring page fault times: (a) without caching, (b) without overflow, and (c) overflow caching

Next, let's look at one of the computing nodes in more detail. As can be seen in Figure 9, in addition to long-term page faults, many short and medium-duration page faults occur during calculations. For example, if we consider a system without a cache as shown in Figure 9(a), the average duration of page faults is about 7 microseconds, and the page fault rate is about 40%. It is worth noting that such a high frequency of page faults occurs due to the fact that the computing node not only takes data pages from the system but also returns them. In the worst case, a situation may arise that the computing node will wait for the required page for a sufficiently long period of time, thereby forming a long-term page fault.

Figure 9(b) also shows that when adding cache from free memory, the average duration of page faults decreased from 7 to 6 microseconds, while reducing the number by an average of 3%. And after adding a cache from data memory as shown in Figure 9(c), the duration of page faults not only did not decrease, but in some places increased to 13 microseconds. It is worth noting that the number of page failures has significantly decreased. And it was about 20%.

Looking at a longer period of time as shown in Figure 10, one can notice an increase in the duration of page faults. This is due to the fact that an increasing number of pages are located in other computing nodes. Figure 11 shows the ratio of normal operations to page faults. As can be seen from these graphs, as pages move from one node to another, the number of page faults normalizes and, as a result, their duration stabilizes.

In Figures 12 and 13 show page fault durations before and after adding the cross-page. If we consider the stabilized period of calculations without caching as shown in Figure 12(a), then the average duration of line failures without a cache was about 15 microseconds, with peaks up to 30 microseconds. At the same time, with the addition of a cache from free memory as shown in Figure 12(b), the duration of page faults was reduced to 12 microseconds with peaks of up to 20-25 microseconds. And after adding a cache from data memory as shown in Figure 12(c), no significant changes were noticed.

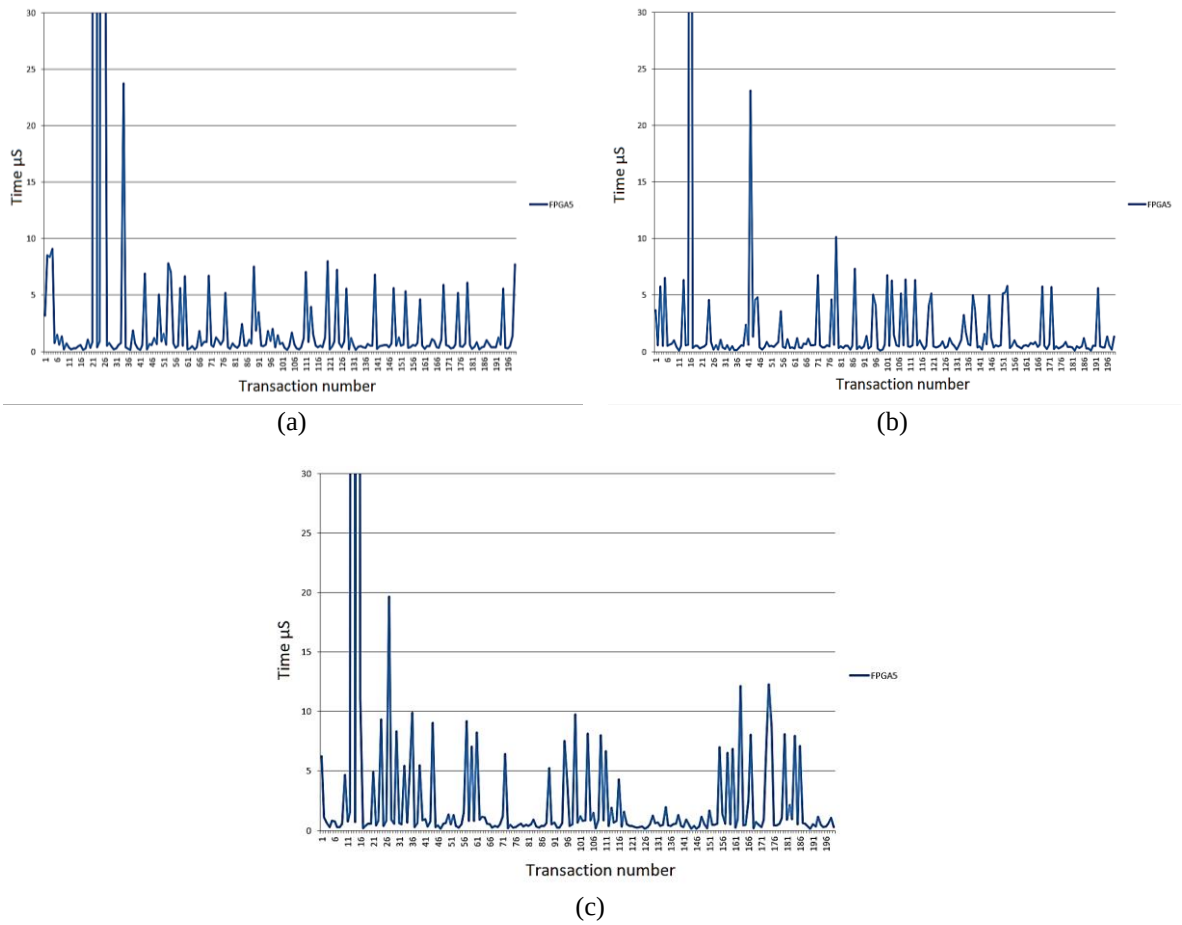


Figure 9. Measuring the time of page faults: (a) without caching, (b) with caching without overflow, and (c) with caching and overflow from 1 to 200 operations

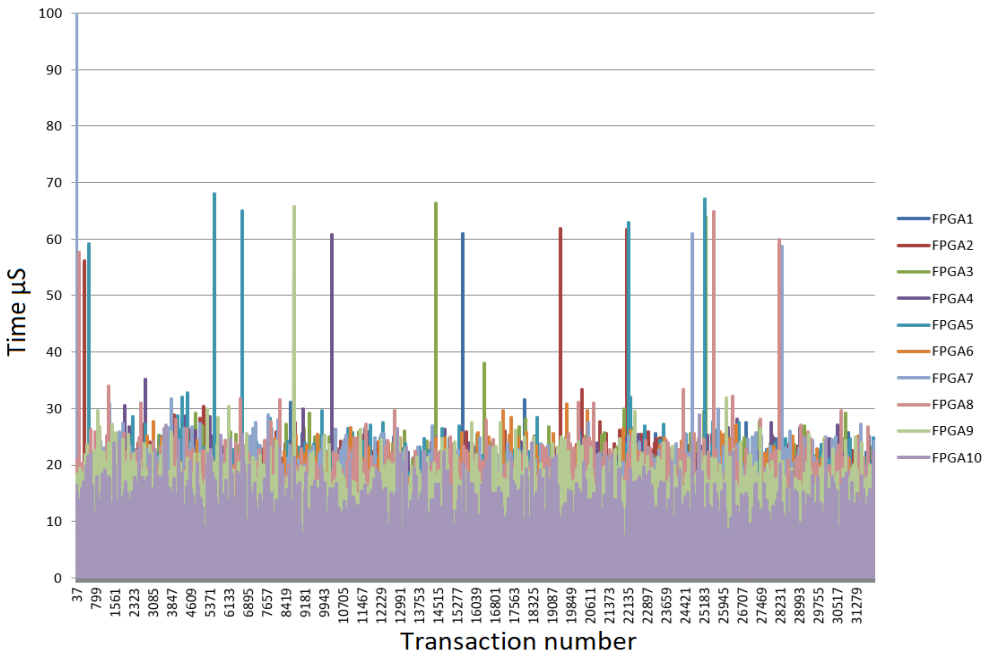


Figure 10. Measurement of page fault time without caching from 37 to 35,000 operations

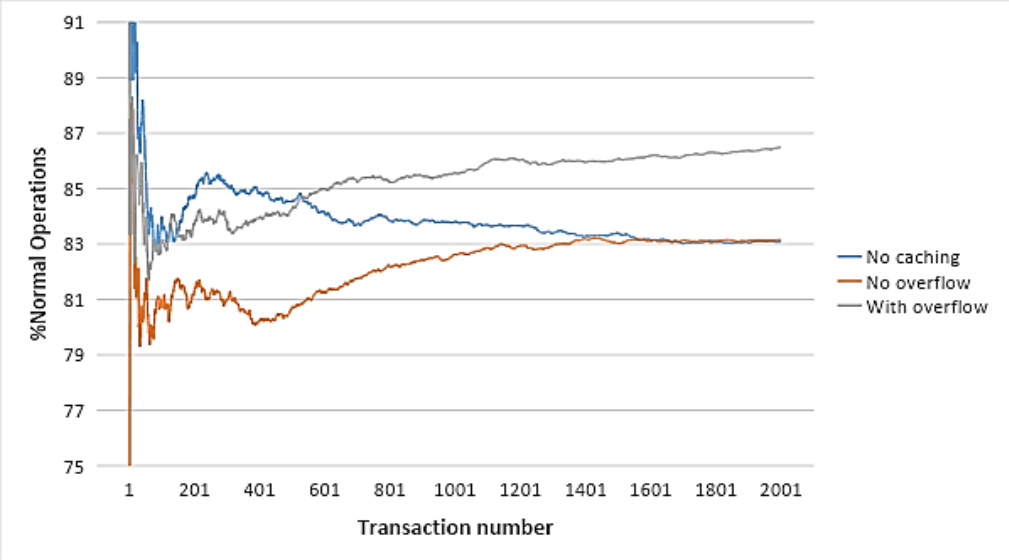


Figure 11. Percentage ratio of normal operations to page faults without caching from 1 to 2,000 operations

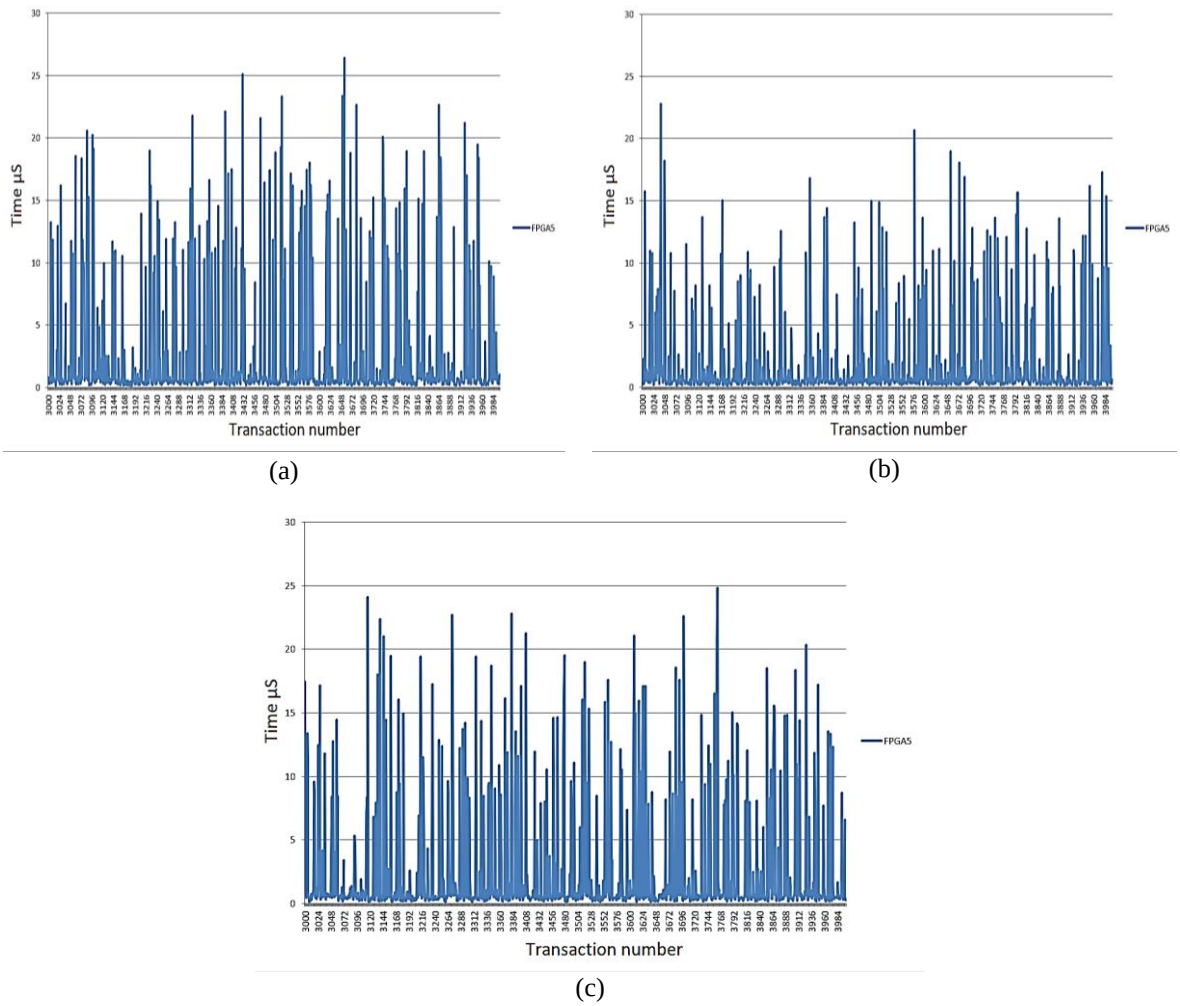
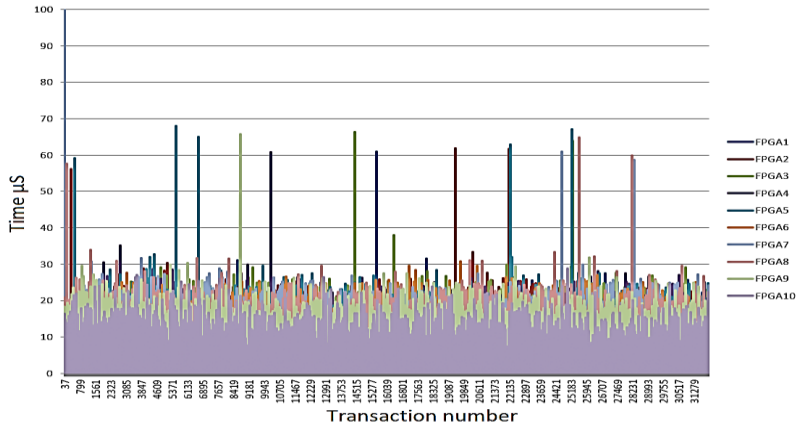
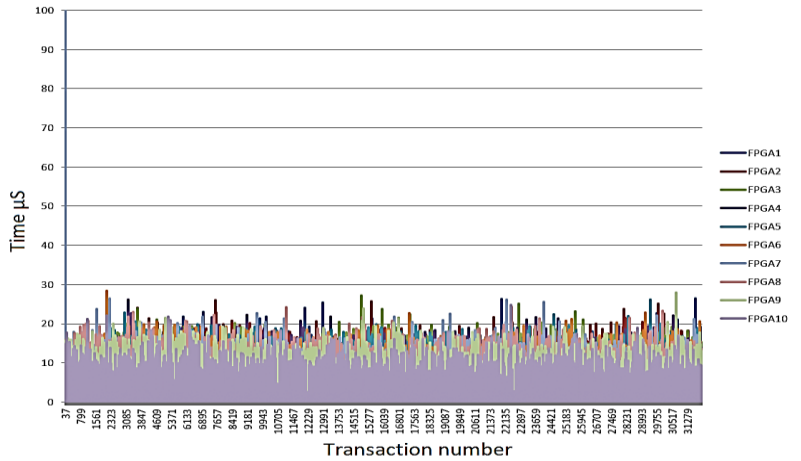


Figure 12. Measuring the time of page faults: (a) without caching, (b) with caching, and (c) with caching and overflow from 3,000 to 4,000 operations

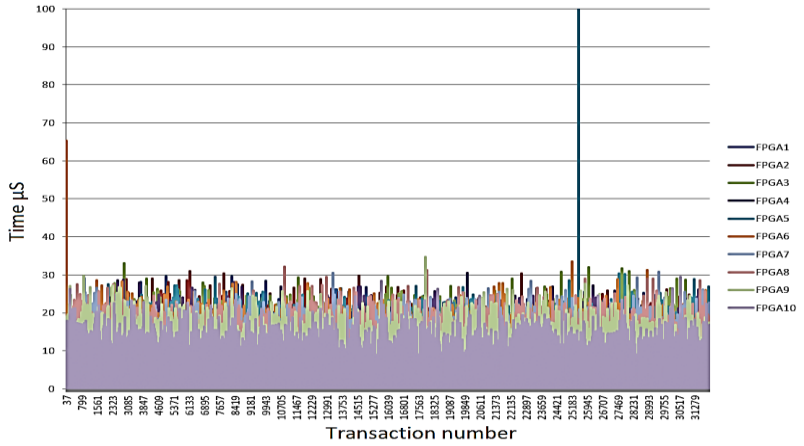
Measuring the time of page faults as shown in Figure 13. Moreover, if we consider a long period as shown in Figure 13(a) for very rare events, that is, long-term page faults. Adding a cache from free memory as shown in Figure 13(b) or adding a cache from data memory as shown in Figure 13(c) significantly reduces their number. Due to this, the performance of the system significantly increases.



(a)



(b)



(c)

Figure 13. Measuring the time of page faults: (a) without caching, (b) with caching without overflow, and (c) with caching and overflow from 37 to 35,000 operations

As a conclusion from the study on FPGA, it can be noted that the execution time without caching was 15 seconds. The execution time with a cache from free memory was 13 seconds, and the execution time with a cache from data memory was 14 seconds. Moreover, if you look at the program execution graph depending on the cache size at 20% of the requested data, you can clearly see the effectiveness of caching.

4. CONCLUSION

In the course of this work, the use of page caching in the RAM of computing nodes in multicomputer systems such as SVM using the working set strategy was investigated. An FPGA-based SVM system was proposed and implemented, and research was conducted to evaluate the effectiveness of caching in hardware implementation. In a study on FPGA, it was found that the execution time with a free cache was 13 seconds and the average duration of page faults decreased from 7 to 6 microseconds, while reducing the number by an average of 3%. The execution time with the cache from data memory was 14 seconds, but the average duration of page faults in some cases began to reach 13 microseconds and the number of page faults was reduced to 20%. While without caching this time is 15 seconds, the average page fault duration is about 7 microseconds, and the page fault rate is about 40%. The performance gain from adding a cache from free RAM memory with one of the worst memory access options was 14%. These results confirm the effectiveness of hardware-based caching. In general, this study can be useful for improving the performance of SVM systems under various application conditions and for developers of distributed computing systems.

ACKNOWLEDGEMENTS

This work was funded by Committee of Science of Republic of Kazakhstan AP09260767 "Development of intellectual information-analytical system for assessing the health of students in Kazakhstan" (2021-2023).

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