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Analysis of the parasitic capacitance effects on the layout of latch-based sense amplifiers for improving SRAM performance

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ABSTRACT

Static random-access memory (SRAM) technology is utilized in designing cache memory to enhance the processing performance of computer systems. The sense amplifier (SA) circuit, a crucial component of memory design, significantly impacts data access time and power consumption. In comparison to conventional differential sense amplifiers (DSA) designs, latch-based sense amplifiers (LSA) used in memory-based computing platforms have specific requirements, including robust noise resistance in harsh working environments and low power consumption, particularly for internet of thing (IoT) embedded computing applications. However, the performance can be degraded due to various factors that arise during the layout, such as conductor resistance or the development of parasitic capacitance. Therefore, this study employs low-voltage 22 nm UMC CMOS technology for LSA design layout and analyzes the factors influencing design performance post-layout process. Layout design optimization techniques are applied to mitigate the impact of parasitic capacitance on important signal lines such as data line/data line bar (DLL/DLLB). Based on the performance analysis results, it is possible to achieve a reduction in power consumption of up to 15% and a 5% decrease in read delay time by implementing circuit layout LSA design optimization techniques.

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1. INTRODUCTION

The integration of fast-access static random access memory (SRAM) technology as a cache is employed to address the bottleneck issue commonly observed in traditional von Neumann computer architecture [1], [2]. Nowadays, computer design is extensively integrated into intelligent applications to fulfill the requirements of distributed computing in the realm of the internet of things (IoT) [3]-[6]. This presents numerous new challenges concerning energy consumption and data access speed. Within the SRAM design, the sense amplifier (SA) plays a vital role in determining access time, power usage, and reliability [1], [2], [7]. The primary function of the SA is to detect data by analyzing the voltage difference between the two-bit lines and amplifying slight voltage variations to logic levels. Typically, SRAM memory design utilizes the array connection approach where memory cells in the same column are connected to the same bit line/bit line bar (BL/BLB) line [1], [8], as depicted in Figure 1. Consequently, the capacitance on the BL/BLB lines directly impacts the performance of the SA circuit when sensing the data stored in each memory cell. Compared to conventional differential sense amplifiers (DSA) design, latch-based sense amplifiers (LSA) demonstrate superior performance [1], [2], [9]-[14] in terms of power consumption and

reliability in the presence of interference, thanks to their foundation on the data latching principle. This makes LSA well-suited for computer designs that operate in low-power and high-signal noise environments.

Regarding layout, random access memory designs require high integration density and symmetry due to the arrangement of memory cells in arrays [1], [2], [8]. An optimal physical structure of transistors and interconnecting lines enhances processing speed and reduces power consumption [1], [2]. Thus, it is crucial to analyze physical factors that arise during the layout process, such as conductor capacitance and length, resistance, parasitic capacitance, and signal propagation delay. Among these factors, parasitic capacitance significantly influences power consumption and signal propagation delay in memory design due to the charging and discharging operations associated with newly formed parasitic capacitors during the layout process [15], [16]. This issue is often overlooked or simplified during pre-layout simulations.

Previous studies have addressed issues related to the performance of SRAM designs and the complete SRAM layout process. However, these studies have either focused solely on analyzing SRAM memory cells or examining the performance of SA circuit configurations, without specifically delving into the analysis of the parasitic capacitance factors that impact power consumption and data access speed. Notable research in this area includes the following studies: Research by Hassan *et al.* [17] compares the design of SRAM using two different SA circuit layouts on 180 nm CMOS technology. The study involves laying out two SA circuits and investigating power consumption and delay at various voltage levels. However, the impact of parasitic capacitance on the performance of the SA design is not addressed in this research. Praveen and Shivaleelavathi [18] focus on the complete layout of a 1 KB SRAM design, including SRAM bitcells, precharge, LSAs, and other components. The study provides comprehensive layout drawings using both 180 nm and 45 nm CMOS technologies for the SRAM blocks, along with results from design rule checks (DRC) and layout versus schematic (LVS) verification. However, optimization strategies for achieving operational performance are not discussed. Bauer's investigation [19] explores various layout options for multi-gate-FET (MuGFET) SRAM cell design. Detailed measurement results for four different core cell layouts using 65nm CMOS technology are presented. However, the study primarily analyzes static noise margin (SNM) and write ability for different layout variants of the SRAM bitcell. The layout of the SA and analysis of physical factors remain unaddressed in the article. Luo *et al.* [20] focuses on layout optimization for 6T-SRAM cells, considering parasitic factors such as capacitance and resistance under advanced nodes beyond 3 nm. The study proposes a methodology to determine the direction of layout optimization for 6T-SRAM cells by assessing their sensitivity to various parasitic parameters. Additionally, the research highlights that parasitic capacitance significantly impacts performance degradation in SRAM compared to parasitic resistance.

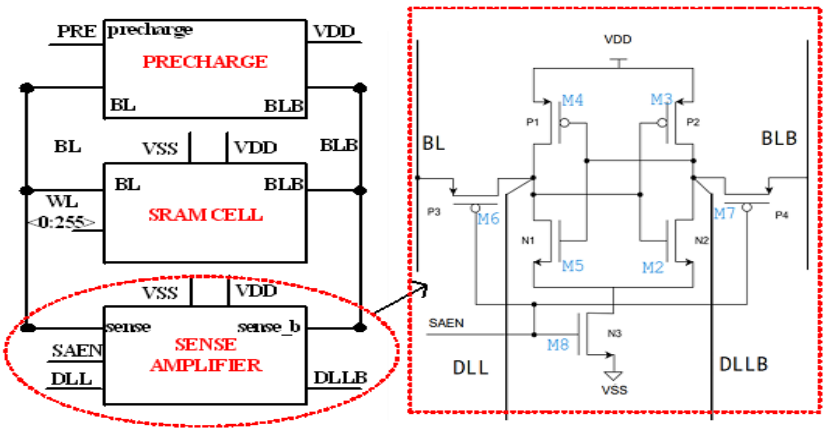

Figure 1. The fundamental components of the SRAM memory design and the schematic design of the LSA circuit

To elucidate the impact of physical factors, particularly parasitic capacitance, on memory performance, precisely read delay time, and dynamic power consumption, this study focuses on the layout of LSA design using 22 nm united microelectronics corporation (UMC) complementary metal-oxide-semiconductor (CMOS) technology [21]. The influence of parasitic capacitors on access time and power consumption is considered. Various techniques are applied in the layout process to rearrange signal lines and position transistors to achieve a balanced configuration of parasitic capacitances. This approach enhances memory performance while simultaneously reducing power consumption and access time.

This paper is organized as follows. Section 2 states the necessity of considering the impact of parasitic capacitance factors when performing layout and presents the method used to optimize power and memory access time after the layout process. The application of arrangement and optimization methods for the SA layout, which brings symmetry to the design, is presented in section 3. The use of the Monte Carlo bisection method combined with the analysis of delay time and power consumption to demonstrate the importance of considering parasitic capacitance factors in performance is shown in Section 4. Finally, the discussion on the results achieved and directions for further research are presented.

2. PARASITIC CAPACITANCE IN THE LSA LAYOUT

As mentioned above, in implementing the layout for the LSA circuit, it is crucial to analyze and address the effects of parasitic capacitances. Parasitic capacitance significantly impacts the performance of both the SA and the SRAM memory [15]. This study utilizes the 22 nm technology for several reasons. Firstly, the advanced CMOS technology offers smaller sizes, enabling increased integration density. Additionally, the technology operates at a lower voltage range of 0.6 V to 1 V, providing improved energy efficiency compared to the previous 28 nm technology [21]-[23]. To meet demanding power consumption requirements, such as caching, design performance can be optimized by reducing leakage currents by up to 30% using UMC's 22 nm fin field-effect transistor (FinFET) technology [21]-[23]. Furthermore, the employment of advanced back-end-of-line (BEOL) Processes facilitates efficient signal routing, reducing impedance and capacitance and thereby enhancing the overall circuit design performance [24].

Figure 2 depicts the sequential stages encompassed in the design and optimization procedure for the circuit layout of LSAs. Using the cadence spectre [25], the SRAM design, including the LSA circuit, is initially simulated to validate its functionality by examining waveforms of critical signals such as write line (WL), BL/BLB, sense amplifier enable (SAEN), and DLL/DLLB. This pre-layout simulation ensures the correct operation of the SRAM. Once the LSA design is confirmed to work correctly, the layout for the LSA is implemented using UMC's 22 nm CMOS technology. In this process, the size of the SA circuit needs to be adjusted based on the layout of the BL/BLB lines and the size of the SRAM memory cell. For 22 nm CMOS technology, each memory cell has a size of 0.71 µm [21]. The primary objective during layout design is to minimize the design area while adhering to the rules of design rule check (DRC) [26]. This maximizes integration density per unit area and minimizes production costs. Once the layout design satisfies the technological constraints specified by DRC and passes the principal design check through the layout versus schematic (LVS) [26] test, the next step involves extracting the parasitic capacitance values. If there is an asymmetrical parasitic capacitance between critical signal lines, layout optimization techniques, such as transistor repositioning and layout adjustments, are applied to balance the parasitic capacitance on the signal lines. After achieving a symmetrical memory layout that meets both DRC and LVS constraints, the basic operations of the SRAM are validated again. If the waveforms of the underlying signals match those obtained in the pre-layout simulation, the optimized layout design proceeds to the analysis of time delay and power consumption.

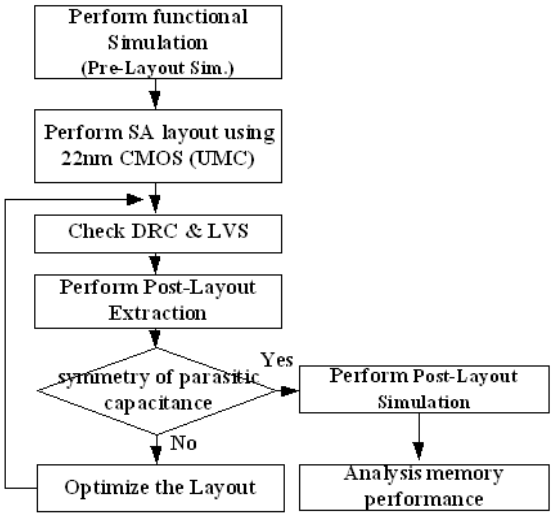

Figure 2. Steps involved in the design and optimization process

Table 1 provides specific information on the parasitic capacitors obtained through layout extraction. These capacitors are formed due to the proximity of metal conductors used for signal connections and the placement of transistors [15], [16], [27]. During switching operations, these parasitic capacitors can cause crosstalk noise [28]. The cap./total value for each signal line of the DLL/DLLB pair indicates the extent of their influence. It is essential to balance these signal lines to prevent interference with the DLL/DLLB [1], [15], [27]. By examining Table 1, it is evident that the signal line with significant capacitance has a notable impact on the total parasitic capacitance, including VDD, VSS, SAEN, and RBL/RBLB. For the VDD source line, the capacitance on the DLL (C=202 aF) is more significant than that on the DLLB (C=169 aF), indicating a bias towards the DLL. Conversely, for VSS, the capacitance on the DLLB (C=163 aF) is more significant than that on the DLL (C=106 aF), signifying a greater influence of VSS on the DLLB.

The presence of asymmetric parasitic capacitors on the DLL/DLLB paths is evident. Achieving a balanced state in transistor placement and realignment of transistor connections is crucial to balance the parasitic capacitors on critical signal lines. Furthermore, adopting the balanced metal layer usage technique ensures an even distribution of metal layers in the layout, preventing the formation of asymmetric parasitic capacitance when using only one metal layer. This study implements several fundamental layout techniques, such as shielding with sheet metal, increasing the distance between signal lines, and ensuring transistor symmetry.

Table 1. The parasitic capacitance values obtained through layout extraction

Signal CAP.	DLL				DLLB				C_DLL/C_DLLB
	ID	Net name	Cap. (F)	Ratio (cap./total cap.	ID	Net name	Cap. (F)	Ratio (cap./total cap.	
	C8_22	DLLB	4.44E-16	39%	C8_22	DLL	4.44E-16	39%	100%
	C8_23	RBLB	2.75E-17	2%	C7_16	RBLB	7.71E-17	6%	108%
	C8_24	RBL	8.36E-17	7%	C7_17	RBL	4.27E-17	4%	64%
	C8_25	VDD	2.02E-16	18%	C7_18	VDD	1.69E-16	15%	120%
	C8_26	VSS	1.06E-16	9%	C7_19	VSS	1.63E-16	14%	65%
	C8_27	SAEN	7.22E-17	7%	C7_20	SAEN	6.22E-17	5%	116%
	C9_29	NET38	2.03E-16	18%	C9_30	NET_38	1.91E-16	17%	106%
	Total Cap.		1.14E-15	100%	Total Cap.		1.15E-15	100%	99%

3. LAYOUT OPTIMIZATION

Let's first consider the impact of VDD and VSS power supply signals on the DLL/DLLB signal lines. As depicted in Figure 3, the corrected signals are shielded by VDD (green) and VSS (blue). For the SAEN signal, using only one line, as depicted in Figure 3, results in a shorter distance between SAEN (orange) and the DLL line (purple) compared to the DLLB line (red), resulting in a larger parasitic capacitor value for DLL (C=72.2 aF) compared to DLLB (C=62.2 aF), as detailed in Table 1. This issue is resolved by introducing an additional symmetrical SAEN line around the Y-axis and adjusting the DLL and DLLB lines to ensure an equal distance to SAEN. Capacitive equalization for RBL/RBLB and DLL/DLLB signal line pairs can be achieved by arranging the metal layers for these signals in a symmetrical and balanced manner across the Y-axis and at each n-channel metal-oxide semiconductor (NMOS) and P-channel metal-oxide semiconductor (PMOS), as illustrated in Figure 3.

Figure 4 illustrates the layout design of the LSA circuit after applying rearrangement methods to adjust the balance of parasitic capacitance. The variation between signal lines causes an imbalance of parasitic capacitance in the layout and after calibration. Comparing the capacitance analysis data in Table 1, the deviation of parasitic capacitance between the signals is significantly reduced and nearly balanced when the C_DLL/C_DLLB ratio in all cases is approximately 100% after calibration, as shown in Table 2.

However, in the case of the parasitic capacitor value on the DLL/DLLB data signal for the VSS power line, there is a deviation of about 8%, unlike other cases where the deviation is 100%. In this specific case, the capacitance value of VSS for the DLL/DLLB signal pair constitutes a small percentage of the total capacitance on both DLL and DLLB signal lines, 5% and 4%, respectively. Since VDD and VSS power lines are highly stable signals, they will not be affected by the coupling tendency of the signals through the same capacitance during switching, resulting in no interference to the signal integrity. Therefore, the slight difference in capacitance due to VDD or VSS with no significant deviation, as analyzed above, can be considered acceptable.

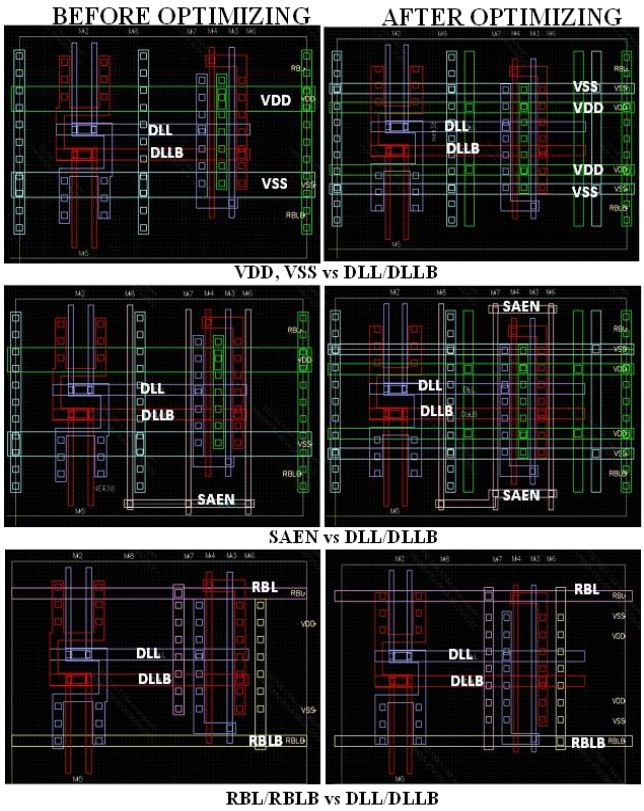

Figure 3. The sense amplifier layouts before and after applying rearrangement methods for the VDD and VSS power lines, the SAEN signal line and the RBL/RBLB signal lines

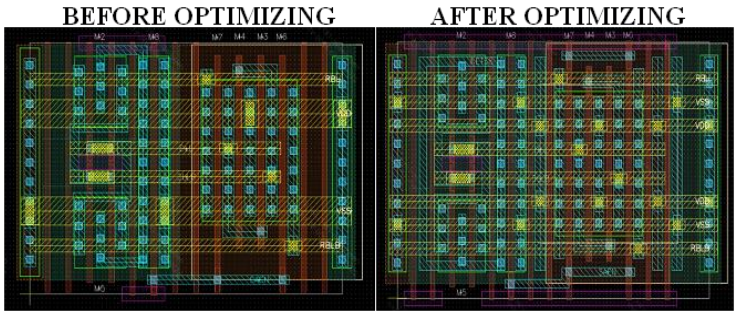

Figure 4. Arrangement of the entire LSA circuit before and after applying rearrangement methods to adjust the balance of parasitic capacitance on the DLL/DLLB data signal

Table 2. The parasitic capacitance values obtained through layout extraction after applying the layout optimization process

Signal CAP.	DLL				DLLB				C_DLL/ C_DLLB
	ID	Net name	Cap. (F)	Ratio (cap./total cap.	ID	Net name	Cap. (F)	Ratio (cap./total cap.	
	C8_22	DLLB	4.57E-16	38%	C8_22	DLL	4.57E-16	38%	100%
	C8_23	RBLB	2.76E-17	2%	C7_16	RBLB	8.28E-17	7%	100%
	C8_24	RBL	8.29E-17	7%	C7_17	RBL	2.77E-17	2%	100%
	C8_25	VDD	2.59E-16	21%	C7_18	VDD	2.59E-16	21%	100%
	C8_26	VSS	5.66E-16	5%	C7_19	VSS	5.24E-16	4%	108%
	C8_27	SAEN	8.73E-17	7%	C7_20	SAEN	8.76E-17	7%	100%
	C9_29	NET38	2.48E-16	20%	C9_30	NET_38	2.20E-16	21%	99%
	Total Cap.		1.22E-15	100%	Total Cap.		1.22E-15	100%	100%

4. PERFORMANCE ANALYSIS

Following the finalization of the layout for the LSA design, this study assessed the impact of parasitic capacitors on performance after implementing the layout. The evaluation primarily focused on Delta-V, which plays a significant role in influencing the overall performance of memory designs. Delta-V is a crucial specification determining the acceptable voltage margin for read and write operation. It represents the voltage difference between the high and low levels that the memory cell can withstand without encountering errors or malfunctions. A significant power consumption occurs when switching takes place due to the substantial difference in Delta V supply. This is because the power consumption of an SRAM cell is in direct proportion to the voltage difference between the data bitlines, with a larger voltage difference resulting in higher power consumption. As such, it is imperative to design the Delta-V value to achieve the minimum value while ensuring stable memory operation. Through careful consideration and optimization of Delta-V, memory designers can guarantee the reliable and efficient performance of memory circuits. However, it should be noted that reducing the voltage difference can increase the design's sensitivity to noise [28], as a smaller Delta-V means that even a small amount of noise can cause errors in the circuit's operation. To address this issue, this study employs a symmetric layout with balanced capacitances on bitlines as a technique to enhance noise immunity.

In this study, the Monte Carlo bisection method [29] is employed to efficiently and accurately determine the Delta-V value while adhering to the design constraints of SA. Figure 5 displays the Delta-V values at various process corners, both before and after layout implementation and after layout optimization. In the typical-typical (TT) case, where both PMOS and NMOS transistors operate in typical mode, Figure 5 demonstrates that the differential voltage values of the sensing and amplification circuits change and tend to increase at all process corners after layout implementation. Specifically, Delta-V increased by around 10% after layout implementation compared to pre-layout values, rising from 73 mV to 79 mV. This increase is attributed to parasitic capacitances created by the metal connections and suboptimal transistor arrangement during the layout process. However, Delta V decreased by 5% after layout optimization, reaching 76 mV. These results indicate that the layout design process introduces parasitic capacitance, deviating the LSA circuit from its original ideal design. Layout optimization aims to bring the circuit as close as possible to its original design performance. The most negligible difference in Delta V was observed in the fast-fast (FF) corner, while the fast-slow (FS) corner exhibited the maximum contrast with a value of 16 mV. Therefore, the difference after layout optimization across process corners is approximately 5% compared to the pre-layout Delta V value.

The data access time on the memory determines the processing performance of a computer [1], [2], [5]. Therefore, it is essential to optimize the delay time for data read operations. In LSA design, the delay is influenced by the internal resistance of the signal line and the parasitic capacitances. The time it takes to sense and amplify the voltage difference between two bitlines into a complete logic level determines the delay. This delay can be reduced by achieving symmetric capacitance between bitlines through an optimized layout design process. As mentioned in the previous section, implementing the layout introduces parasitic capacitance, which significantly affects the delay time compared to the ideal design. The three primary factors contributing to circuit delay are the capacitance on the BL/BLB line resulting from bit line sharing, the resistance of the metal layers used for circuit connections, and the parasitic capacitance of the SRAM memory cell. After doing layout optimization, if the capacitances on both sides of the SA are balanced, the voltage on both sides will change at the same rate, reducing the time it takes for the differential voltage to be amplified [30]. Additionally, a symmetrical layout with balanced capacitances can help minimize variations in delay due to factors such as process variations, temperature changes, and supply voltage variations [31].

Figure 6 illustrates the changing in delay time for data reading as the capacitance value on the BL/BLB line varies from 10 fF to 200 fF. Assuming a capacitance value of C=200 fF for the shared bit line, the delay time increases significantly after layout implementation. It rises by approximately 6%, from 80 pS to 86.6 pS. Similarly, with C=100 fF, the delay increases by about 6%, from 78.6 pS to 83.3 pS, both before and after layout implementation. The asymmetrical layout of the amplifier and sensing circuitry has a significant impact on parasitic capacitance. However, after optimizing the layout design, the difference in delay for the data reading process is reduced to approximately 2% of the original ideal value when not considering the layout perspective.

Power consumption is a critical factor when evaluating the performance of an integrated circuit design [1], [2], [5], [32]-[34]. The SA circuit must operate at high frequencies to support high-speed and continuous data access between the processor and memory. Compared to static power consumption, dynamic power consumption has a significantly larger value and is the main component affecting the total power consumption of integrated circuit designs [1], [34]. Generally, passive power consumption is influenced by factors such as the operating voltage (VDD), the distributed total design capacitance (C), and the design operating frequency (f) [1], [33]. The power consumption and access time of a SA design can be improved by reducing its distributed total capacitance. Minimizing total capacitance reduces the energy and time required

to charge and discharge the capacitors [1]. Even if the distributed total capacitance increases after optimizing the layout design process, dynamic power consumption may still decrease if C_DLL is equivalent to C_DLLB. Designing a symmetric capacitance SA with a C_DLL/C_DLLB ratio close to 100% can further reduce dynamic power consumption and delay time by reducing the offset voltage of the SA, which is the minimum voltage difference required to trigger its positive feedback loop [26]. Figure 7 illustrates the power dissipation of the LSA design at three different operating frequencies: 100 MHz, 500 MHz, and 1,000 MHz. In addition, the design is set to operate at a voltage of 1 V and an ambient temperature of 27 C. The bitline capacitance is also set to a value of 100 fF in this simulation. Three scenarios were investigated for measuring power consumption: without implementing layout for the design, with layout implementation, and with optimized layout design.

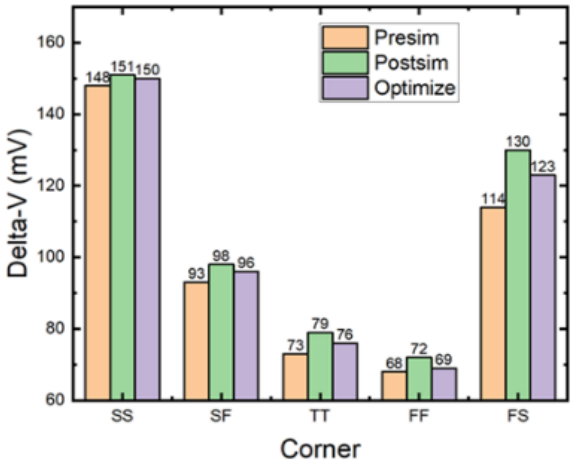

Figure 5. The Delta-V value of the LSA circuit was examined in three scenarios: before layout, after layout, and after optimizing the layout design for each specific process corner

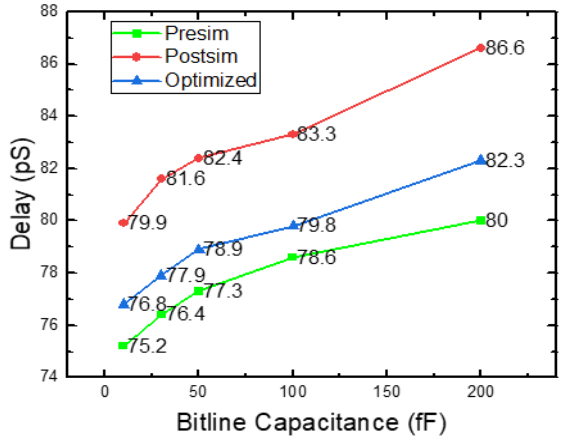

Figure 6. The examination involves three scenarios: one where the layout is not considered, another where the layout is taken into account, and a third where the layout design is optimized. The analysis focuses on the delay of the LSA circuit for different bit-line capacitance values

Analyzing the results from Figure 7 without considering the influence of parasitic capacitors in the design layout process (Presim), the dynamic power consumption of the LSA design reaches 310 nW at 1,000 MHz. After implementing the layout (Postsim) for the LSA design, the active power consumption increased by approximately 1.5 times, from 310 nW to 472 nW. However, by applying layout techniques (optimized) to reduce the parasitic capacitance in the design, the dynamic power consumption is reduced by approximately 15% from 472 nW to 401 nW. In summary, the SA circuit is crucial in determining the data access speed, power consumption, and reliability of SRAM memory designs. Physical factors, such as wire

resistance and parasitic capacitance that arise during layout implementation, significantly affect and reduce the overall design performance. Therefore, it is essential to consider and analyze post-layout elements to minimize differences in operation and performance before and after layout implementation. Achieving a balanced parasitic capacitance when implementing the SRAM memory layout significantly improves reliability, reduces memory access delay, and optimizes power consumption. Analysis results in this paper demonstrate that considering the influence of parasitic capacitance on the layout design can lead to a 15% improvement in overall design performance. In the subsequent research, we will optimize the layout considering parasitic capacitance and explore various methods to minimize power consumption in both the current mode sense amplifier (CMSA) and the voltage mode sense amplifier (VMSA). These investigations will be conducted using 14 nm and 12 nm CMOS technology. The goal is to identify the most effective solution for reducing power consumption and enhancing data access time in the design of SRAM circuits.

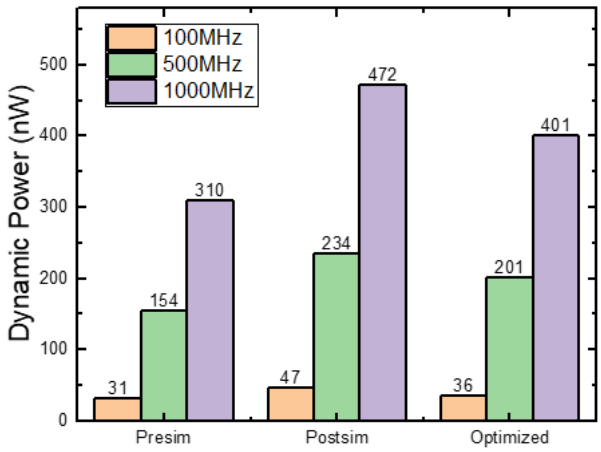

Figure 7. The examination involves three scenarios: one where the layout is not considered, another where the layout is taken into account, and a third where the layout design is optimized. The analysis focuses on the dynamic power consumption at different operating frequencies

5. CONCLUSION

SRAM technology is utilized in designing cache memory to enhance the processing performance of computer systems. The SA circuit, a crucial component of memory design, significantly impacts data access time and power consumption. In comparison to conventional differential SA designs, latch-based SA used in memory-based computing platforms have specific requirements, including robust noise resistance in harsh working environments and low power consumption, particularly for IoT embedded computing applications. This study employs low-voltage 22 nm UMC CMOS technology for LSA design layout and analyzes the factors influencing design performance post-layout process. Layout design optimization techniques are applied to mitigate the impact of parasitic capacitance on important signal lines such as DLL/DLLB. Based on the performance analysis results, it is possible to achieve a reduction in power consumption of up to 15% and a 5% decrease in read delay time by implementing circuit layout latch-based SA design optimization techniques.

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