Indonesian Journal of Electrical Engineering and Computer Science
Vol. 32, No. 3, December 2023, pp. 1378~1383
ISSN: 2502-4752, DOI: 10.11591/ijeecs.v32.i3.pp1378-1383

Field programmable gate array implementation of edge detection system based on an improved sobel edge detector

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Article Info

Article history:

Received Sep 1, 2023
Revised Sep 16, 2023
Accepted Oct 11, 2023

Keywords:

Algorithm for image processing
Design filter
Field-programmable gate array
Image edge detection
Image processing

ABSTRACT

Field programmable gate array (FPGA) is an integrated circuit consisting of internal hardware blocks with programmable link connections for users to customize operations for a particular application. Link connections can be easily reprogrammed, allowing the FPGA to adapt to changes to the design or even support a new application throughout the department's uptime. One of the important tasks in image processing is image edge detection image, with computer aided, image recognition is concerned with the recognition and classification of objects in an image, so edge detection is an important tool. In this paper, we design filter for edge detection in image processing using FPGA kit. We analysis and implementation of algorithm for image processing on FPGA, load the code and run the results. Comparative analysis with images processed by MATLAB software.

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1. INTRODUCTION

Image processing is a sub-discipline of digital signal processing where the processed signal is an image. This is a very developed new branch of science, image processing is increasingly popular and strongly developed with many practical applications in medicine, security, transportation, security systems, automation. Applications of image processing in medicine such as ultrasound, X-ray [1]–[7]. In security, it helps in motion detection and intrusion warning. In traffic, it helps to measure speed, warn of congestion, image edge detection is one of the important tasks in image processing. Image recognition with computer aided is concerned with the recognition and classification of objects in an image, so sobel edge detection is an important tool. Edge detection remove unnecessary information and will significantly reduce the amount of data to be processed while important structural properties of the image are preserved, this issue is mentioned and researched in [8]–[16].

Field programmable gate array (FPGA) is an integrated circuit that uses logical element array structure, FPGA has a fast-processing speed, which can provide low latency or defined latency for real time applications such as image and video processing by directly importing images or videos into the FPGA. FPGAs can also satisfy a variety of functions that provide high energy efficiency. An FPGA can use part of the FPGA for a function instead of the entire chip-allowing the FPGA to store or execute multiple functions in parallel [17]–[25].

In this paper, we design filter for edge detection in image processing using FPGA kit, we analysis and implementation of algorithm for image processing on FPGA. The remainder of the paper is organized as follows. In section 2, digital image filter methods are described. In section 3, we present the filter design. The numerical results and discussions are presented in section 4, and finally, we conclude the paper in section 5.

2. DIGITAL IMAGE FILTER METHODS

2.1. Edge detection

Edge detection is an technique to determine the boundaries of objects within images by detecting discontinuities of brightness, and it is an important tool in digital image processing, it is used for image segmentation and extraction of data. It significantly reduces the amount of data to be calculated, retaining only a handful of necessary information while preserving the critical structures in the image [2]. The boundary point is where adjacent pixels have a sudden change in intensity as shown in Figure 1, there are some types of borders is shown in Figure 1(a)-1(d). Borderline is a typical type of local characteristic in analysis, image recognition and helps segment the areas in the image [9].

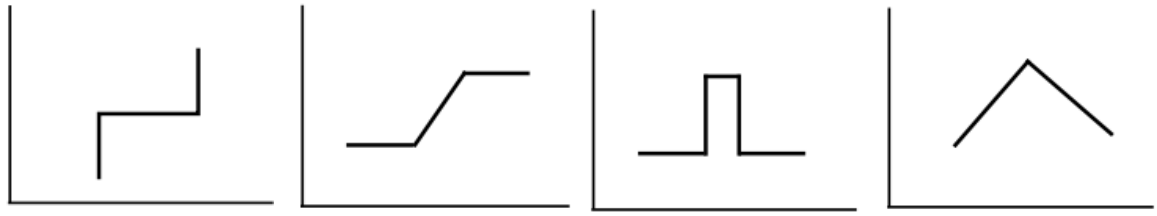


Figure 1. Some types of borders: (a) step jump profile, (b) steep borders, (c) Square pulse borderline, and (d) cone border

2.2. The methods of edge detection

There are many methods of boundary detection being applied, but we can be divided into two basic groups: gradient detection and Laplacian method. Gradient detection method (using operator: Roberts, Prewitt, Sobel, Canny) is based on the maximum and maximum value of the image's top function. The Laplacian method will look for points of value 0 when taking the second-order derivative of the image [14].

Gradient-based methods, the core of gradient edge detection is, of course, the gradient operator, the first-order derivative in the horizontal and vertical direction is calculated and given by [15]:

$$\Delta f = \begin{bmatrix} G_x \\ G_y \end{bmatrix} = \begin{bmatrix} \frac{\partial f}{\partial x} \\ \frac{\partial f}{\partial y} \end{bmatrix} \quad (1)$$

to produce an edge detector, one may simply extend the case described earlier, the amplitude of the vector gradient or the total magnitude of the derivative value located at the boundary is a combination of both of these values according to the formula.

$$\Delta f = |\Delta f| = \sqrt{G_x^2 + G_y^2} \quad (2)$$

The direction of the vector gradient is angle of Δf , and is determined by (3). The direction of the boundary will be perpendicular to the direction of this vector gradient, the angle is expressed under the tang angle as follows:

$$\text{angle of } \Delta f = \tan^{-1}\left(\frac{G_y}{G_x}\right) \quad (3)$$

the gradient method is only suitable for variable contrast image areas that are leap fly, which makes it difficult to detect straight lines. To overcome this weakness, we often use a second-order derivative. Laplacian method for [15].

$$L(x,y) = \frac{\partial^2 I}{\partial x^2} + \frac{\partial^2 I}{\partial y^2} \quad (4)$$

Laplacian is combined with a photo smoothing filter to find the edge. If this function is performed with a picture to look for the edge, the result is that the image will be blurred, the degree of blurring depends on the value of the image. Laplacian of h i.e., order derivative of h according to r is given by [15].

$$\Delta^2 h(r) = -\left[\frac{r^2-\sigma^2}{\sigma^4}\right] \exp\left(\frac{r^2}{2\sigma^2}\right) \quad (5)$$

In this method, the Gaussian filter is combined with Laplacian which allows the display of areas of rapidly changing image that increases the efficiency of marginal detection. It allows working with a wider area around the pixel being studied to more accurately detect the location of the boundary. The downside of this method is that the direction of the margin is not determined due to the use of two too different Laplacian filters.

2.3. Virtex-7 FPGA KIT

The Virtex-7 FPGA VC707 rating toolkit is a high-speed, flexible, fully functional serial platform of the Virtex-7 XC7VX485T-2FFG1761C, the board of Virtex-7 FPGA VC707 is shown in Figure 2. It includes the basic components of hardware, design tools, IP and preverified references designed for system designs that require high performance, serial connection and advanced memory communication. Pre-verified reference designs come with and FPGA (FMC) industry standards allow for expansion and customization with sub cards.

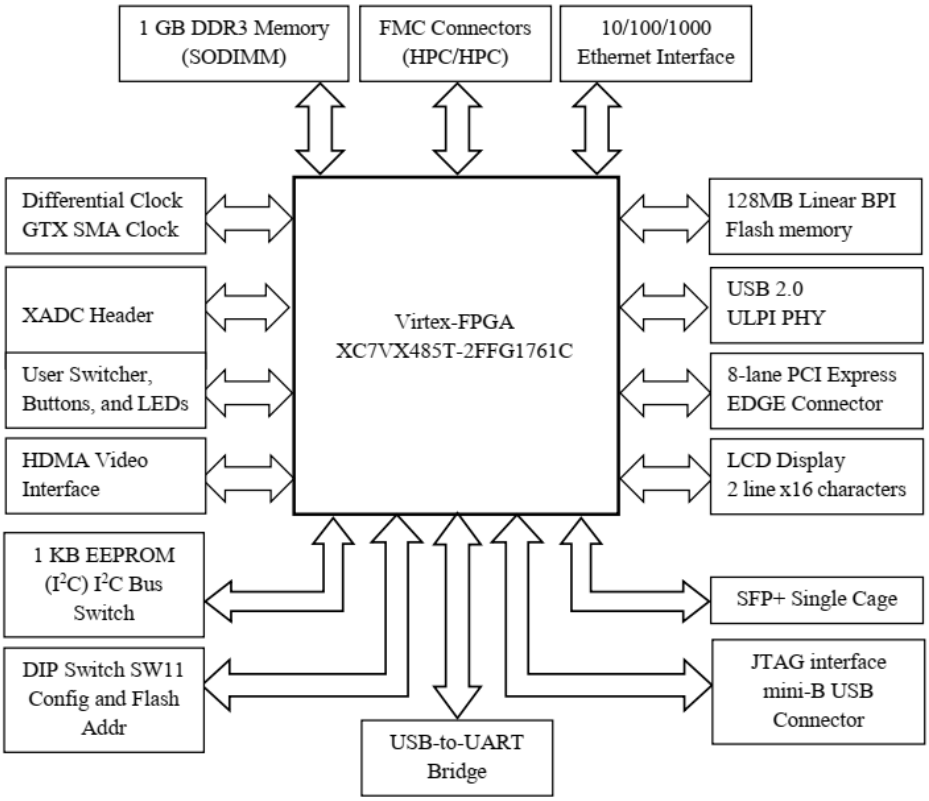


Figure 2. Board Virtex-7 VC707

The features of Virtex-7 FPGA VC707; 40Gb/s connectivity platform for high performance and high bandwidth applications using Virtex-7 VX485T FPGA; desigh tools, hardware, internet protocol and preverified reference designs; embedded processing support with RISC 32bit, Micro Blaze. It allows serial connections to SFP+ and SMA, PCIe Gen2x8, IIC pairs, UART; Advanced memory interface with 1GB DDR3 SODIM Memory up to 800 MHz/1600 Mbps; expand I/O with FPGA mezzanine card (FMC) interface. And it can develop network applications with 10 Mbps, 100 Mbps, 1000 Mbps Ethernet (GMII, RGMII, and SGMII).

3. FILTER DESIGN

3.1. Sobel edge detector

Use two masks of size [3 x 3] where one is simply the rotation of the other by 90 degrees. These masks are designed to best outline the vertical and horizontal borders, when performing convolution between the image and these masks, we get vertical and horizontal gradients Gx, Gy. The gradient of image is a directional change of color or intensity in an image and that is one of the basic building blocks in image processing:

$$\begin{bmatrix}+1\\+2\\+1\end{bmatrix} \times [+1 \quad 0 \quad +1] \rightarrow \begin{bmatrix}+1 & 0 & -1\\+2 & 0 & -2\\+1 & 0 & -1\end{bmatrix} \text{and} \begin{bmatrix}+1\\0\\-1\end{bmatrix} \times [+1 \quad +2 \quad +1] \rightarrow \begin{bmatrix}+1 & +2 & +1\\0 & 0 & 0\\-1 & -2 & -1\end{bmatrix} \tag{6}$$

$$G_x = \begin{bmatrix}+1 & 0 & -1\\+2 & 0 & -2\\+1 & 0 & -1\end{bmatrix} * A \text{ and } G_y = \begin{bmatrix}+1 & +2 & +1\\0 & 0 & 0\\-1 & -2 & -1\end{bmatrix} * A \tag{7}$$

add the last result together.

$$B = (A * G_x) + (A * G_y) \tag{8}$$

3.2. Line buffer

The line buffer is shown in Figure 3, an image is composed of 512*512 pixels, that width is 512 and height is 512. With using FPGA for image processing, the pixel rows is cached and transformed in internal storage resources of FPGA, it is often necessary to open a window for the image. We design a 3-line cache for [3 x 3] window, the data of the most of image are row by row, first from left to right, and then from top to bottom output each pixel data. If we don't add processing, then we can't get the [3 x 3] image window, ultimate goal should be to make three lines of data, it is aligned and output at the same time, and then can get the [3 x 3] window of image.

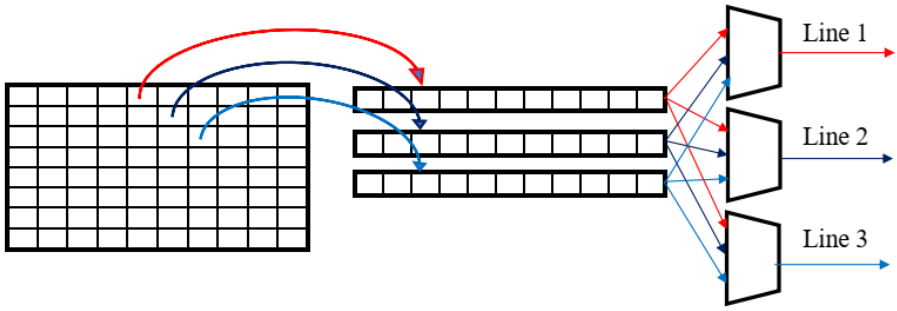
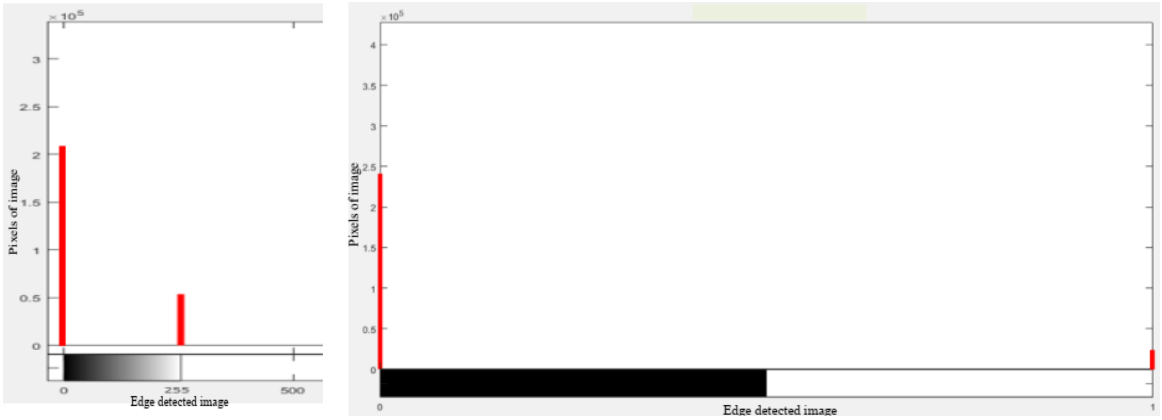


Figure 3. Line buffer

In order, we need 3 FIFOs that to implement 3-Line cache, as shown in the Figure 3. Enter the first line (Line 1) of data in turn and write in to FIFO1. When the last data in the Line 1 is written, proceed to read the data from FIFO1 in turn, then write in to FIFO2. In this way, when the fourth line (Line 4) of data arrives, the three FIFOs will output data at the same time, and the output data of the three line (Line 3) is aligned.

4. RESULTS AND DISCUSSION

Using board of Virtex-7 FPGA VC707 (Figure 2) and perform edge detection with a grayscale image with Width of 512px and Height of 512px, a pixel count of 512′ 512 equals 262,144 pixels. Then in these 262,144 pixels, there will be pixels with the same gray intensity. Let's say the bit range of that image is from 0 to 255, and bit 0 has 100 identical pixels, and bit 1 has 150 pixels. up to bit 255 is N identical pixels. And the sum of the pixels of these bits will be 262,144. Figure 4, illustrates the edge detection, with using Virtex-7 FPGA VC707 is shown in Figure 4(a) and using MATLAB is shown in Figure 4(b). As it is clearly shown, edge detection with Virtex-7 FPGA VC707 shows more detailed edges than MATLAB software.



(a) (b)

Figure 4. Histogram edge detection (a) edge detection FPGA and (b) edge detection MATLAB

5. CONCLUSION

In this paper, we have presented FPGA implementation of edge detection system based on an improved Sobel edge detector. Design edge detection by FPGA to improve image processing speed and capacity and reduce intermediate process, the algorithm is mapped onto a Xilinx Virtex-7 FPGA platform. The proposed FPGA implementation takes only 0.721ms, including the SRAM read/write time and the computation time to detect edges of 512×512 images in the USC SIPI database when clocked at 50 MHz. Thus, the proposed implementation is capable of supporting fast real-time edge detection of images.

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