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Advances on CMOS Shift Registers for Digital Data Storage

Mohammad Arif Sobhan Bhuiyan*, Hasrul Nisham Bin Rosly, Mamun bin Ibne Reaz, Khairun Nisa Minhad, Hafizah Husain
Department of Electrical, Electronic and Systems Engineering, Universiti Kebangsaan Malaysia, 43600, Bangi, Selangor, Malaysia
*Corresponding author, e-mail: md.arif.sobhan@gmail.com

Abstract

The shift register is the heart of the current digital data storage system. Current trends of wireless device designs are to balance the power consumption, cost and portability of the device. The worldwide research is giving emphasize on increasing the amount of memory at minimum possible space to reduce the overall size of the devices now a days. This paper reports a detailed survey on different types of shift registers in CMOS technology from the performance, design and application point of view. It also discusses the technologies available for the design of shift registers with their merits and demerits. This survey will act as a reference for the scientists to design the high-performance memory module.

Keywords*: shift registers, digital storage, dynamic CMOS, static CMOS*

1. Introduction

A shift register is a digital data storage. The data can be the letters to be displayed on a TV screen, numbers in a computer or calculator, intermediate values in a digital filter or part of an elaborate code or sequence. Shift registers are made up of individual stages. Each stage can store one bit of information, called a binary 1 or a 0, and usually corresponding to a "yes" or "no" or else perhaps a "present" or "absent" command. Four bits together can represent a decimal number, while six bits together can handle one ASCII character, and so on. In a shift register, the contents can be moved or shifted so that the contained information is marched one and only one stage at a time through the device. The shifting process is called clocking and one or more clocks can be involved in completing the shifting operation.

During the early days, shift registers with many stages were used for memories of computer and other electronics gazettes [1-3]. Usages of shift registers substituted mercury delay lines, speeding up data processing and allowing for smaller computer components and peripherals [4]. Today, shift registers are considered antiquated as primary memories for computers and other electronic devices. Circuit boards, however, still feature shift registers to reduce the amount of wiring needed, especially in display drivers, digital to analog converters, and serial data memory [5].

As applied to digital circuits, a shift register is a series of flip-flops based on sequential clock timing. The flip-flops facilitate moving data from input to output using sequential logic. A clock, in the form of a repeating wave in a square pattern, is used to synchronize how data travels through shift registers, creating a short delay in the transmission of a digital signal [6]. Most often, shift registers of varying lengths are used to convert parallel data to serial [7], but may also be used for data flow in microprocessors or to covert analog data to digital and vice versa [8, 9].

Shift registers are high-speed circuits [7]. Primarily, a shift register moves bits of data either left or right along a circuit, depending on structure and design of the circuit. In its simplest form, a shift register takes data in at the first stage and shifts bits one stage left or right as the clock signals are needed for a data advance. Registers are identified by the number of temporary storage slots available after each stage between input and output [10]. Temporary storage slots allow a shift register to delay data signals until the clock signals approve data

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advance. An 8-bit register, for example, has eight stages and thus eight temporary storage slots for bits in a data string.

Shift Registers are usually used for data storage or data movement in calculators, computers and other electronic devices such as two binary numbers before they are added together or to convert the data from either a serial to parallel or parallel to serial format [11]. Serial data over shorter distances of tens of centimeters, uses shift registers to get data into and out of microprocessors. Numerous peripherals, including analog to digital converters, digital to analog converters, display drivers, and memory (digital storage), use shift registers to reduce the amount of wiring in circuit boards. Some specialized counter circuits actually use shift registers to generate repeating waveforms. Longer shift registers, with the help of feedback generate patterns so long that they look like random noise, pseudo-noise. The individual data latches that make up a single shift register are all driven by a common clock (Clk) signal making them synchronous devices. Shift register IC's are generally provided with a clear or reset connection so that they can be "SET" or "RESET" as required.

Instead of using memory elements in a sequential system, dynamic logic circuits can be used to store temporary data in different devices [12-16]. In a dynamic shift register, storage is accomplished by continually shifting the bits from one stage to the next and re-circulating the output of the last stage into the first stage [17]. The data continually circulates through the register under the control of clock. To obtain output, a serial output terminal must be accessed at a specific clock pulse; otherwise, the sequence of bits will not correspond to the data stored.

This paper presents a detailed discussion on shift registers for different applications from their architecture and performance point of view. The basics of shift registers and their operations are also discussed. The technologies available for shift registers along with their merits and demerits are also included in this review. This review will help the scientists to have basic as well as advanced knowledge on shift registers for their future researches.

2. Shift Registers and Classifications

Each flip-flop is a binary cell capable of storing one bit of information [18]. A Register is simply a group of flip-flops. An n-bit register has a group of n flip-flops. The basic function of a register is to hold information within a digital system so as to make it available to the logic elements during the computing process. Since a register consist a finite number of flip-flops and as each of those flip-flops is capable to store a single 0 or 1, there are a finite number of 0-1 combinations that can be stored into a register. Each of those combinations is known as state or content of that register [19]. With flip-flops we can store data bitwise but usually data does not appear as single bits. Instead it is common to store data words of n bit with typical word lengths of 4, 8, 16, 32 or even 64 bits. Thus, several flip-flops are combined to form a register to store whole data words. Registers are synchronous circuits thus all flip-flops are controlled by a common clock line [18].

The Shift Register is one type of sequential logic circuit that is used to store or transfer data in the form of binary numbers and then "shifts" the data out once every clock cycle [20]. It basically consists of several single bit "D-Type Data Latches", one for each bit (0 or 1) connected together in a serial or daisy-chain arrangement so that the output from one data latch becomes the input of the next latch and so on. The data bits may be fed in or out of the register serially, i.e. one after the other from either the left or the right direction, or in parallel, i.e. all together. The number of individual data latches required to make up a single Shift Register is determined by the number of bits to be stored.

Generally, shift registers operate in one of the four different modes [20], they are:

1. Serial-in to Parallel-out (SIPO) - The register is loaded with serial data, one bit at a time, with the stored data being available in parallel form.
2. Serial-in to Serial-out (SISO) - The data is shifted serially "IN" and "OUT" of the register, one bit at a time in either a left or right direction under clock control.
3. Parallel-in to Serial-out (PISO) - The parallel data is loaded into the register simultaneously and is shifted out of the register serially one bit at a time under clock control.
4. Parallel-in to Parallel-out (PIPO) - The parallel data is loaded simultaneously into the register, and transferred together to their respective outputs by the same clock pulse.

The data movement from left to right through a shift register in different modes is graphically illustrated in Figure 1.

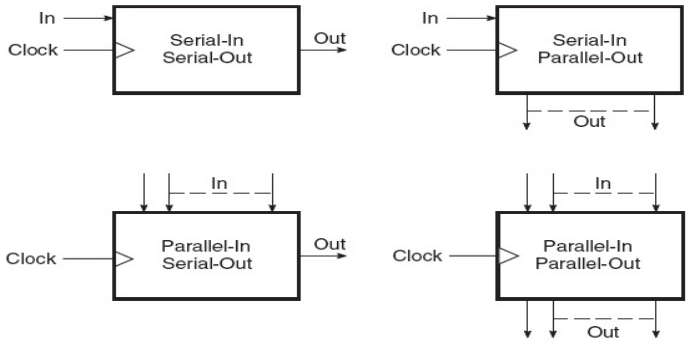

Figure 1. Shift Register in Different Modes

2.1. Serial-in to Parallel-out (SIPO)

Figure 2 shows a 4-bit Serial-in to Parallel-out Shift Register. Assume that all the flip-flops (FFA to FFD) have just been RESET (CLEAR input) and that all the outputs QA to QD are at logic level "0" i.e., no parallel data output. If a logic "1" is connected to the DATA input pin of FFA then on the first clock pulse the output of FFA and therefore the resulting QA will be set HIGH to logic "1" with all the other outputs still remaining LOW at logic "0". Assume now that the DATA input pin of FFA has returned LOW again to logic "0" giving us one data pulse or 0-1-0.

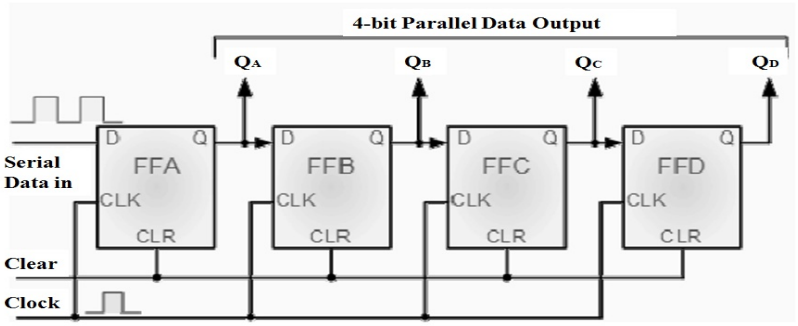

Figure 2. 4-bit Serial-in to Parallel-out Shift Register

The second clock pulse will change the output of FFA to logic "0" and the output of FFB and QB HIGH to logic "1" as its input D has the logic "1" level on it from QA. The logic "1" has now moved or been "shifted" one place along the register to the right as it is now at QA. When the third clock pulse arrives this logic "1" value moves to the output of FFC (QC) and so on until the arrival of the fifth clock pulse which sets all the outputs QA to QD back again to logic level "0" because the input to FFA has remained constant at logic level "0".

Table 1. Basic Movement of Data through a Shift Register

Clock Pulse No	QA	QB	QC	QD
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	0	0	0	1
5	0	0	0	0

The effect of each clock pulse is to shift the data contents of each stage one place to the right, and this is shown in the following table until the complete data value of 0-0-0-1 is stored in the register. This data value can now be read directly from the outputs of QA to QD. Then the data has been converted from a serial data input signal to a parallel data output. The

truth table, shown in Table 1, shows the propagation of the logic "1" through the register from left to right with clock pulses.

It is clear that after the fourth clock pulse, the 4-bits of data (0-0-0-1) are stored in the register and will remain there provided clocking of the register has stopped. In practice the input data to the register may consist of various combinations of logic "1" and "0". The practical application of the serial-in/parallel-out shift register is to convert data from serial format on a single wire to parallel format on multiple wires for example to illuminate LEDs (Light Emitting Diodes).

2.2. Serial-in to Serial-out (SISO)

This shift register is very similar to the SIPO above, except that the data was read directly in a parallel form from the outputs QA to QD. In this circuit, data are allowed to flow through the register and out of the other end. Since there is only one output, the data leaves the shift register one bit at a time in a serial pattern, hence the name Serial-in to Serial-Out Shift Register or SISO.

The SISO configuration is one of the simplest structures of the shift registers as it has only three connections, the serial input (SI) which determines what enters the left hand flip-flop, the serial output (SO) which is taken from the output of the right hand flip-flop and the sequencing clock signal (Clk). Figure 3 shows a generalized 4 bit serial-in serial-out shift register.

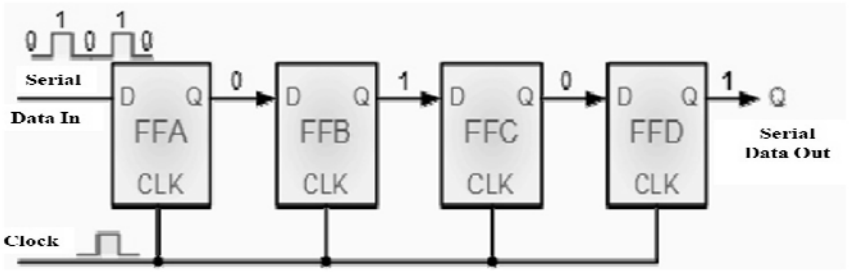

Figure 3. 4-bit Serial-in to Serial-out Shift Register

SISO is the type of Shift Register that acts as a temporary storage device or as a time delay device for the data, with the amount of time delay being controlled by the number of stages in the register, 4, 8, 16 etc or by varying the application of the clock pulses [21].

2.3. Parallel-in to Serial-out (PISO)

The Parallel-in to Serial-out shift register acts in the opposite way to the serial-in to parallel-out configuration. The data is loaded into the register in a parallel format i.e. all the data bits enter their inputs simultaneously, to the parallel input pins PA to PD of the register. The data is then read out sequentially in the normal shift-right mode from the register at Q representing the data present at PA to PD. This output data is transferred one bit at a time on each clock cycle in a serial format. It is important to note that with this system a clock pulse is not required to parallel load the register as it is already present, but four clock pulses are required to unload the data. Figure 4 shows a typical 4 bit Parallel-in serial-out shift register.

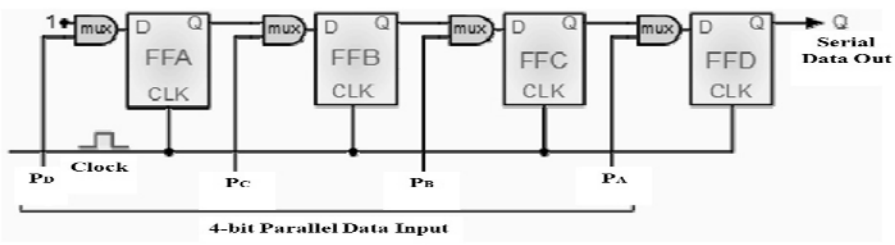

Figure 4. 4-bit Parallel-in to Serial-out Shift Register

As this type of shift register converts parallel data, such as an 8-bit data word into serial format, it can be used to multiplex many different input lines into a single serial data stream which can be sent directly to a computer or transmitted over a communications line [22].

2.4. Parallel-in to Parallel-out (PIPO)

The final mode of operation is the Parallel-in to Parallel-out Shift Register. This type of register also acts as a temporary storage device or as a time delay device similar to the SISO configuration [20]. The data is presented in a parallel format to the parallel input pins PA to PD and then transferred together directly to their respective output pins QA to QD by the same clock pulse. Then one clock pulse loads and unloads the register. This arrangement for parallel loading and unloading is shown in Figure 5.

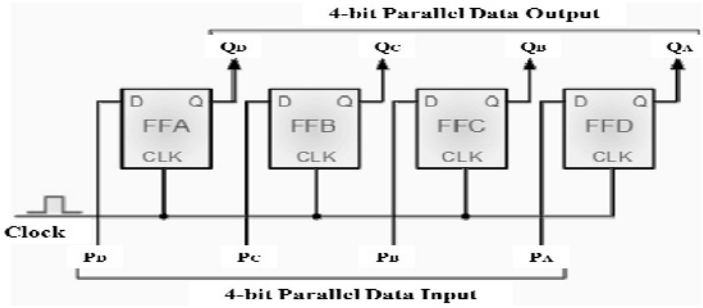

Figure 5. 4-bit Parallel-in to Parallel-out Shift Register

The PIPO shift register is the simplest of the four configurations as it has only three connections, the parallel input (PI) which determines what enters the flip-flop, the parallel output (PO) and the sequencing clock signal (Clk). Similar to the Serial-in to Serial-out shift register, this type of register also acts as a temporary storage device or as a time delay device, with the amount of time delay being varied by the frequency of the clock pulses. Also, in this type of register there are no interconnections between the individual flip-flops since no serial shifting of the data is required.

2.5. Bidirectional Shift Registers

The registers discussed so far involved only right shift operations. Each right shift operation has the effect of successively dividing the binary number by two. If the operation is reversed (left shift), this has the effect of multiplying the number by two. With suitable gating arrangement a serial shift register can perform both operations. A bidirectional, or reversible, shift register is one in which the data can be shift either left or right [23]. A four-bit bidirectional shift register using D flip-flops is shown Figure 6.

Here a set of NAND gates are configured as OR gates to select data inputs from the right or left adjacent bistables, as selected by the LEFT/RIGHT control line.

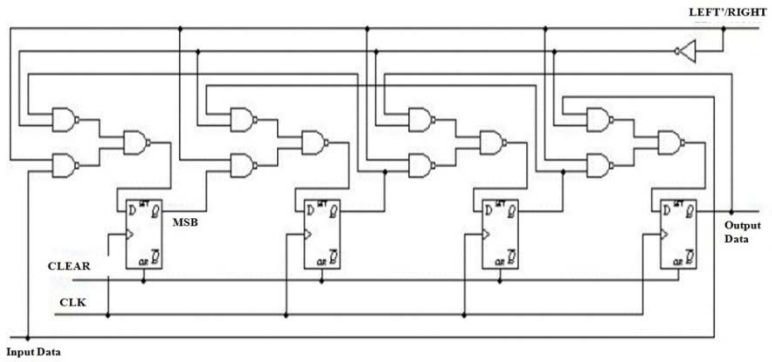

Figure 6. 4-bit Bidirectional Shift Register

3. CMOS Shift Registers

The rapid down-scale in CMOS technology has advanced the research in almost all areas of microelectronics [24-28]. CMOS inverters (Complementary MOSFET Inverters) are some of the most widely used and adaptable MOSFET inverters used in chip design [29]. They operate with very little power loss and at relatively high speed [30]. Furthermore, the CMOS inverter has good logic buffer characteristics, in that, its noise margins in both low and high states are large. This short description of CMOS inverters gives a basic understanding of the how a CMOS inverter works. It will cover input/output characteristics, MOSFET states at different input voltages, and power losses due to electrical current.

A CMOS inverter contains a PMOS and a NMOS transistor connected at the drain and gate terminals, a supply voltage Vdd at the PMOS source terminal, and a ground connected at the NMOS source terminal, were Vin is connected to the gate terminals and Vout is connected to the drain terminals (Figure 7). It is important to notice that the CMOS does not contain any resistors, which makes it more power efficient that a regular resistor-MOSFET inverter [31]. As the voltage at the input of the CMOS device varies between 0 and 5 volts, the state of the NMOS and PMOS varies accordingly.

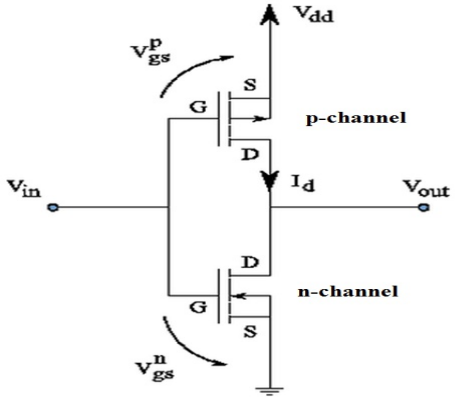

Figure 7. Schematic of a CMOS Inverter Circuit

3.1. Transistor Switch Model

The switch model of the MOSFET transistor is defined as Table 2.

Table 2. Condition and State of MOSFET Transistor Switch Model

MOSFET	Condition on MOSFET	State of MOSFET
NMOS	Vgs < Vtn	OFF
NMOS	Vgs < Vtn	ON
PMOS	Vsg < Vtp	OFF
PMOS	Vsg < Vtp	ON

When V_{in} is low, the NMOS is "off", while the PMOS stays "on": instantly charging V_{out} to logic high. When V_{in} is high, the NMOS is "on and the PMOS is "on: draining the voltage at V_{out} to logic low.

This model of the CMOS inverter helps to describe the inverter conceptually, but does not accurately describe the voltage transfer characteristics to any extent. A more full description employs more calculations and more device states.

3.2. Multiple State Transistor Model

The multiple state transistor model is a very accurate way to model the CMOS inverter [32]. It reduces the states of the MOSFET into three modes of operation: Cut-Off, Linear, and Saturated: each of which have a different dependence on V_{GS} and V_{DS}. The formulas which govern the state and the current in that given state is given by Table 3.

Table 3. NMOS and PMOS Mode of Operation

NMOS Characteristics	Condition on V_{GS}	Condition on V_{DS}	Mode of Operation
ID = 0	VGS < VTN	ALL	Cut-off
ID = KN [2 (VGS-VTN)VDS - VDS^2]	VGS > VTN	VDS<VGS-VTN	Linear
ID = KN (VGS – VTN)^2	$V_{GS} > V_{TN}$	$V_{DS}>V_{GS}-V_{TN}$	Saturated
PMOS Characteristics	**Condition on V_{SP}**	**Condition on V_{SD}**	**Mode of Operation**
ID = 0	VSG < -VTP	ALL	Cut-off
ID = KP [2 (VSG-VTP)VSD - VSD^2]	VSG > VTP	VSD<VSG+VTP	Linear
ID = KP (VSG – VTP)^2	$V_{SG} > -V_{TP}$	$V_{SD}>V_{SG}+V_{TP}$	Saturated

3.3. Pass Transistor Logic

A popular and widely used alternative to complementary CMOS is pass transistor logic. Pass transistor logic attempts to reduce the number of transistors required to implement logic by allowing the primary inputs to drive gate terminals as well as source/drain terminals [33]. This is in contrast to logic families that only allow primary inputs to drive the gate terminals of MOSFETS. Figure 8 shows a transistor level implementation of the AND function constructed using NMOS transistors. In this gate, if the B input is high, the top transistor is turned on and copies the input A to the output F. When input B is low, the bottom pass transistor is turned on and passes a 0. The switch driven by B seems to be redundant at first glance. Its presence is essential to ensure that a low-impedance path exists to the supply rails under all circumstances, or, in this particular case, when B is low.

The potential advantage of pass transistor is that a fewer number of transistors are required to implement a given function. Pass transistor logic uses fewer devices and therefore has lower physical capacitance [34]. Unfortunately, a NMOS device is effective at passing a 0 but is poor at pulling a node to V_{DD}. In pass transistor logic, the pass transistors are used to pass high and low voltages. Therefore, when the pass transistor pulls a node high, the output only charges up to V_{DD} -VTn. In fact, the situation is worsened by the fact that the devices experience body effect since there is a significant source to body voltage when pulling high since the body is tied to GND and the source charge up close to V_{DD}.

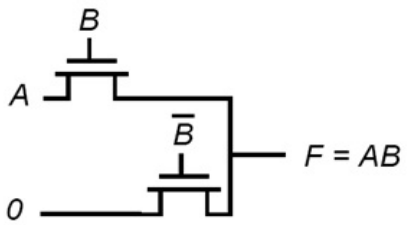

Figure 8. Pass Transistor Implementation of an AND Gate

3.4. Static CMOS Design

The most widely used logic style is static complementary CMOS [35]. The static CMOS style is really an extension of the CMOS inverter to multiple inputs. In review, the primary advantage of the CMOS structure is robustness (i.e, low sensitivity to noise), good performance, and low power consumption (with no static power consumption) [36]. Therefore, most of those properties are carried over to large fan-in logic gates implemented using the same circuit topology. The complementary CMOS circuit style falls under a broad class of logic circuits called static circuits in which at every point in time (except during the switching transients), each gate output is connected to either V_{DD} or V_{SS} via a low-resistance path. Also, the outputs of the gates assume at all times the value of the Boolean function implemented by the circuit [37] (ignoring, once again, the transient effects during switching periods). This is in contrast to the dynamic circuit class that relies on temporary storage of signal values on the capacitance of high-impedance circuit nodes. The latter approach has the advantage that the resulting gate is simpler and faster. On the other hand, its design and operation are more involved than those of its static counterpart, due to an increased sensitivity to noise.

A static CMOS gate is a combination of two networks, called the pull-up network (PUN) and the pull-down network (PDN) [38] as shown in Figure 9. This shows a generic N input logic gate where all inputs are distributed to both the pull-up and pull-down networks. The function of the PUN is to provide a connection between the output and V_{DD} anytime the output of the logic gate is meant to be 1 (based on the inputs). Similarly, the function of the PDN is to connect the output to V_{SS} when the output of the logic gate is meant to be 0. The PUN and PDN networks are constructed in a mutually exclusive fashion such that "one and only one" of the networks is conducting in steady state [39]. In this way, once the transients have settled, a path always exists between V_{DD} and the output F, realizing a high output ("one"), or, alternatively, between VSS and F for a low output ("zero"). This is equivalent to stating that the output node is always a low-impedance node in steady state [40].

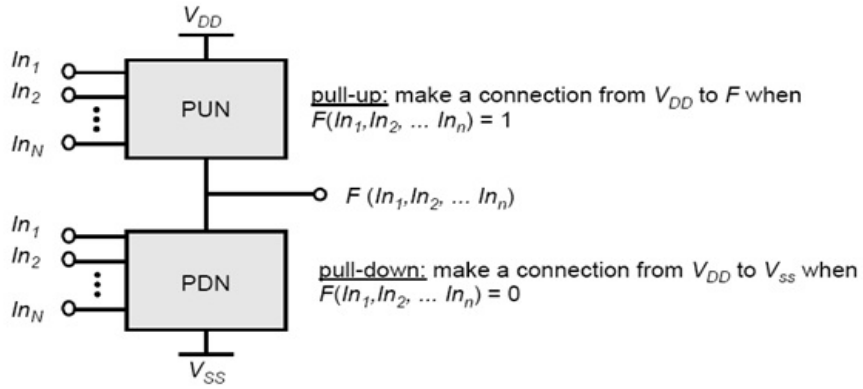

Figure 9. Complementary Logic Gate as a Combination of a PUN (pull-up network) and a PDN (pull-down network)

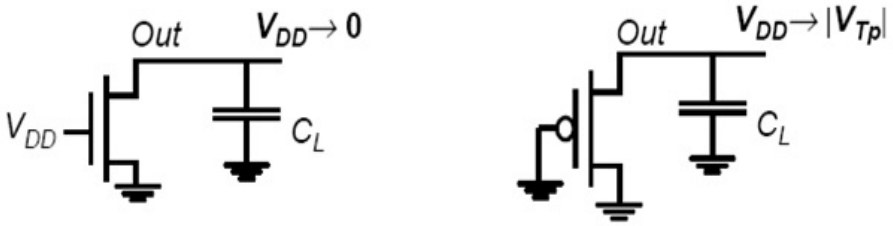

Figure 10. Pulling Down a Node using NMOS and PMOS Switches

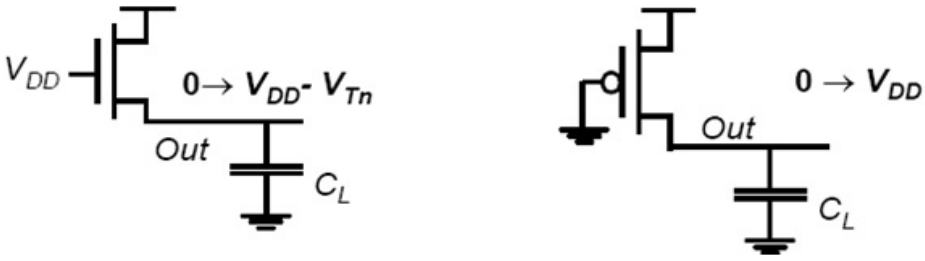

Figure 11. Pulling up a Node using NMOS and PMOS Switches

A transistor can be considered as a switch controlled by its gate signal [41]. An NMOS switch is on when the controlling signal is high and is off when the controlling signal is low. A PMOS transistor acts as an inverse switch that is on when the controlling signal is low and off when the controlling signal is high. The PDN is constructed using NMOS devices, while PMOS transistors are used in the PUN. The primary reason for this choice is that NMOS transistors produce "strong zeros," and PMOS devices generate "strong ones". To illustrate this, consider

the examples shown in Figure 10 and Figure 11. In Figure 10, the output capacitance is initially charged to V_{DD}. Two possible discharge scenario's are shown. An NMOS device pulls the output all the way down to GND, while a PMOS lowers the output no further than $|V_{Tp}|$, the PMOS turns off at that point, and stops contributing discharge current. NMOS transistors are hence the preferred devices in the PDN. Similarly, two alternative approaches to charging up a capacitor are shown in Figure 11, with the output load initially at GND. A PMOS switch succeeds in charging the output all the way to V_{DD}, while the NMOS device fails to raise the output above V_{DD}-V_{Tn}. This explains why PMOS transistors are preferentially used in a PUN.

3.5. Dynamic MOS Design

The dynamic storage mechanism is widely used for momentary storage of data in digital circuits [42]. Among the technologies widely used for digital design, MOS technology provides two unusual features that lead to particularly efficient way to store data momentarily. These two features are the MOS transistor's extremely high input resistance and the ability of an MOS transistor to function as a nearly ideal electrical switch. The circuit combination of these features with the source terminal of one MOS transistor connected to the gate terminal of a second MOS transistor allows electrical charge to be stored momentarily on or removed from the gate terminal of the second transistor [43].

The three circuits of Figure 12, 13, 14 show typical circuit configurations used to achieve dynamic charge storage. The pass transistor and transmission gate devices are often designed with the minimum size transistor to reduce layout area. Figure 12 is useful with NMOS circuit, while the other two examples from CMOS circuits.

Operation of the circuit of Figure 12 depends on whether the pass transistor is off or on. If the pass transistor is at a high logic voltage, then the pass transistor conducts. In this case, the gate terminal of the inverter input transistor will be charged or discharged according to the logic voltage at the input to the pass transistor. The time required to charge or discharge the gate terminal will depend on the gate capacitance, the pass transistor resistance, and the signal source. The gate can be discharged to 0 V, or can be charged to $V_{DD} - V_{TN}$. This sets the gate terminal to either logic 0 or logic 1 value, respectively. Because the inverter input voltage range has been reduce from the normal range of V_L to V_{DD} to a smaller range of V_L to $V_{DD} - V_{TN}$ by the pass transistor, the switching threshold voltage V_M should be lowered by increasing the inverter sizing ratio *k* from 4 to about 8.

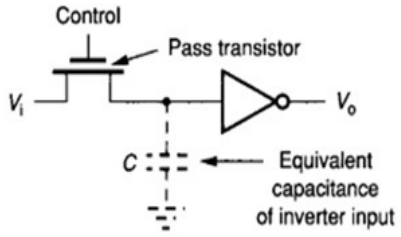

Figure 12. NMOS Dynamic Storage Circuit

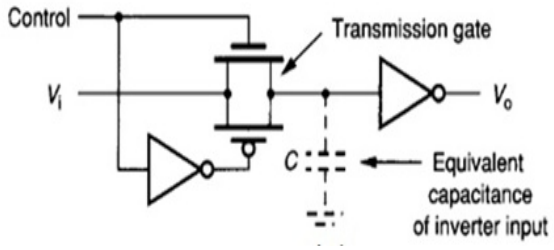

Figure 13. CMOS Dynamic Storage Circuit

When the gate of the pass transistor is at logic low voltage, the pass transistor is off, thereby isolating any charge on the gate capacitance of the inverter input transistor. This charge (or the lack thereof) represents the stored logic value. If the stored charge were perfectly isolated, the logic value would be store indefinitely. However, the isolation is less than perfect, primarily because of leakage through the reverse-biased diode created between the pass transistor source diffusion and the substrate [35]. Leakage also occurs through the pass transistor switch. Because the stored charge will leak away over time, this circuit is termed a dynamic storage circuit. For dynamic storage with present MOS devices, the primary charge leakage path occurs through the diode between source diffusion and the substrate. As MOS processes are created with linearly scaled-down devices, sub-threshold leakage through the pass transistor's channel will become the predominant leakage factor.

Dynamic storage can be implemented in CMOS by replacing the pass transistor with transmission gate, as shown in Figure 13. Note the increase in circuit complexity caused by the addition of p-channel transistor in the transmission gate and the requirement for a dual-polarity control signal. The situation can be alleviated somewhat with the circuit of Figure 14 in this circuit, called a level-restoring inverter; n-channel pass transistor is followed by a special inverter with a weak p-channel feedback transistor to restore the logic high level. The p-channel transistor must be sized to have an equivalent resistance much greater than the series pull-down resistance of the pass transistor and any circuit that drives the pass transistor input. The pass transistor can discharge the inverter gate to 0 V to give a good low logic level. In this case, the inverter output is high and the p-channel feedback transistor is off. As explained earlier, an n-channel pass transistor cannot raise the voltage high enough to ensure that the p-channel transistor of the inverter is off. Nevertheless, the pass transistor can pull the inverter input high enough to force the inverter's output to a low logic voltage. This low voltage turns on the p-channel feedback transistor, thereby pulling the inverter input to the upper supply voltage and holding it there.

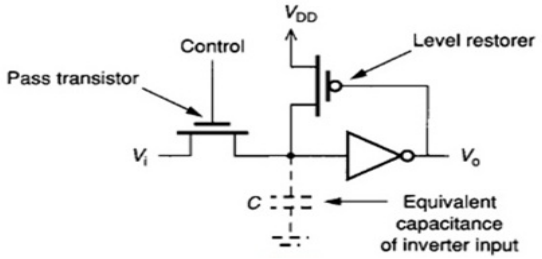

Figure 14. CMOS Pass Transistor Storage Circuit with Level Restoration

Dynamic storage is widely used within MOS circuits because of the simplicity of the required circuitry [44]. The NMOS version of figure 12 requires only three transistors, while the CMOS version of Figure 14 requires just four transistors. Thus, dynamic storage is area-efficient compared to the static storage circuits. A frequent use of dynamic storage circuits is to create shift registers [45]. The following discussion shows shift registers that are built upon a generic MOS dynamic storage stage consisting of a pass transistor and a simple inverter for NMOS or a level-restoring inverter for CMOS.

3.6. Dynamic VS Static

Dynamic and static storage are part of digital storage:

a. Dynamic Storage: This type of storage device allows the user to work within the storage device, making changes while working within the file, and easily saving changes to a file or database. This type of storage device has many advantages to work within genealogical databases and frequently alter the data file, and add, remove, and change information [47].

b. Static Storage: This type of storage device allows the user to save data at a specific point in time and create a non-vulnerable version of the data that may not be easily altered or deleted, as with dynamic storage devices [48].

Table 4. Comparison between Static Logic and Dynamic Logic

Static Logic	Dynamic Logic
Valid logic levels are steady-state operating points [40]	The operation depends on temporary storage of charge in parasitic node capacitances [32]
Outputs are generated in response to input voltage levels after a certain time delay, and it can preserve its output levels as long as there is power [22]	The stored charge does not remain indefinitely, so must be updated or refreshed. This requires establishment of an update or recharge path to the capacitance frequently enough to preserve valid voltage levels [46]
All gate output nodes have a conducting path to V_{DD} or GND, except when input changes are occurring [5]	

Although static CMOS logic is widely used for its high noise margins and relative ease of design, it is limited at running extremely high clock speeds. For applications requiring the faster circuit speeds, dynamic CMOS logic has numerous advantages over static CMOS including not only higher speeds but also significantly reduced surface area. The advantages do not come without a cost however. Due to the nature of dynamic CMOS logic, undesired effects can occur within the circuit unless extra effort is put into the engineering design. Table 4 shows a simple comparison between static logic and dynamic logic gate.

4. Available Digital Storages

a) Dynamic Memory Cards: Memory cards are not just used for digital cameras. These storage devices may be used in PDAs containing genealogical databases, digital images, e-mail archives, and other information. Music devices such as I-Pods and MP3 players containing memory card storage may be used as digital recorders genealogically to record oral histories and interview ancestors. Cellular phones or Smart phones devices may also contain many internet features, and will increasingly allow for storage, online viewer capabilities, and storage for computer programs. This type of memory is not susceptible to magnetic deterioration, but may be damaged through digital malfunction. Memory cards are not a good choice for a permanent type of storage, but could be used as a temporary transfer of information.

b) Static Optical Disks: CDs, DVDs, DVD-Rs, DVD+Rs, CD+Rs, and Blueray optical disks are often useful for storage devices. Most of the usages of optical disks are to store data such as photographs, movies, and non-changing data. Optical disks are most frequently used for distribution of databases, or product creation and distribution. Optical disks can be used as a permanent or semi-permanent storage solution. As with most digital storage, optical disks may be corrupted in a variety of ways. First, if information was incorrectly written to the disk, the entire disk may become unreadable. Second, oxidation may create data damage. Digital data is highly volatile and with a minor flaw, all data may become unreadable and unrecoverable.

c) Dynamic Flash Memory: Flash memory is a consumer form of memory that is often used in the workplace. Flash memory is a non-volatile form of memory that allows the user to write/read without changing the integrity of the memory. While this type of storage has a high rate of usability, flash memory devices are easily damaged and often non-recoverable. This should not be used as a permanent form of storage, rather a temporary storage transfer device.

d) Dynamic Hard Drives: Hard drive memory are used in computers, servers, and external hard drives. Hard drives also make up an important part of a data disaster recovery system. Hard drives consist of several dual side platters, with read/write arms that are all attached and move together across the platters at the same time. Platters are made of light aluminum alloy and coated with magnetizable material like ferrite compound applied in liquid form and spun across the plate evenly or electroplated onto the platters like chrome. Newer technology uses glass/ceramic platters because they are thinner, and more efficient at resisting heat. Disk spacers hold the platters apart.

e) Unlike their early predecessors from the 1860s, hard drive disks spin at around 5400-7200 RPMs. Hard drive storage is based on magnetic particle placement, and is therefore susceptible to magnetic surge damage. Also, because the space between the heads and the platters is so small, a small fleck of dust could prevent the disk from spinning and they must be contained in a clean environment. Hard drives are also susceptible to power surges, and breaking parts. Often hard drive information is recoverable if data is lost. Despite the failure factors of hard drive storage, this continues to be a reliable form of digital storage. Hard drives in server arrays may be configured to work together to provide immediate recovery for a failed drive or server. These configurations allow a consumer-transparent recovery, and immediately compensate for device failure. In these configurations, no data is lost and a replacement server or drive will not use any down time to load information because the information is spread evenly across several servers or drives [49]. The capability of many hard drives to work as one hard drive compensates for the occasional hard drive failure and makes hard drive storage a superior choice for dynamic storage.

f) Static Tape: Most large companies, repositories, and storage facilities utilize a linear tape device to back up data from a local area network (LAN) or storage area network (SAN). Data from tapes often stored at an off-site location where this information may be accessed in case of a data disaster. Data from tapes is not rapidly restored like RAM memory, however,

because retrieving data from tape is sequential, rather than random. Tapes are a strip of plastic magnetically coated to allow encoding, not unlike music cassettes. The tapes are not as easily damaged as music cassettes due to the archival thickness and size of the tape strips, but these, like hard drives, are susceptible to magnetic damage, and are also susceptible to heat damage. The portability and cost of these devices make them a frequently used data recovery option. Tapes are not a suitable option for regular file access, however, and are only used for long-term storage.

5. Conclusion

Shift registers, consist of a series of flip-flops, serve an important role in different applications like delay circuit, memory circuit, serial-parallel interface circuit and many more. This review illustrates the different types of shift registers in CMOS technology highlighting their properties and parameters that are particularly important for digital data storage. Moreover, it presents the concept of dynamic storage and a comparative study among the dynamic and static storage systems. However, this review will provide a better understanding of current digital data storage systems and also it can be a guideline for the researcher for their future development of compact and efficient storage system.

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