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A Low-Voltage High PSRR and High Precision CMOS Bandgap Reference

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Abstract

By adopting the technique of pre-regulator, a high PSRR and low temperature coefficient piecewise-linear bandgap reference (BGR) is designed for analog and mixed-signal application in this paper. The piecewise-linear BGR with pre-regulator, which is analyzed and simulated in SMIC 0.18µm CMOS process, has simple circuit architecture. Simulation results show that piecewise-linear BGR with pre-regulator achieves power supply rejection ratio (PSRR) of -102.488dB and -99.73dB, -82.983dB at 10Hz, 100Hz and 1kHz respectively. Piecewise-linear BGR with pre-regulator achieves the temperature coefficient of 2.235 ppm/°C when temperature is in the range from -50°C to 115°C. When power supply voltage V_{DD} changing from 1.2V to 10V, output voltage deviation of piecewise-linear BGR with pre-regulator is only 0.2765mV, but output voltage of piecewise-linear BGR without pre-regulator has a deviation of 38.08mV.

Keywords: *piecewise-linear compensation, pre-regulator, power supply rejection ratio (PSRR), bandgap reference (BGR)*

1. Introduction

Bandgap reference (BGR) is a very important block in most analog and mixed-signal applications, such as digital-to-analog (D/A) and analog-to-digital (A/D) converters [1, 2].The BGR voltage should be independent of fluctuations of power supply voltage and temperature, and also be implemented without modification of fabrication process. In standard CMOS technology, the basic idea of BGR voltage is a weighted summation of the forward-bias emitter-base voltage V_{EB} across parasitic vertical PNP bipolar transistor and the thermal voltage V_t.Traditional BGR inspired by Widlar [3] and Brokaw [4] is first-order temperature compensation. However, temperature coefficient (TC) of first-order temperature compensated references is limited between 10 and 100ppm/ºC over the whole tempearaure range [5], so the first-order temperature compensated BGR cannot meet the requirements of high precision circuits.

To improve temperature perfromance of BGR, many temperaure compensation techniques have been reported [6-9]. These reported BGRs in [7-9] have achieved very good temperature characteristic, but their power supply rejection ratio (PSRR) at 10Hz is less than -80dB. Recently, demands for low-voltage BGR circuits have increased enormously because they are widely used in portable electronic applications. Unfortunately, power supply noise becomes one of the bottlenecks under low power supply voltage, and the power supply noise injected to the output of the BGR circuit is sometimes the most significant noise. So, for mixed-signal and analog integrated circuits under low power supply voltage, in order to reject the power supply noise coupled from the high-speed digital circuit on the chip, it is necessary to choose a BGR structure to achieve high PSRR performance over a broad frequency range. Fortunately, many techniques have been reported to improve PSRR of BGR, such as supply independent current source technique [10], pre-regulator technique [11-14], subtractor technique [15], pseudo floating voltage source technique [16], cascade technique [17], self-cascode current mirror technique [18], low dropout regulator technique [19], and voltage follower technique with PMOS as input transistor [20]. These reported BGR with enhancement PSRR

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technique have achieved some improvement PSRR performance, but they generally have a relatively high temperature coefficient. Therefore, BGR architecture with low temperature coefficient and high PSRR performance must still be analyzed and discussed under low power supply voltage.

A high PSRR and low temperature coefficent CMOS BGR with less than 1V output voltage is designed by adopting piecewise-linear temperature compensation and pre-regulator technique in this paper. Employing a piecewise-linear temperature compensation technique, the designed BGR circuit achieves very good temperature characteristic over a wide temperature range. And, the pre-regulator architecture is used to improve PSRR of BGR over a broad frequecny range.

This paper is organized as follows. In section 2, analysis of piecewise-linear BGR without pre-regulator will be discussed. Section 3 will discuss the improved piecewise-linear BGR with pre-regulator. Simulation results will be shown in Section 4. Finally, conclusions will be given in Section 5.

2. Analysis of Piecewise-linear BGR without Pre-regulator

Figure 1 shows piecewise-linear BGR without pre-regulator, which consists of MOS transistors M_1~M_{11}, bipolar transistors Q_1~Q_2, resistors R_1~R_4 and amplifiers A_1~A_2. In this paper, all MOS transistors adopt the long channel component so that the channel-length modulation effect is negligibly small. For convenience analysis, it is assumed that I_j is the drain current of transistor M_j, here j=1, 2…, 11.

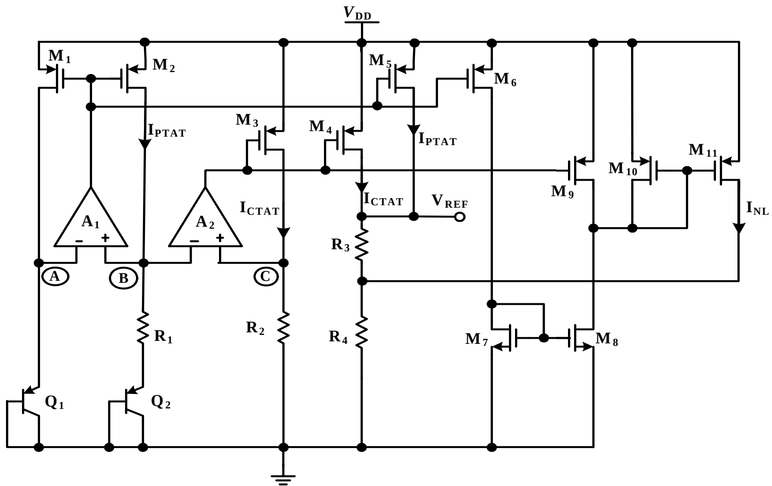

Figure 1. Piecewise-linear BGR without Pre-regulator

As shown in Figure 1, bipolar transistor Q_2 has an emitter area that is m times that of Q_1. Amplifiers A_1 and A_2 are entirely the same, and their dc gain A_d has that A_d>>1. Amplifier A_1 forces voltage V_A of node A and voltage V_B of node B be equal, and amplifier A_2 forces voltage V_B of node B and voltage V_C of node C be equal, i.e. V_A=V_B=V_C=V_{EB1}. Here, V_{EB1} is the emitter–base voltage of bipolar transistor Q_1. Transistors M_1 and M_2 are entirely the same, so the drain current I_{PTAT} of M_2 can be obtained as:

$$I_{PTAT} = \frac{kT}{q}\frac{1}{R_1}\ln m \quad (1)$$

Where, k is Boltzmann’s constant, q is electronic charge, and T is absolute temperature. Equation (1) shows that I_{PTAT} is proportional to absolute temperature T. Similarly, the drain current I_{CTAT} of M_3 can also be obtained as:

$$I_{CTAT} = \frac{V_{EB1}}{R_2} \tag{2}$$

In Equation (2), V_{EB1} has a negative temperature coefficient, so I_{CTAT} is a current with negative temperature coefficient. M_3 and M_9 are entirely the same, so drain current I_9 of M_9 is equal to drain current I_3 of M_3, i.e. $I_9=I_3=I_{CTAT}$. M_2 and M_6 are also entirely the same, and it is concluded that $I_6=I_2=I_{PTAT}$. M_7 and M_8 form current mirror pair, and the channel width-length ratio of M_8 is α times that of M_7. For the drain current I_8 of M_8, it is concluded that $I_8=\alpha\times I_{PTAT}$. By optimizing the parameter α, it is concluded that $I_8=\alpha\times I_{PTAT}=I_9=I_{CTAT}$ under the room temperature T_r. Therefore, the following expression can be obtained as:

$$\begin{cases} I_8 = \frac{\alpha}{R_1}\frac{kT}{q}\ln m < I_9 = \frac{V_{EB1}}{R_2}, & when \quad T < T_r \\ I_8 = \frac{\alpha}{R_1}\frac{kT}{q}\ln m = I_9 = \frac{V_{EB1}}{R_2}, & when \quad T = T_r \\ I_8 = \frac{\alpha}{R_1}\frac{kT}{q}\ln m > I_9 = \frac{V_{EB1}}{R_2}, & when \quad T > T_r \end{cases} \tag{3}$$

According to the circuit shown in Figure 1, drain currents of M_8, M_9 and M_{10} have that $I_{10}=I_8-I_9$. M_{10} and M_{11} are entirely the same, so the drain current I_{NL} of M_{11} can be obtained as:

$$\begin{cases} I_{NL} = 0, & when \quad T \le T_r \\ I_{NL} = \alpha\frac{kT}{q}\frac{1}{R_1}\ln m - \frac{V_{EB1}}{R_3}, & when \quad T > T_r \end{cases} \tag{4}$$

M_3 and M_4, M_5 and M_2 are, respectively, entirely the same, so the output voltage V_{REF} of BGR can be written as:

$$V_{REF} = (R_3 + R_4)(\frac{kT}{q}\frac{1}{R_1}\ln m + \frac{V_{EB1}}{R_2}) + R_4 I_{NL} = V_{PTAT} + V_{CTAT} + V_{NL} \tag{5}$$

Where,

$$V_{PTAT} = (R_3 + R_4)\frac{kT}{q}\frac{1}{R_1}\ln m \tag{6}$$

$$V_{CTAT} = (R_3 + R_4)\frac{V_{EB1}}{R_2} \tag{7}$$

$$V_{NL} = R_4 I_{NL} \tag{8}$$

According to the above analysis, V_{PTAT} and V_{CTAT} are a voltage with positive- and negative- temperature coefficient respectively, and V_{NL} is a voltage with piecewise temperature characteristic. So, by choosing appropriate values of R_1~R_4 and m, the temperature coefficient of bandgap voltage V_{REF} will become negligibly small in theory. Figure 2 shows the relation of V_{REF}, V_{PTAT}, V_{CTAT} and V_{NL}. However, the operation supply voltage of piecewise-linear BGR without pre-regulator is power supply voltage V_{DD}, which cannot achieve high PSRR over a broad frequency range. To improve PSRR of the BGR shown in Figure 1, an improved piecewise-linear BGR is analyzed and designed by adopting a pre-regulator in the next section.

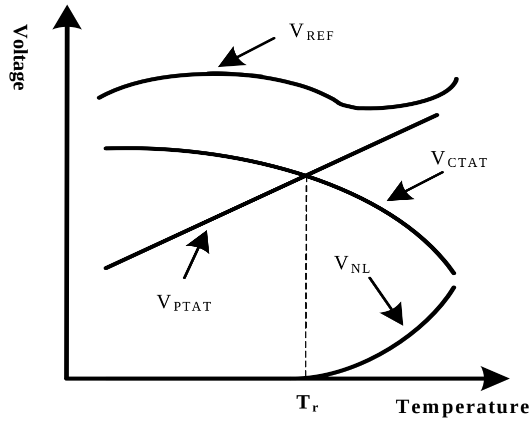

Figure 2. Relation of V_{PTAT}, V_{CTAT} and V_{NL}

3. Analysis and Design of Improved Piecewise-linear BGR with Pre-regulator

To improve the PSRR performance of BGR shown in Figure 1, a high PSRR piecewise-linear BGR is designed by adopting pre-regulator technique, as shown in Figure 3. The improved BGR with pre-regulator consists of a start-up circuit, pre-regulator and BGR core circuit. The BGR core circuit is similar as that reported in Section 2, but the operating supply voltage of BGR core circuit is the output voltage V_{REG} of pre-regulator instead of power supply voltage V_{DD}. There are two possible equilibrium points in the BGR core circuit, so a start-up circuit is necessary. M_{s1}~M_{s6} form the start-up circuit, as shown in Figure 3(c).

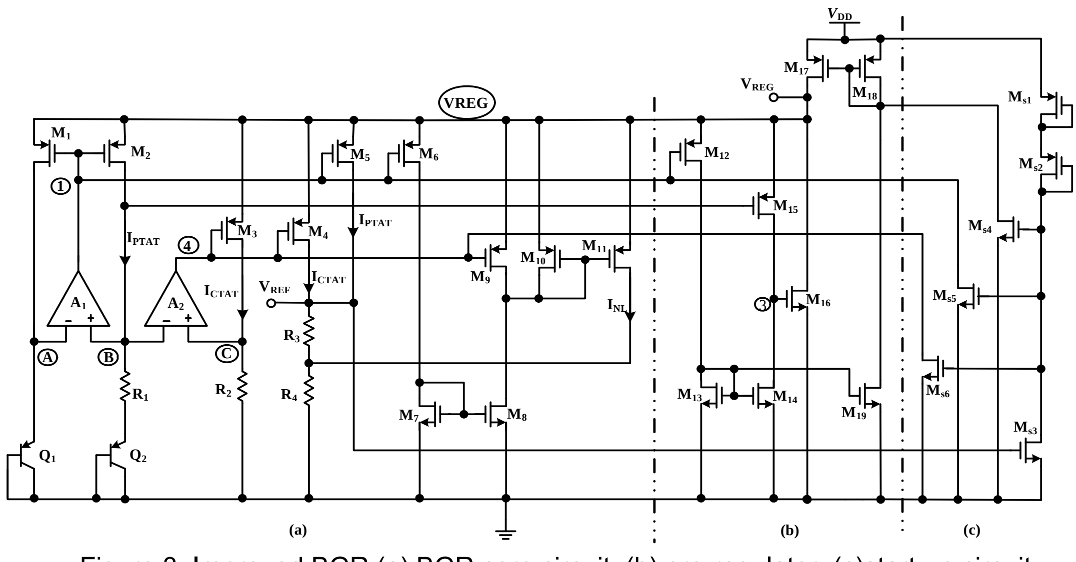

Figure 3. Improved BGR (a) BGR core circuit; (b) pre-regulator; (c)start-up circuit

As shown in Figure 3(b), pre-regulator is made up of transistors M_{12}~$M_{19,}$ and whose function will provide a regulated supply voltage V_{REG} which is the operation supply voltage of BGR core circuit. V_{REG} is adjusted by a negative feedback loop so that the variation of power supply voltage V_{DD} is rejected at node VREG. Assumed an incremental voltage variation v_{reg} at node VREG, node 1 and node B will achieve incremental voltage variation v_1 and v_b respectively. And, node 3 achieves an amplified incremental voltage variation v_3, which feeds a current into the output of pre-regulator and forces the voltage at node VREG to the right voltage. So, the PSRR of piecewise-linear BGR with pre-regulator will be improved and be quantitatively analyzed as follows.

For convenience, it is assumed that g_{mj} and i_j are, respectively, the transconductance and small-signal drain current of M_j, here j=1, 2, 3…, 19. Assumed that there is an incremental voltage variation v_{reg} at node VREG, there are incremental voltage variation v_a and v_b at node A and node B respectively.Then, v_a and v_b can be obtained as:

$$v_a = g_{m1}(v_{reg} - v_1)r_a \tag{9}$$

$$v_b = g_{m2}(v_{reg} - v_1)r_b \tag{10}$$

Where, r_a and r_b are the resistance seen from node A and node B to ground respectively. MOS transistors M_1, M_2, M_5, M_6 and M_{12} are entirely the same, so it is concluded that $g_{m1}=g_{m2}=g_{m5}=g_{m6}=g_{m12}$. Amplifier A_1 and A_2 are entirely the same, and their dc gain A_d has that $A_d>>1$. According to the circuit shown in Figure 3, the voltage variation v_1 at node 1 has that $v_1=A_d\times(v_b-v_a)$. So, v_1 can be written as:

$$v_1 = \frac{A_d g_{m1}\beta v_{\mathrm{reg}}}{1+A_d g_{m1}\beta} \tag{11}$$

Where,

$$\beta = r_b - r_a \tag{12}$$

So, the following expression can be obtained as:

$$\begin{cases} i_{mj} = g_{mj}(v_{reg} - v_1) = g_{mj}\dfrac{1}{1+A_d g_{m1}\beta}v_{reg} \\ j = 1 \sim 2, 5 \sim 6, 12 \end{cases} \tag{13}$$

According to Equation (13) and the circuit shown in Figure 3, the drain current variation i_{15} of M_{15} can be obtained as:

$$i_{m15} = g_{m15}\left(1 - \frac{g_{m2}r_b}{1+A_d g_{m1}\beta}\right)v_{reg} \tag{14}$$

M_{13} and M_{14} are entirely the same, so it is concluded that $i_{14}=i_{13}=i_{12}$. So, the drain current variation i_{16} of M_{16} can be obtained as:

$$i_{m16} = g_{m16}r_3 g_{m15}\left(1 - \frac{g_{m2}r_b}{1+A_d g_{m1}\beta}\right)v_{reg} - g_{m16}r_3 g_{m12}\frac{1}{1+A_d g_{m1}\beta}v_{reg} \tag{15}$$

Where, r_3 is the resistance of node 3. v_4 has also that $v_4=A_d\times(v_c-v_b)$, and $v_c=g_{m3}\times(v_{reg}-v_4)$. So, the voltage variation v_4 at node 4 can be obtained as:

$$v_4 = \frac{A_d g_{m4}R_2 v_{reg}}{(1+A_d g_{m4}R_2)} - \frac{A_d g_{m1}r_b}{(1+A_d g_{m1}\beta)(1+A_d g_{m4}R_2)}v_{\mathrm{reg}} \tag{16}$$

M_3, M_4 and M_9 are entirely the same, so it is concluded that $g_{m3}=g_{m4}=g_{m9}$.Then, the following expression can be obtained as:

$$\begin{cases} i_{mj} = g_{mj}\dfrac{1+A_d g_{m1}\beta + A_d g_{m1}r_b}{(1+A_d g_{m1}\beta)(1+A_d g_{m4}R_2)}v_{\mathrm{reg}} \\ j = 3, 4, 9 \end{cases} \tag{17}$$

Transistors M_{10} and M_{11} are entirely the same, and the aspect ratio of M_8 is α times that of M_7. So, it is concluded that $i_{10}=i_{11}=i_8-i_9=\alpha\times i_6-i_9$. Transistors M_{13} and M_{19} are entirely the same, and it is concluded that $g_{m19}=g_{m13}$.

According to the Kirchhoff current law (KCL) at node VREG, the following equation can be obtained as:

$$\frac{v_{dd}-v_{reg}}{r_{o17}}+i_{12}\frac{g_{m19}}{g_{m13}}\frac{g_{m17}}{g_{m18}}=i_1+i_2+i_5+i_6+i_3+i_4+i_9+i_{10}+i_{11}+i_{12}+i_{15}+i_{16} \tag{18}$$

Where, v_{dd} is the incremental voltage variation of power supply voltage V_{DD}, r_{o17} is the source-drain resistance of M_{17}. It is assumed that $A_d\beta>>r_b$, $A_dg_{m15}\beta>>1$ and $A_dg_{m1}\beta>>1$. According to Equation (9)~Equation (18), the following expression can be obtained as:

$$\frac{v_{reg}}{v_{dd}}\approx\frac{1}{1+(g_{m16}r_3g_{m15}+g_{m15})r_{o17}+\frac{\beta+r_b}{\beta A_dR_2}r_{o17}} \tag{19}$$

In the similar ways, the relation of v_{reg} and output voltage variation v_{ref} of BGR can be written as:

$$\frac{v_{ref}}{v_{\mathrm{reg}}}=R_3\frac{\beta+r_b}{\beta A_dR_2}+\frac{(1+\alpha)R_4+R_3}{A_d\beta} \tag{20}$$

So, PSRR of piecewise-linear BGR with pre-regulator can be expressed as:

$$PSRR_{dB}=20\lg\left|\frac{v_{ref}}{v_{dd}}\right|=20\lg\left|\frac{v_{ref}}{v_{reg}}\right|+20\lg\left|\frac{v_{reg}}{v_{dd}}\right| \tag{21}$$

According to Equation (19)~Equation (21), it is concluded that piecewise-linear BGR with pre-regulator achieves an improved PSRR by adopting pre-regulator.

4. Simulation Results

To verify the architecture of the designed piecewise-linear BGR in this paper, it is designed and simulated by Cadence Spectre tools in SMIC 0.18μm CMOS technology with a 1.35-V power supply voltage.

Figure 4 shows the simulated output voltage V_{REF} of piecewise-linear BGR with- and without- pre-regulator as a function of temperature. Simulation results show that the output voltage temperature coefficient of piecewise-linear BGR without pre-regulator is 3.313 ppm/°C when temperature ranging from -50°C to 115°C. And, the output voltage V_{REF} temperature coefficient of the improved piecewise-linear BGR with pre-regulator is only 2.235 ppm/°C.

Figure 5 gives the PSRR simulation results of piecewise-linear BGR with- and without- pre-regulator. Piecewise-linear BGR without pre-regulator achieves PSRR of -75.354dB, -75.308dB, -72.2dB, -55.181dB, -35.23dB at 10Hz, 100Hz, 1kHz, 10kHz and 100kHz respectively, and piecewise-linear BGR with pre-regulator achieves PSRR of -102.488dB, -99.73dB, -82.983dB, -63.036dB and -42.962dB at 10Hz, 100Hz, 1kHz, 10kHz and 100kHz respectively. Simulation results show that the PSRR is increased by about 36% at 10Hz by adopting the technique of pre-regulator.

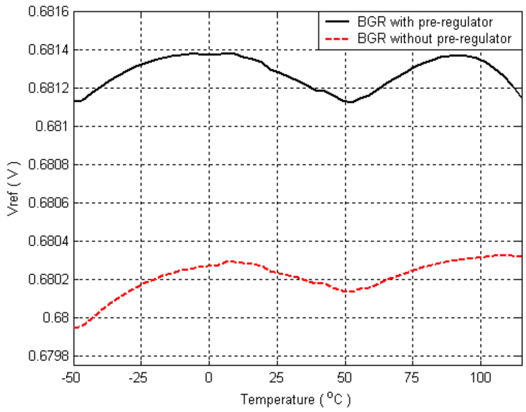

Figure 4. Simulated Output Voltage of Piecewise-linear BGR with- and without- pre-regulator as a Function of Temperature

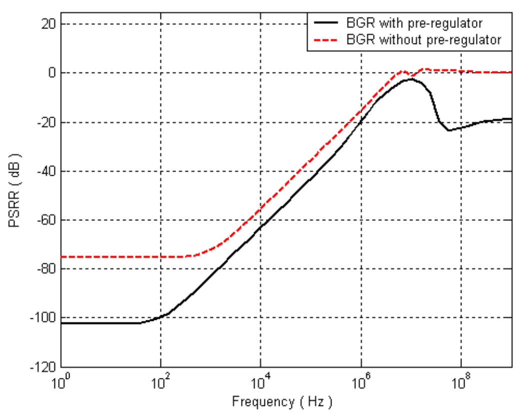

Figure 5. Simulated PSRR of Piecewise-Linear BGR with- and without- pre-regulator

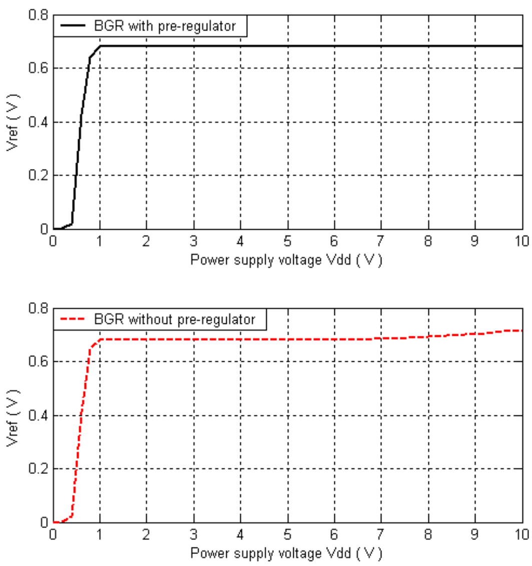

Figure 6. Simulated Line Regulation of Piecewise-linear BGR with- and without- pre-regulator

Simulated line regulations of piecewise-linear BGR with- and without- pre-regulator is shown in Figure 6. When power supply voltage V_{DD} changes from 1.2V to 10V, output voltage variation of piecewise-linear BGR without pre-regulator is 38.08mV, but output voltage variation of piecewise-linear BGR with pre-regulator is only 0.2765mV. Simulation results shows that piecewise-linear BGR with pre-regulator achieves well line regulation performance by adopting the technique of pre-regulator.

Finally, performances of piecewise-linear BGR with- and without- pre-regulator are summarized in Table 1. From this table, comparing with the temperature dependencies of the BGRs, which have been reported in [8] and [20], it can be found that they are in commensurate level. But, by adopting the technique of pre-regulator in this paper, the improved piecewise-linear BGR with pre-regulator achieves better PSRR and line regulation performance than that reported in [8] and [20].

Table 1. Performance Summary of BGR

		Ref. [8]	Ref. [20]	BGR without pre-regulator	BGR with pre-regulator
Process		0.18μm CMOS	0.09μm CMOS	0.18μm CMOS	0.18μm CMOS
Supply voltage (V)		1.8	2.7	1.35	1.35
Output voltage (mV)		646.4	213.982	680.25	681.29
Temperature coefficient (ppm/°C)		1.7	6.071	3.313	2.235
Temperature range (°C)		-40~125	-20~120	-50~115	-50~115
PSRR @25ºC (dB)	10Hz	-75	-82.7	-75.354	-102.488
	100Hz	-	-	-75.308	-99.73
	1kHz	-	-	-72.2	-82.983
	10kHz	-	-	-55.181	-63.036
	100kHz	-	-	-35.23	-42.962

5. Conclusion

A piecewise-linear CMOS BGR with pre-regulator, whose architecture is simple, is designed and analyzed in this paper. By adopting the technique of pre-regulator, piecewise-linear BGR with pre-regulator achieves higher PSRR performance than piecewise-linear BGR without pre-regulator. Simulation results show that piecewise-linear BGR with pre-regulator achieves an output voltage with excellent stability, a low-temperature coefficient, and high PSRR performance. It is well suited for high precision circuits.

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