Indonesian Journal of Electrical Engineering and Computer Science
Vol. 33, No. 3, March 2024, pp. 1397~1404
ISSN: 2502-4752, DOI: 10.11591/ijeecs.v33.i3.pp1397-1404

Design a self-controlled high-performance evaluation of content addressable memories using 45 nm technology

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Article Info

Article history:

Received Aug 18, 2023
Revised Dec 6, 2023
Accepted Dec 26, 2023

Keywords:

Content addressable memory
Low power
Matchline
Self-controlled logic
Tanner tools 45-nm technology

ABSTRACT

A special type of random access memory (RAM) array called as content addressable memory (CAM), in which stored data is compared with the search data which can be returning the address. In the applications of high-speed searching, the CAMs are used. NOR type matchline CAMs are helpful for applications requiring faster search speeds. Because the NOR type match line (ML) CAM consumes a lot of power, therefore many published designs have attempted to reduce power consumption. The design self-controlled high-performance content addressable memories (SC-CAM) using 45-nm technology is presented in this paper. The 6T 4×4 CAM arrays in this paper uses SC logic and Tanner tools 45-nm technology. When compared to the conventional CAM, described SC-CAM architecture reduces the number of voltages sources. Described 6T 4×4 SC-CAM design needs less number of MOSFETs than existed 8T 4×4 CAM array and thus reduces the area with high speed.

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1. INTRODUCTION

The current rapid improvement of electronic circuit technology has resulted in aggressive scaling of devices and connectivity dimensions. Performance and security issues are the two main factors that determine whether current and future internet usage will persist. Data is stored in memory components at various memory locations. If a memory component provides the data right immediately, it is said to be efficient. The input and output of traditional memory are address and data, respectively. In this case, the user must know the content which has been stored in the address location [1]. Due to availability of large amounts of data, determining address location is difficult operation. Software-based search techniques are utilized for this reason; however, the process takes longer. Content-addressable memories (CAMs) are the best options for cloud computing applications because of their high-speed comparing capabilities [2]. Applications like data compression, network security, pattern recognition, and address lookup in internet routers all commonly make use of CAM. Due to their frequent parallel comparison and lookup, match-lines (MLs) had become as CAM's biggest power consumers [3].

CAM has memory unit and comparison unit and search data is considered with stored data. The user can find out where the data is stored with the aid of CAM. Compared to software-based search algorithms, content addressable memory was quicker in searching [4]. There are many different applications at which high speed of operation is required. Applications of this nature can employ CAMs. However, the primary use

of CAM is packet classification and sending high-speed network routers. As CAM applications grow, the demand for huge CAM sizes increases, which makes the power issues worse. Therefore, lowering power consumption in large capacity CAMs without compromising speed is the main challenge [5].

Ternary CAM (TCAM) and binary CAM (BiCAM) are two groups of CAM cells [6]. In this case, the TCAM uses all 0s, 1s, and x [don't care set], while the BiCAM uses both 0 s and 1 s [7]. Moreover, sparse clustering networks have been used to develop a small number of associated memories. Decreasing the power usage in CAMs with large capacity is the key challenge. Since CAM power consumption is inversely correlated with CAM memory capacity, the power consumption of CAM must improve spontaneously when a few applications request a bigger size of CAM memory [8]. Through bitline drivers, the data is stored in its internal memory CAM. The search operation is carried out by CAM after receiving the search content from input data driver. If search data is similar to stored content, it generates match address. Every search is followed by precharge phase, which limits faster search frequency. The match data (hit/miss) is accessed using a sense amplifier. Designing a high-speed CAM that can handle increasing word lengths is challenging. This analysis describes self-controlled CAM (SC-CAM) that reduces CAM cell dependence and increases operation frequency [9].

CAM is of memory which will control by content alternatively by address. To control the specific entry, to find matches, the search data word is parallelly compared with words that have previously been saved. Every stored word has connected tag which is utilized in comparison procedure. As soon as search data word was implemented for input of CAMs, match data word is obtained within one clock cycle [10]. This superior capability makes CAM ideal for applications requiring frequent and fast lookup functions like database accelerators, translation lookaside buffers (TLBs), parametric curve extractions, image processing, hough transforms, huffman coding/decoding, and imagery. Dynamic complementary metal-oxide-semiconductor (CMOS) circuit methods provide low-power and cost-effective CAM, but structure will suffers from reduced charge sharing, noise margins, and different issues that reduce power efficiency during scaling [11].

CAM is utilized in different applications and it requires very short times. It is ideal for a variety of operations like ethernet address lookup, data compression, packet-based security for high-performance data switches, and encrypted information [12]. First, CAM is extension of random-access memory (RAM), so to understand CAM you need to know what RAM does. There are typically two read and write operations in RAM. Three capabilities are available to CAM: read, write, and compare. Data kept in RAM can be read or written. CAM comparison function can be used for various purposes such as network routers. Network routers refer to their routing tables to forward incoming packets from sender port to correct destination port. Fundamentally, CAM is utilized to structure network routers for high-speed transmission or sending packets [13].

Packet classification and forwarding are two most frequently used search-intensive CAM tasks in internet routers. Examining protocol header fields, such as incoming and outgoing ports, source and destination addresses, internet protocol (IP) routing is carried out. Once more, save the data in routing tables. The package was forwarded toward port(s) specified in table if a match is registered [14]. This task must be completed quickly and in a massive parallel fashion networks are extremely high speeds and volumes of traffic. The management of high speeds and sizable lookup tables, however, necessitates silicon area and power usage.

The write and search stages of a CAM data operation can be separated. The write operation in CAM, which is comparable to semiconductor memory, is distinct from the search operation. The total cascade of CAM cells considerably slows down the search process. Short circuit current as well as charge sharing difficulties with conventional NAND and NOR type CAM, a novel self-controlled match line approach is presented. Therefore, the overall performance parameter was enhanced by the self-controlled circuit's ability to decrease voltage swing on mismatched matchline [15]. This summary's remaining content is arranged as follows: section 2 explains on the literature review, section 3 represents the described 45 nm SC-CAM model, simulation results is represented in section 4 and the conclusion of the paper is represented in section 5.

2. LITERATURE SURVEY

A novel CAM architecture with a pre-charge controller is presented which is simple and very effective [16]. When unique words are stored in a CAM every search cycle necessarily requires the release of all MLs predicts one matches the search word. Mismatched MLs will always dissipate the charge during the evaluation stage, here to prevent these lines from fully precharged, such MLs are expected earlier in the precharge stage. This promises a CAM with lower power usage and faster searches times. A CAM matrix configuration using BiCAM is described in [17]. Other names for CAM include associative memory,

associative storage, and associative array. Parallel comparisons are filtered out of searches using the design method. The described design operates more quickly and with less electricity than the conventional design.

A novel method for producing high-performance CAMs is explained that consumes less power and has a faster response time than similar traditional architectures [18]. The first approach is pipeline search operation by fragmenting a similar matching action for different search registers. Speed has significantly increased to the simultaneous comparison of four search-line registers. The following components can also be turned off to reduce power usage. To achieve even greater performance, the second method employs a multi-bank involves evaluating register structure. According to the testing results, up to 37.32% power will be preserved and 90.79% of time will be saved as compared to a standard NOR-type CAM architecture.

A novel, effective, and modular approach for fabricating static random-access memory (SRAM)-based BiCAMs on field programmable gate arrays (FPGAs) to attain huge storage capability hierarchical search is used [19]. Explained approach effectively generates match indication for each unique address by keeping indirectly indexes for addressing match indicators. Due to the repeatability of the offered method, exponential growth into linear is alleviated. Our method has increased storage effectiveness and can create BCAMs that are up to 9 times wider than those created by conventional techniques. Open-source library is being provided by an entirely parameterized verilog implementation. The library has received extensive testing using altera's model sim and quartus.

A brand-new and effective method for building thin and thick BCAMs in FPGA utilizing regular SRAM blocks [20]. Due to the fact that pattern width and BRAM (block RAM) usage are inversely correlated, this method performs well for both deep and thin CAMs. Conventional techniques only produce a third of the Fmax and 43 times more adaptive logic modules (ALMs) for the 64K-entry test-case. There is a verilog implementation that is fully customizable. Utilizing altera's capabilities, this solution has undergone extensive testing. Outlined a method for lowering the material memory is a bit energy usage in systems that use dataflow distributed processing [21]. The described way involves breaking memory word into multiple shorts chunks and starts search in every successive segments only if match is already available. The findings of the computer modeling show that this method can minimize bits in search function by 77%.

A differentially ML sensing amplifier which is based on the low-power CAM [22]. Once the suitable comparisons are created, the self-disabled sensing system mentioned will choke charged current fed to ML. Unique NAND (NOT AND) CAM cell with both differentiated ML design was introduced in place of the common nor/nand-type CAM cells with single-ended match line, which could also speed up comparisons while reducing power consumption. Additionally, to update the data and ensure its accuracy prior to searching, the 9-T CAM cell offers extensive write, read, and comparison capabilities. There is also a read-out circuit that is deactivated.

For 180 nm CMOS innovation, a comparative study of standard 8T, suggested 8T, and traditional 6T SRAM cells with enhanced stability and static noise margin is completed in [23]. The following is the way this paper is organised: section 2 shows the 6T SRAM cell, which is introduced in area 1. The suggested 8T SRAM cell is shown in area 3. typical 8T SRAM cell in area 4. The simulation and the results that examine the various limits of 6T and 8T SRAM cells are included in Segment 5, along with the conclusions from segment 6.

The integration of hierarchical bank division with xor (HBDX) and bank division with remap table (BDRT) techniques is used in [24] to create efficient multi-ported memory (MPMs). To prevent write conflicts, the BDRT technique is set up using a remap table and a hash write controlling mechanism. The 2W4R uses 64 BRAMs to achieve 16K memory depth at a frequency of 268 MHz, using 2.27% of the available slices. In a comparable manner, the 3W4R utilises 2.28% slices and 96 BRAMs to provide 16K memory depth at a frequency of 250 MHz. The suggested designs on the same FPGA device are compared with the best present designs in terms of chip utilisation (slices), frequency, and BRAMs.

A SRAM cell structure with eight transistors and extremely low leakage is presented in [25]. When compared to other 8T SRAM cells already in use and 6T SRAM, the suggested cell's leakage power in hold mode was greatly reduced. Compared to 6T SRAM, the proposed SRAM achieves a slightly lower read margin but a greater write margin. In hold mode, the suggested methodology uses 790 PW of power, which is incredibly low when compared to other methods currently in use.

For the 9T schmitt trigger-based SRAM cell (9T-ST), a reconfigurable negative bit line collapsed supply (RNBLCS) write driver circuit is shown in [26], greatly enhancing write performance for real-time memory applications. Write-ability of SRAM cells is greatly reduced by increasing device parameter deviations in deep sub-micron technology. With respect to transient-negative bit line (Tran-NBL), capacitive charge sharing (CCS), and conventional write circuits, the proposed RNBLCS write-assist driver for 9T-ST SRAM cell has optimised write access delays of 0.84, 0.48, and 0.27; improvements in write static noise margin (WSNM) of 1.05, 1.08, and 1.19; improvements in write margin (WM) of 1.05, 1.13, and 1.39; and minimum write trip-point (WTP) of 0.96, 0.89, and 0.72.

3. CAM ARCHITECTURE

This paper describes the development of self-controlled high-performance evaluation of CAMs in 45-nm technology (SC-CAM). There are two varieties of content accessible memory. This group includes memory that can be addressed with both binary and ternary content. BiCAM cells can only store 1 and 0, however TCAM cells will store 1 and 0 and won't care (X). ML architectures of the NOR and NAND types are used in CAMs. In contrast to NOR (NOT OR) type ML, which has high speed at the price of high energy dissipation, NAND kind ML has low-power consumption but low speed. Therefore, NOR type MLs are typically chosen over NAND type MLs. The self-control operation avoids depending on the previous ML value by using the charge stored at each connection node to regulate the ML transistors. The 6T CAM cell's node value generates the output and manages the evaluation mechanism. A high value is sent to ML if the search content matches the prestored data; otherwise, a low value is passed. Therefore, time required for described SC-CAM is minimized.

In this paper, NOR type TCAM and BiCAM cells are designed. Figure 1 displays a BiCAM cell of the NOR type. Only one SRAM cell is needed for a BiCAM cell. Setting I=0 stores a logic "0," while setting I=1 stores a logic "1." In a cell BiCAM, a search for a "0" logic occurs when search line (SL)=1 and SL=0, while a search for a logic "1" occurs when SL=1 and SL=0. M1 will be ON, M2 will be OFF, M3 will be OFF, and M4 will be ON if SL=0 and I=0 (search bit and stored bit are the same). ML not being linked to the ground ensures that ML is kept at a high value. SL=0 and I=1 (search bit and the stored bit are different) result in M1 being OFF, M2 being ON, M3 being ON, and M4 being OFF. ML linked to ground, which causes ML to discharge.

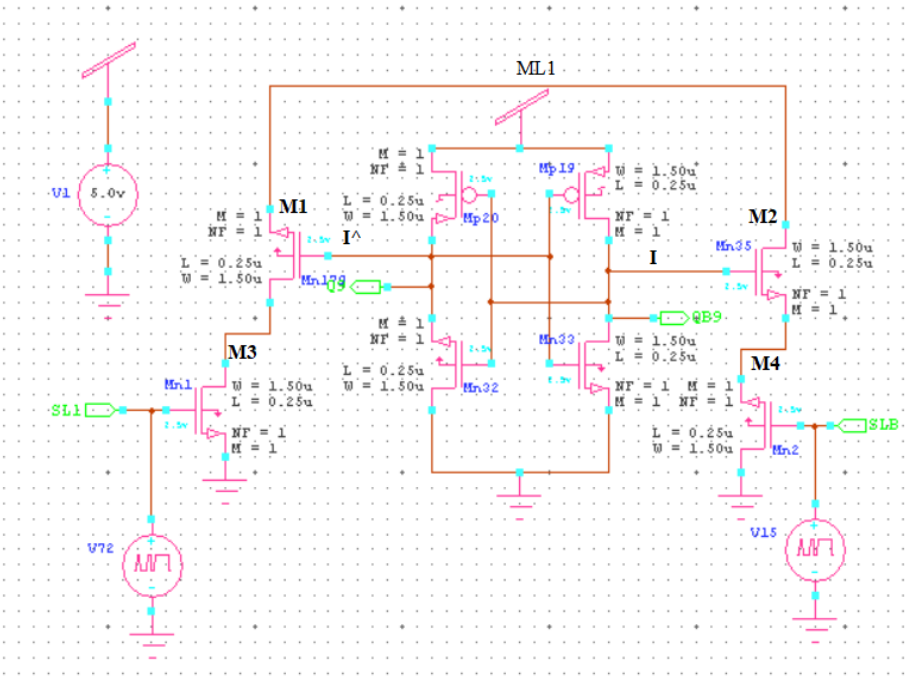

Figure 1. NOR type Bi-CAM cell

Compared to BiCAM, TCAM is the CAM that is utilized widely. In Figure 2, the TCAM cell and its encoding are displayed. The TCAM cell can store the two bits required to define three states with the aid of two SRAM cells. Setting B=1 and A=0 stores a "0" logic, setting B=0and A=1 stores a "1" logic, and setting B=1 and A=1stores a "don't care" logic (X). Here, the states of A and B are both empty. In the TCAM cell, the search for a logic "0" occurs when SL=0 and SL=1, the search for a logic "1" occurs when SL=1 and SL=0, and the search for a logic "don't care" (X) occurs when SL=1 and SL=1.

Figure 3 depicts the structure of the NOR type BiCAM matchline. In this case, the supply voltage voltage drain drain (VDD) is coupled to the BiCAM cell through a positive-metal oxide semiconductor (PMOS) transistor. Writing data through the CAM is the initial step. Then, ML must be recharged to a high voltage level prior to searching. When "pre" value is assigned low, the matchline is originally charged to a high voltage.

If A=0, B=1, and SL=0, SL=1, then M1 is ON, M2 is OFF, M3 is OFF, and M4 is ON (stored data and search data are same). ML maintains a high value since it is not attached to the earth. If A=0, B=1, SL=1, and SL=0, M1 is ON, M2 is OFF, M3 is ON, and M4 is OFF (stored data and search data are different).

Due of ML's direct connection to ground, ML discharges as a result. If A=1 and B=1, M1 and M2 are in the OFF state. So, ML is always high, regardless of the search data. TCAM cells utilize more power than BiCAM due to their additional state. Figure 4 depicts the NOR type TCAM matchline structure. It operation is similar to the BiCAM matchline structure.

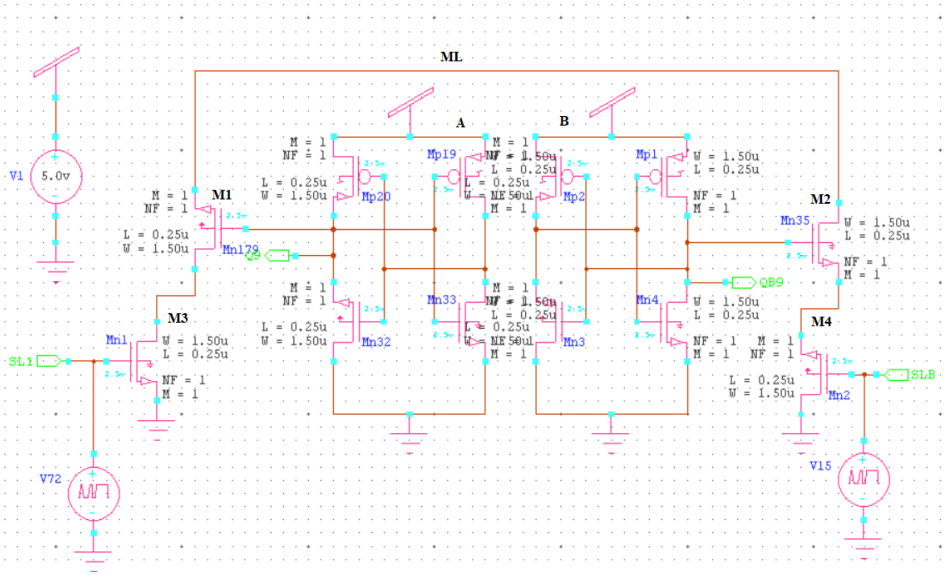

Figure 2. Nor type T-CAM cell

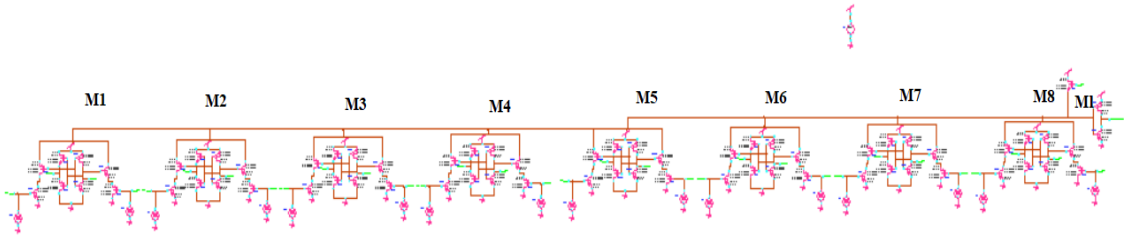

Figure 3. NOR type matchline BICAM

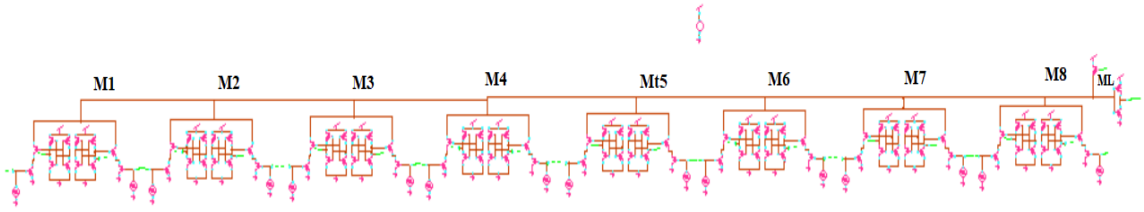

Figure 4. NOR type matchline TCAM

4. RESULTS ANALYSIS

The Tanner tool 45 nm technologies were used to develop the BiCAM and ternary CAM cells. The schematic design of 6T 4×4 CAM consists of 4 rows and 4 columns each consists of one 6T-CAM cell. BL (bit line) are used as input to write the data into the memory cells and Q are used as output port to read the data from the memory. Here WL (word line) and is used to select the each row of memory array to read the data in that row. This presented design needs less number of transistors than existed 8T 4×4 CAM array.

4.1. Comparative performance

The comparative performance analysis of 8T 4×4 CAM and 6T 4×4 CAM is represented in Table 1. Figure 5 shows the graphical comparative analysis of required number of MOSFETs for 8T 4×4 CAM and 6T 4×4 CAM. Described 6T 4×4 CAM requires less number of MOSFETs compares to 8T 4×4 CAM. Therefore, it is concludes that the performance of 6T 4×4 CAM is improved.

Figure 6 shows the graphical comparative analysis of required number of voltage sources for 8T 4×4 CAM and 6T 4×4 CAM. Described 6T 4×4 CAM requires less number of voltage sources compares to 8T 4×4 CAM. Therefore, it is concludes that the performance of 6T 8×8 CAM is improved.

Table 1. Comparative analysis

Parameters	8T 4×4 CAM	6T 4×4 CAM
MOSFETs	128	96
Voltage sources	41	37
Computed models	2	2
Independent nodes	48	32
Boundary nodes	42	38
Total nodes	90	70

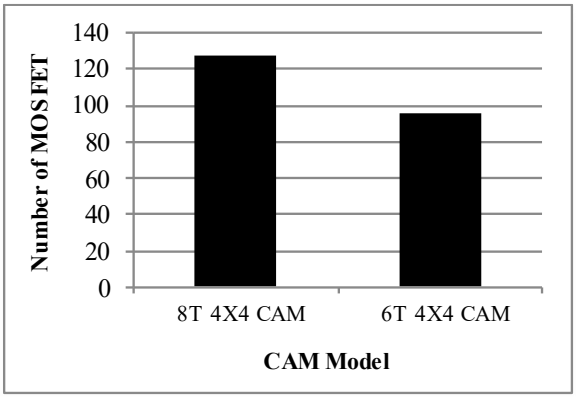

Figure 5. Comparative analysis in terms of mosfet

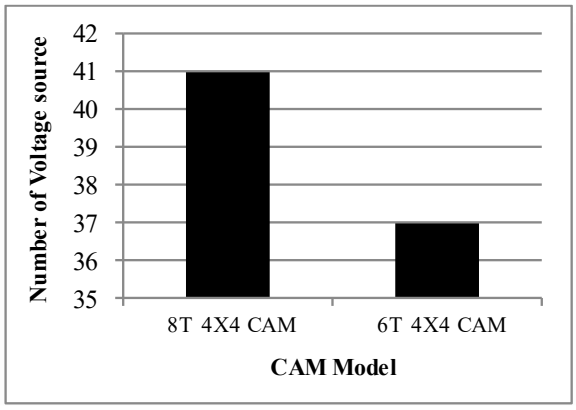

Figure 6. Comparative analysis in terms of voltage sources

Figure 7 shows the comparative analysis 8T 4×4 CAM and 6T 4×4 CAM models in terms of independent nodes. Described 6T 4×4 CAM requires less number of independent nodes compare to 8T 4×4 CAM which is also improves the performance of 6T 4×4 CAM. Figure 8 shows the comparative analysis 8T 4×4 CAM and 6T 4×4 CAM models in terms of boundary nodes. Described 6T 4×4 CAM requires less number of boundary nodes compare to 8T 4×4 CAM which is also improves the performance of 6T 4×4 CAM.

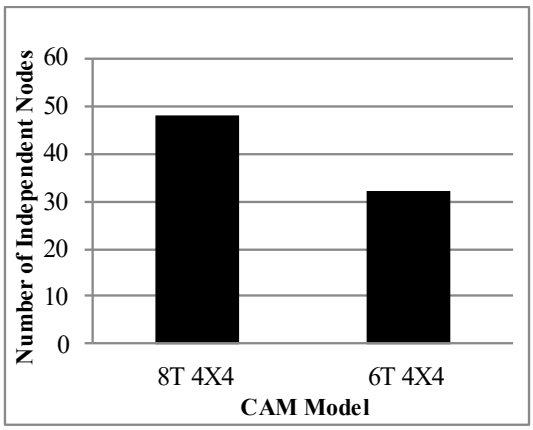

Figure 7. Comparative analysis in terms of independent nodes

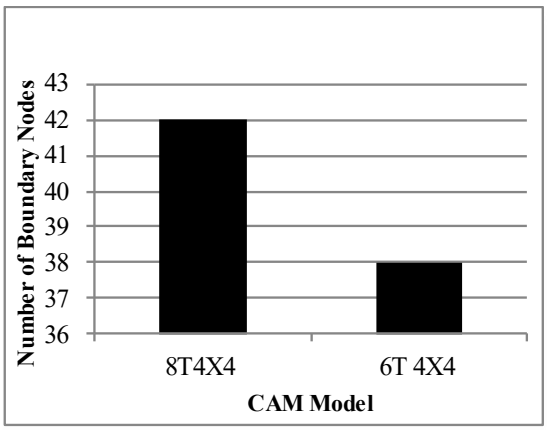

Figure 8. Comparative analysis in terms of boundary nodes

5. CONCLUSION

In this paper, the design of SC-CAM using 45 nm technology is discussed. NOR type TCAM and BiCAM cells are observed and simulated in this study. The Tanner tool 45 nm technology was employed in the development of the BiCAM and ternary CAM cells. Compared to the conventional CAM, described SC-CAM architecture reduces the number of voltages sources. Described 6T 4×4 SC-CAM design needs less number of MOSFETs than existed 8T 4×4 CAM array and thus reduces the area with high speed.

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