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Input-Current and Load Voltage Sharing in Input-Parallel Output-Series Connected Boost Half Bridge DC-DC Converter Using Stable Control Scheme

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Abstract

This paper explores a configuration for boost half bridge DC-DC converters, connected in parallel at the input and series at the output, such that the converters share the input current and load voltage equally. A stable control scheme has been developed to achieve this objective. In order to verify the effectiveness and stability of control scheme, input-parallel output-series (IPOS) connected boost half bridge (BHB) DC-DC Converter has been simulated for the different load conditions such as for fixed load, half load and continuously varying load. The results are found to be satisfactory at each load condition and validate the proposed converter structure.

***Keywords**: boost half bridge (BHB), DC-DC converter, input-parallel output series (IPOS), input current sharing (ICS), output voltage sharing (OVS)*

1. Introduction

Recently, many applications requires high output voltages, the IPOS connection is renowned and is presently used in such applications. With independent output voltage controllers, standard DC-DC converters can achieve equal ICS and OVS [1]. A scheme based on common output voltage loop and individual inner current loops is discussed in [2]. DC-DC converters are commonly used in residential, industrial and aerospace environments. The power supplies have high power density and high reliability due to the advancement in modern scientific technology. Vast research has been made, over last few decades, to develop isolated DC-DC converters which possess the capability of processing the energy effectively [3-8]. For high power density, it is necessary to have high switching frequency. However, increase of the electromagnetic interference and increase of switching losses may be caused by increasing switching frequency. Number of applications are found in literature where low input voltage has to be converted into high output voltage. It is hard to sustain high input current stresses and high output voltage stresses for the single module [9, 10]. A new control strategy has been presented for series-parallel modularDC-DC converters in [11].

An unbalanced output voltage is produced due to the intrinsic variations in the parameters of properly connected identical converters. In addition, this may cause the nonlinear behavior for the circuit variables [12]. The individual converter connected in multi-modular system may suffer from thermal stresses due to the non-uniform distribution of output voltages resulting in the unreliable operation of the system.The architectures with unified approach of voltage distribution control are available in [13, 14]. One common filter has been recommended in [15] for IPOS modular based DC-DC converter with the advantages such as high efficiency, low cost and rapid dynamic response. The full bridge DC-DC converters in IPOS configuration with parameter difference has been analyzed for its performance and the sensitivity of the output voltage error to the maximum parameter variance of circuit components is shown in [16].

This paper proposes the IPOS configuration of BHB DC-DC converters with stable control scheme. The main purpose of the control scheme is to maintain equal ICS and OVS. Therefore, the relationship between ICS and OVS has been developed. In order to verify the control objective, the IPOS configuration of BHB DC-DC converter is simulated on MATLAB

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using simpower tools. Simulation for the converter configuration has been carried out for the different load conditions so that the effectiveness and stability of control scheme can be observed. Equal ICS and OVS are obtained regardless of the different load conditions.

This paper is organized as follows. The IPOS BHB DC-DC converter is shown in section II. The mathematical representation of ICS and OVS is given in Section III. The proposed control strategy is illustrated in Section IV. Simulations and results are presented in Section V. Conclusions are discussed in Section VI.

2. Proposed IPOS BHB DC-DC Converter Configuration

The BHB DC-DC converter in the form of IPOS configuration is represented in Figure 1 as a general block diagram. The proposed configuration with schematic diagram is shown in Figure 2. Identical BHB DC-DC converters are connected in parallel at the input side whereas at the output side these are connected in series. The green blocks shown in Figure 2, as module# 01 and module# 02, consisting of a half bridge together with an inductor and input DC voltage; have been connected at the primary side of high frequency transformer while voltage doubler rectifier is connected at secondary side of high frequency transformer. The turn ratio of high frequency transformer is set to be 1:2 for individual modules. The output voltage will be increased in the proportion as the turn ratios of high frequency transformer are selected. The proposed configuration has been design to operate at various load conditions. Complementary switching signals are given to Q_1, Q_2 of module# 01 and Q_3, $Q_4$of module# 02. The switching signal of individual switches is called duty cycle. Same duty cycle will be achieved in proposed converter configuration due to the identical converters. Moreover, equal ICS and OVS can be achieved inspite of the various load conditions. The configuration of IPOS considered in this paper comprising of only two BHB DC-DC converters but can be extended to any number converters.

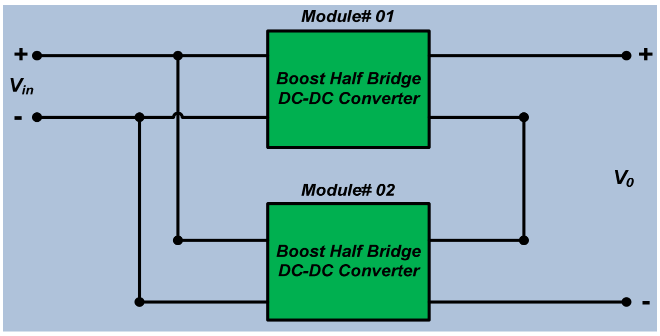

Figure 1. Block Diagram of IPOS

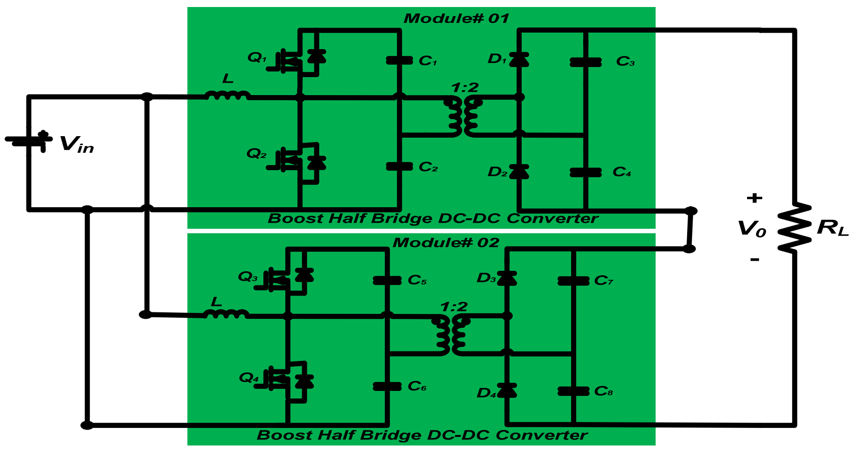

Figure 2. Proposed IPOS BHB DC-DC Configuration

3. Numerical Representation of ICS and OVS

Numerical representation of ICS and OVS can be achieved for IPOS BHB DC-DC converter configuration taking into consideration Figure 1. As the input of the converter configuration is connected in parallel, therefore the voltage across each input of converters must be equal to total input voltage V_{in}. Similarly, the output side of the converter configuration is connected in series, as a result the output current through each converter must be same as the load current i_0. Since the voltage across each converter is represented as V_{in1} and V_{in2} respectively, whereas the current through each converter at the output side is shown as i_{01} and i_{02} respectively. Hence,

$$\begin{bmatrix} V_{in} \\ i_0 \end{bmatrix} = \begin{bmatrix} V_{in_1} \\ i_{01} \end{bmatrix} = \begin{bmatrix} V_{in_2} \\ i_{02} \end{bmatrix} \tag{1}$$

The total input current generated through input voltage is i_{in} which is distributed between the two inputs of the converter modules asi_{in1} and i_{in2} respectively. In the same way, the voltage across the load (V_0) is shared at the output side of each converter as V_{01} and V_{02} respectively. Thus,

$$\begin{bmatrix} i_{in} \\ V_0 \end{bmatrix} = \begin{bmatrix} i_{in1} \\ V_{01} \end{bmatrix} + \begin{bmatrix} i_{in2} \\ V_{02} \end{bmatrix} \tag{2}$$

The equal amount of the current will be shared between the inputs due to the identical converters and hence the output voltage will be shared equally.

$$i_{in1} = i_{in2} \tag{3}$$

$$V_{01} = V_{02} \tag{4}$$

Equation (3) and (4) represents that equal ICS and OVS can be achieved by the proposed IPOS BHB DC-DC converter.

4. Stable Control Scheme

The stable control scheme for achieving equal ICS and OVS for IPOS BHB DC-DC converter configuration is demonstrated in Figure 3. It is obvious from Figure 3 that each converter module has its own controller. With the help of individual controllers each module will detect the input current and the common output voltage. The individual controller consists of dual loop control for each module so as to obtained fast dynamic response and steady state response. The individual controllers are used to generate the duty cycles for the switches of each module with the help of switching frequency. The duty cycle for Q_1 and Q_2 are complementary, in the same way the duty cycles for Q_3 and Q_4 are also complementary. The phenomenon of generating duty cycles for switches Q_1, Q_2, Q_3 and Q_4 is illustrated in Figure 4.

Assuming i_{in1} is greater i_{in2} at any instant, then the error signal of input currents is obtained for module# 01.

$$\Delta i_1 = i_{in1} - i_{in2} \tag{5}$$

Therefore, the reference value of the voltage can be described as:

$$V_{ref_1} = V_{ref} - K\Delta i_1 \tag{6}$$

Similarly, we can get the expression for converter module# 02.

$$\Delta i_2 = i_{in2} - i_{in1} \quad (7)$$

Hence,

$$V_{ref_2} = V_{ref} - K\Delta i_2 \quad (8)$$

It can be concluded with the help of Equation (5) to Equation (8) that:

$$V_{ref_1} < V_{ref_2} \quad (9)$$

As long as the duty cycle is concerned, converter module# 02 will have the larger duty cycle as compared to converter module# 01. It happens due to the fact that the dual loop control operating in the situation where V_{ref1} is less than $V_{ref2}$for BHB DC-DC converters. It shows that i_{in2} is increasing while i_{in1} is decreasing with respect to time. This will continue until both currents are in equilibrium. Hence, equal current sharing at the input is obtained. Once the currents are equal at the input, the voltages at the output will also be equal.

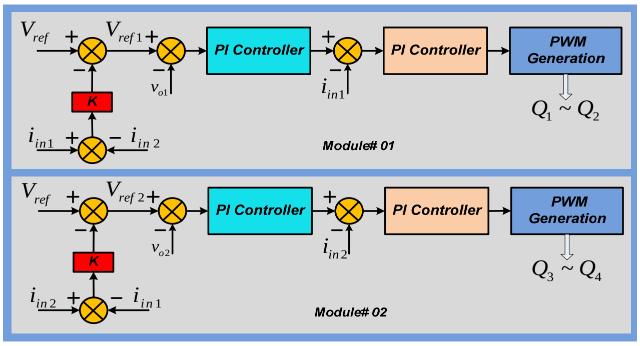

Figure 3. Stable Control Scheme

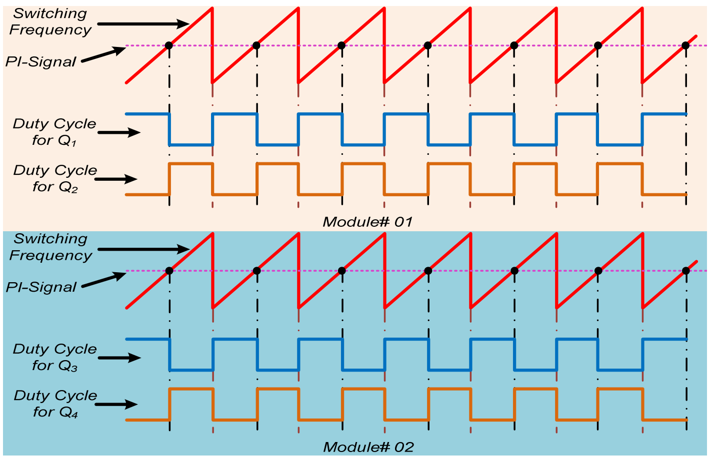

Figure 4. The Phenomenon of Generating Duty Cycles for Switches

5. Simulations and Results

The proposed control scheme, illustrated in Figure 3, together with IPOS BHB DC-DC converter have been simulated using simpower tool of MATLAB. The specifications required to simulate the converter configuration have been shown in Table 1. In order to observe the steady state and dynamic response of the control scheme, the IPOS configuration for BHB DC-DC converter was simulated for different load conditions. Based on load conditions, the simulated results are classified into three different categories which are described as under:

Table 1. Specifications

Parameters	Value	Parameters	Value
V_{in}	50V	V_0	200V
L	200μH	C_3,C_4,C_7 andC_8	8μF
C_1,C_2,C_5 andC_6	10μF	R_{L_full}	50 Ω
f_s	20KHz	R_{L_half}	25 Ω

5.1. At Full Load Condition

The simulation results at full load condition for IPOS BHB DC-DC converter configuration are represented in Figure 5. The simulation result for ICS and OVS are described together with output current sharing and load voltage. It is obvious from Figure 5 that during full load condition ICS is equal to 8A whereas the OVS is equal to 100V. Furthermore, output current is 4A and the load voltage is 200V.The results obtained through simulation at full load condition are demonstrated in Figure 6 by using the block diagram of IPOS BHB DC-DC converter.

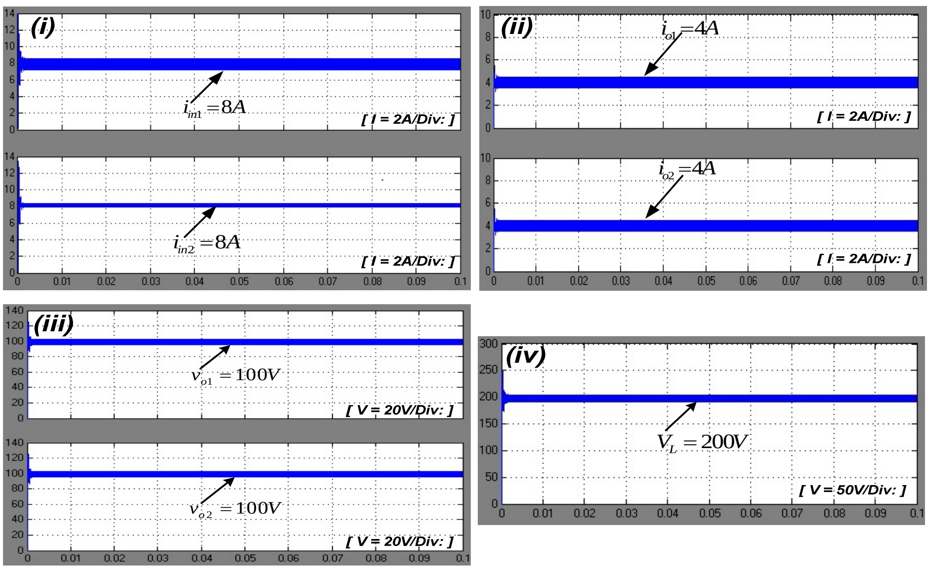

Figure 5. Simulation Results at Full Load Condition: (i) ICS, (ii) Output Current, (ii) OVS, (iv) Load Voltage

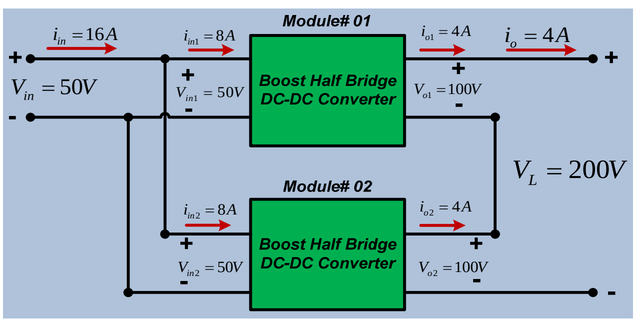

Figure 6. Block Diagram at Full Load Condition

5.2. Full Load to Half Load Condition

The behavior of IPOS BHB DC-DC converter configuration is shown in Figure 7 when the load is changing from full load to half load condition. The load variation and the effect on the ICS and OVS is described in Table 2. Equal ICS and OVS is observed regardless of the load variation. The results acquired by simulation at half load condition are demonstrated in Figure 8.

Table 2

Load Condition	Time Range	Load Value	ICS	OVS
Full Load	0 - 0.05 Sec	50 Ohms	8A	100V
Half Load	0.05 - 0.1 Sec	25 Ohms	16A	100V

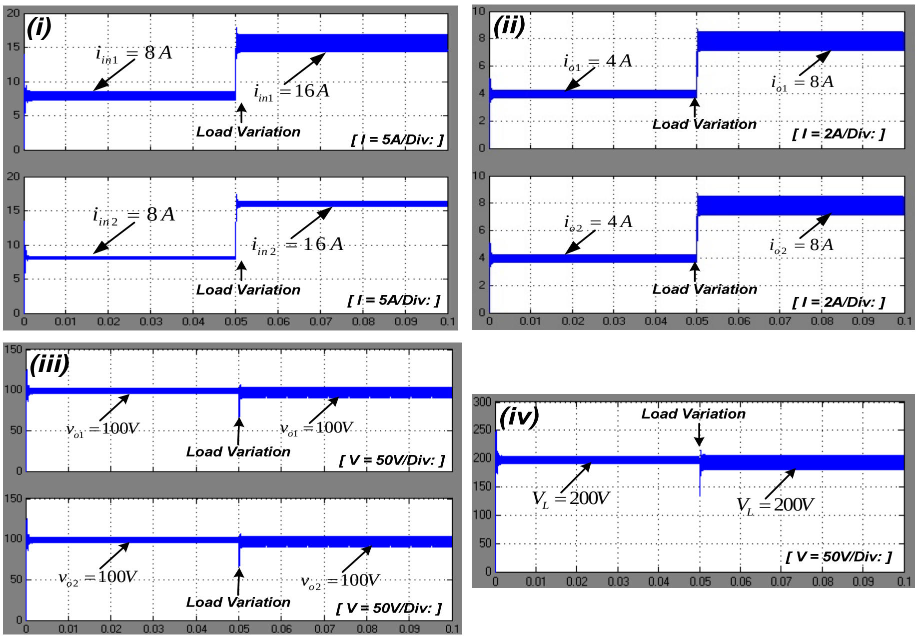

Figure 7. Results for Full Load to Half Load Condition: (i) ICS, (ii) Output Current, (ii) OVS, (iv) Load Voltage

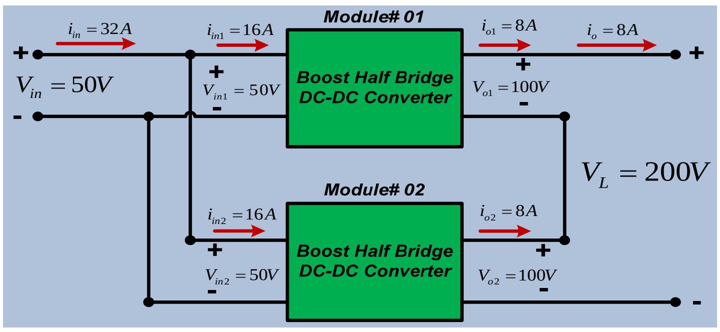

Figure 8. Block Diagram at Half Load Condition

5.3. Half-full-half Load Condition

The results for IPOS BHB DC-DC converter configuration are represented in Figure 9 when the load is repeatedly changing from half load to full load condition. The load variation and the effect on the ICS and OVS is expressed in Table 3. Regardless of the load variation, equal ICS and OVS is observed.

Table 3

Load Condition	Time Range	Load Value	ICS	OVS
Half Load	0 - 0.03 Sec	25 Ohms	16A	100V
Full Load	0.03 - 0.07 Sec	50 Ohms	8A	100V
Half Load	0.07 - 0.1 Sec	25 Ohms	16A	100V

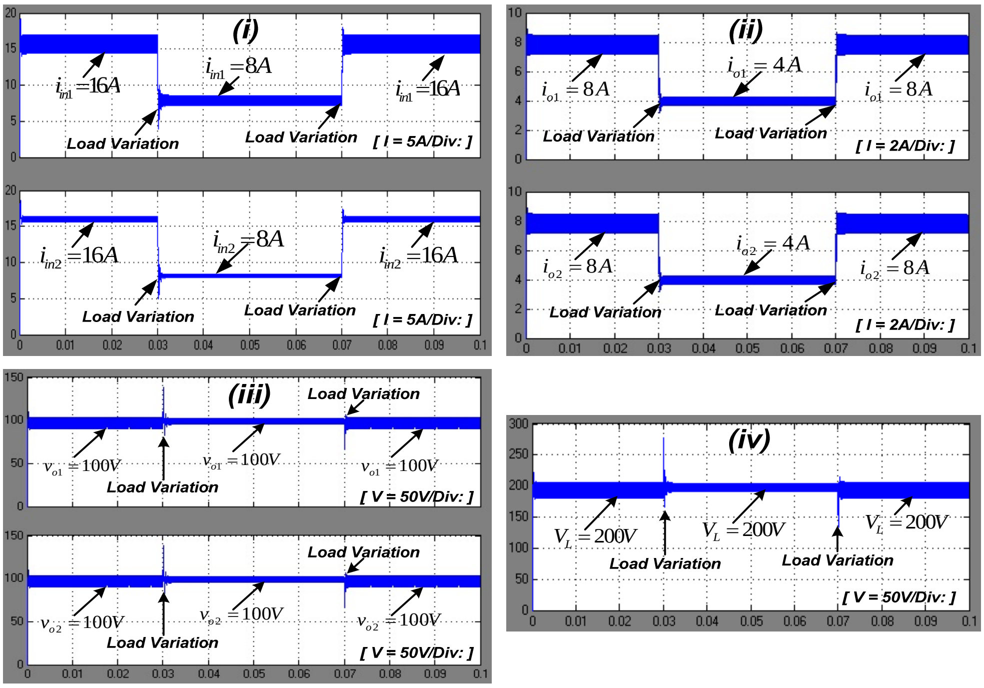

Figure 9. Results for Half-full-half Load Condition: (i) ICS, (ii) Output Current, (ii) OVS, (iv) Load Voltage

6. Conclusion

The configuration proposed in this paper for BHB DC-DC converter is IPOS with the stable control scheme. The prime purpose of stable control scheme is to achieve equal ICS and load voltage sharing under steady state condition. The main objective of the control scheme has been achieved not only for the full load but also for the half load. The response of the converter configuration at different loads has been observed in simulation results. Satisfactory simulation results at different load conditions have been found. Therefore it can be concluded that the IPOS BHB DC-DC converter configuration in conjunction with stable control scheme has good dynamic and steady state response. The two converter modules have been focused in this research work for IPOS configuration but can be extended to any number.

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