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Experimental Verification of Circulating Current Mitigation Scheme in MMC by Using ISE Technique

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Abstract

The circulating currents of a modular multilevel converter (MMC) are ideally assumed to be the sum of an ac component and dc ac component operating with fundamental frequency. However, as ac current flows through the submodule (SM) capacitors, the capacitor voltages fluctuate with time. Consequently, the circulating current is usually distorted and allows multiple frequency components with the peak value of it is increased compared with the theoretical value. The circulating currents will increase power losses and may threaten the safe operation of the switching devices and module capacitors. This article proposes a MMC with a new controller design to mitigate circulating currents for various modulation indexes for wide ranges in load. This new controller is optimized with upper and lower module voltages as an objective function. The optimum values for controller are obtained by using conventional integral square error technique (ISE). The proposed scheme shows its effectiveness by controlling the circulating currents for various loads. It made strategic conclusions on MMC to make the system more robust in operation and less complexity in design and control. The proposed system is verified by 10KVA prototypes MMC and results are explored.

Keywords: *modular multi level converter, circulating current mitigation, application of ISE to MMC*

1. Introduction

Many investigations in the field of modular multi-level inverters are lead to successful operation in high voltage DC (HVDC) systems. In recent times, In the power transmission era, for very long distances HVDC transmission lines based on current source inverters (CSI) and voltage source inverters (VSI) have been offering more economic and cost effective power transmission. But, recently HVDC transmission systems based on VSI have received increasing attention due to many opportunities like to the grid access of weak AC networks, independent control of active and reactive power, supply of passive networks and black start capability, high dynamic performance and small space requirements.

In particular, the novel power converter topology for MMI has been intensively researched and developed, valuated by many features like high modularity, simple scalability, low expense of filters, robust control, simple in design and redundancy. This converter is composed by identical power cells connected in series, each one build up with standard components, enabling the connection to high voltage poles. Although the MMI and derived topologies offer several advantages they also introduce a more complex design of the power circuit and control goals, which have been the main reason for the recent and ongoing research. Furthermore also Medium Voltage Converters are an interesting area for the application of MMCs.

The important features of the modular multilevel converters are as follows:

a. Voltage sharing of the devices will be handled automatically by the topology.
b. The waveform shape will lead to sinusoidal waveform due to which the THD will be reduced and the harmonics as well.
c. The operating voltage can be increased of the converters, instead of connecting the devices in series or in parallel, which makes the system more complex.

As the concept is still in nurturing stage, many researches are going on in suppression of circulating currents. In [1], it proposes a circulating current suppressing controller (CCSC) based on the double line-frequency, negative-sequence rotational frame and are minimized by a pair of proportional integral controllers. A closed-loop method for suppression of the inner

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current in an MMC was proposed [2]. Where as in [3], it develops a general framework for the capacitor voltage balancing of an MMC. In [4], it designs, constructs, and tests a 100-V 5-kVA pulsewidth-modulated STATCOM based on the SDBC, with focus on the operating principle and performance. An improved circulating current control method [5] by applying a digital plug-in repetitive controller is discussed for harmonic elimination of a carrier-phase-shift pulse-width-modulation (CPS-PWM) based modular multilevel converter is discussed. In [6] proposes a control method for circulating currents MMCs under unbalanced voltage conditions. In [7] it proposes a supplementary dc voltage ripple suppressing controller (DCVRSC) to eliminate the second-order harmonic in the dc voltage of the MMC-HVDC system. A modified control architecture for MMC, aiming at suppressing the AC components in the circulating current has proposed in [8]. An additional proportional-resonant control loop is designed to regulate the AC component of the circulating current to zero [9]. Multicarrier level-shifted pulse-width-modulation is applied and the performance of interleaving and non-interleaving the carrier waveforms between the upper and the lower arms is reported [10]. The proportional-resonant (PR) terms for the line current, making it thus possible to introduce explicitly any chosen harmonic component [11]. In [12], it presents a multivariable control approach to realize an optimal current control of the positive, negative and zero phase-sequence converter currents without steady-state error and the compensation of higher harmonics using an extended estimator. A control method of adding the feed-forward current is introduced with strategy of removing the second harmonic current is also described in order to improve the arm currents [13]. One of the proposed solutions includes a main-circuit filter that is tuned to block the second-order harmonic in the circulating current the ac-side current and the higher-order harmonics in the circulating current when such a filter is used [14]. The optimal amplitude and phase of the harmonic current components can be injected in the circulating currents of a MMC to minimize the capacitor voltage fluctuations [15].

This paper is organized in five sections. In section-1, it introduces about the MMC and it will reveals about the necessisty of MMC and problems faced, In section-2, it shall be discussed about the proposed circuit and its operation. In section-3, it shall be discussed about the controller design and it's stability analysis. In section-4, it shall discussed about thesimulation and experimental results. In Section 5, it shall discussed about conclusion with recommendations.

The basic circuit topology is shown in Figure 1. It is a three phase five level MMC having four sub modules in upper limb and four sub modules in lower limb. Each sub module basic circuit is shown in Figure 2. This circuit mainly consist of an inductor having self-inductance L_1 and L_2.Each module consists of main switch S_1 and auxiliary switch S_2 with their anti-parallel diodes D_1 and D_2 respectively. Main switch and auxiliary switch consists of a capacitor connected in parallel as C_{s1}.

It has been considered the five levels MMC for validation. The switching operations are as shown in Table 1. The top four switches in 'R' phase limb is taken as S_1, S_2, S_3, S_4 and the bottom four switches considered as S_5, S_6, S_7, S_8 of a single leg. Whereas the auxiliary switches are in anti-operation of main switches provided with delay, which will be explained in subsequent sections. In the Table 1, it shows the switching states of a MMC. Here, it has been considered '1' indicates the switch is in ON condition and '0' indicates the switch is in off conditions. It mainly consists of one state of 'V/2' output voltage and '16' states of 'V/4' output voltage and '16' states of '0' voltage. In Table 2, It shows the basic operation of a redundancies switch state condition of a one upper limb of Figure 2. In Table 3, it shows the capacitor charging status of a upper limb of a Figure 2.

2. Five Level MMC Operation and Derivation of Circulating Currents

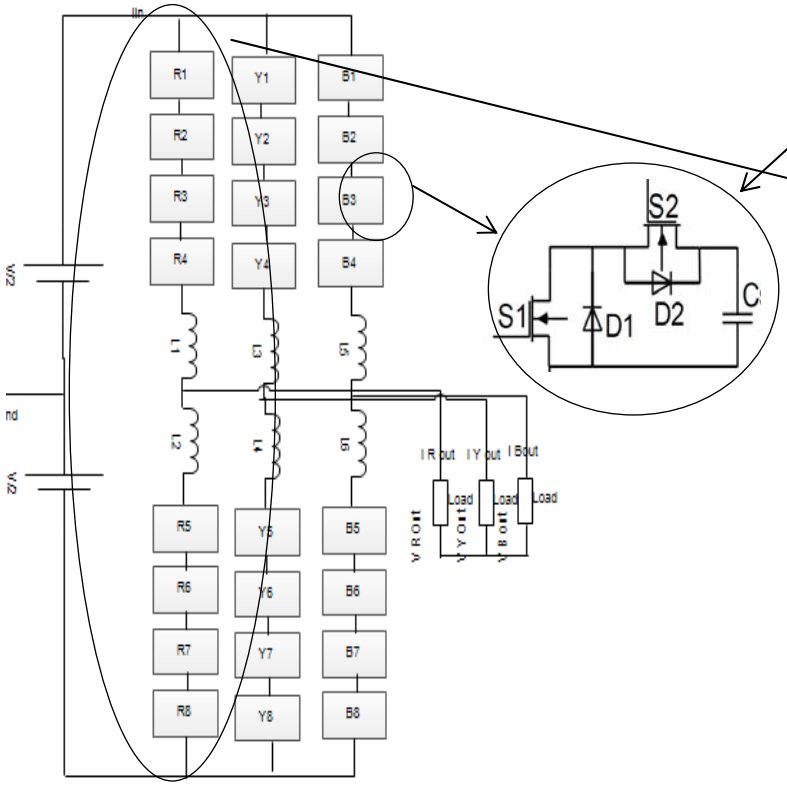

Figure 1. Three Phase Five Level MMC

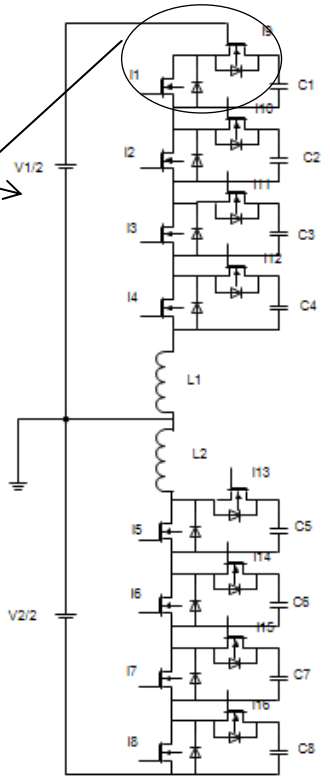

Figure 2. Expanded MMC for a 'R' Phase Limb

Table 1. Basic Switching Operation of a Five Level MMI

State	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	State
$-v/2$	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	$-v/2$
	1	1	1	0	1	0	0	0	0	0	0	1	0	1	1	1	
	1	1	1	0	0	1	0	0	0	0	0	1	1	1	0	1	
	1	1	1	0	0	0	0	1	0	0	0	1	1	1	1	0	
	0	1	1	1	1	0	0	0	1	0	0	0	0	1	1	1	
	0	1	1	1	0	1	0	0	1	0	0	0	1	0	1	1	
	0	1	1	1	0	0	1	0	1	0	0	0	1	1	0	1	
	0	1	1	1	0	0	0	1	1	0	0	0	1	1	1	0	
	1	0	1	1	1	0	0	0	0	1	0	0	0	1	1	1	
	1	0	1	1	0	1	0	0	0	1	0	0	1	0	1	1	
	1	0	1	1	0	0	1	0	0	1	0	0	1	1	0	1	
$v/4$	1	0	1	1	0	0	0	1	0	1	0	0	1	1	1	0	
	1	1	0	1	1	0	0	0	0	0	1	0	0	1	1	1	$-v/4$
	1	1	0	1	0	1	0	0	0	0	1	0	1	0	1	1	
	1	1	0	1	0	0	1	0	0	0	1	0	1	1	0	1	
	1	1	0	1	0	0	0	1	0	0	1	0	1	1	1	0	
	1	1	1	0	1	0	0	0	0	0	0	1	0	1	1	1	
	1	1	1	0	0	1	0	0	0	0	0	1	0	1	1	1	
	1	1	1	0	0	0	1	0	0	0	0	1	1	1	0	1	
	1	1	1	0	0	0	0	1	0	0	0	1	1	1	1	0	
	1	1	0	0	1	1	0	0	1	0	1	0	1	1	0	0	
	1	1	0	0	0	1	1	0	1	0	1	0	0	1	1	0	
	1	1	0	0	0	0	1	1	1	0	1	0	0	0	1	1	
	1	1	0	0	1	0	0	1	1	0	1	0	1	0	0	1	
	1	1	0	0	1	0	1	0	1	0	1	0	1	0	1	0	
0	1	1	0	0	0	1	0	1	1	0	1	0	0	1	0	1	0
	0	1	1	0	1	1	0	0	0	1	0	1	1	1	0	0	
	0	1	1	0	0	1	1	0	0	1	0	1	0	1	1	0	
	0	1	1	0	0	0	1	1	0	1	0	1	0	0	1	1	
	0	1	1	0	1	0	0	1	0	1	0	1	1	0	0	1	

0	0	1	1	1	1	0	0	1	0	0	1	0	1	1	0
0	0	1	1	0	1	1	0	1	0	0	1	0	0	1	1
0	0	1	1	0	0	1	1	1	0	0	1	1	0	0	1
0	0	1	1	1	0	0	1	1	0	0	1	1	0	1	0
0	0	1	1	1	0	1	0	1	0	0	1	0	1	0	1
0	0	1	1	0	1	0	1	0	1	0	1	1	0	1	0
1	0	0	1	1	1	0	0	0	1	0	1	0	1	0	1

Table 2. Basic Switching Operation of a Redundance Switching State in MMI

State	Current	Switching	Capacitor	Capacitor
1010	i_a > 0	S_1 D_2 S_4 D_3	Cs_2 ↑	Cs_4 ↑
1010	i_a < 0	S_2 D_1 S_3 D_4	Cs_4 ↑	Cs_2 ↑
0110	i_a > 0	S_2 D_1 S_4 D_3	Cs_1 ↑	Cs_4 ↑
0110	i_a < 0	S_2 D_1 S_4 D_3	Cs_4 ↑	Cs_1 ↑
0101	i_a > 0	S_2 D_1 S_3 D_4	Cs_1 ↑	Cs_3 ↑
0101	i_a < 0	S_1 D_2 S_4 D_3	Cs_3 ↑	Cs_1 ↑
1001	i_a > 0	S_1 D_2 S_3 D_4	Cs_1 ↑	Cs_3 ↑
1001	i_a < 0	S_2 D_1 S_4 D_3	Cs_3 ↑	Cs_2 ↑

Table 3. Basic Capacitor Switching Operation of a Redundance Switching State in MMI

S_1	S_2	V_{out}	Current	Power	Capacitor
On	Off	0	i_{out} > 0	S_1	Undefined
On	Off	0	i_{out} < 0	D_1	Undefined
Off	On	V_{dc}	i_{out} > 0	D_2	Charge
Off	On	V_{dc}	i_{out} < 0	S_2	Discharge

Due to the un even voltage distribution in the phase legs, circulating current will flow through the system. It also consists of current harmonics which deteriorates the system performance. So, an attempt is made to derive the current harmonics present in circulating currents and its necessary controller to suppress the same. The instantaneous voltage across the capacitor is taken as V_{c1}, V_{c2} ,V_{c3}, V_{c4}…. V_{cN}. It considers the voltage distribution across the capacitors is same.

$$\mathrm{V_{c1}} = \mathrm{V_{c2}} = \mathrm{V_{c3}} = \mathrm{V_{c4}} \ldots . = \mathrm{V_{cN}}. \quad (1)$$

Under any switching condition, the average voltage across the upper arm switches is shown in Equation (2):

$$\frac{\mathrm{V_{C_u}}}{\mathrm{N}} = \frac{\mathrm{V_{Dc}} + \Delta \mathrm{V_{cu}}}{\mathrm{N}} \quad (2)$$

The total capacitor voltage of the capacitor is shown in Equation (3) and deferential capacitor voltage is is shown in Equation (4). The same has been repeated for lower limb and shown in Equation (5), (6) and (7).

$$\mathrm{V_{C_u}} = \mathrm{V_{c1}} + \mathrm{V_{c2}} + \mathrm{V_{c3}} \ldots . \mathrm{V_{cN}}. \quad (3)$$

$$\Delta \mathrm{V_{C_u}} = \Delta \mathrm{V_{c1}} + \Delta \mathrm{V_{c2}} + \Delta \mathrm{V_{c3}} \ldots . \Delta \mathrm{V_{cN}}. \quad (4)$$

$$\frac{\mathrm{V_{C_l}}}{\mathrm{N}} = \frac{\mathrm{V_{Dc}} + \Delta \mathrm{V_{CL}}}{\mathrm{N}} \quad (5)$$

$$\mathrm{V_{CL}} = \mathrm{V_{c(N+1)}} + \mathrm{V_{c(N+2)}} + \ldots . \mathrm{V_{c2N}} \quad (6)$$

$$\Delta V_{CL} = \Delta V_{c(N+1)} + \Delta V_{c(N+2)} + \ldots . \Delta V_{c2N} \quad (7)$$

The circulating currents in the arm inductors consists of both DC and AC components. These AC components are called as the harmonics, since those are rotating with the higher frequencies in the system.

$$i_{cir} = \frac{i_{dc}}{3} + \sum_{n=1}^{\infty}(i_{acn}) \quad (8)$$

$$i_{cir} = \frac{i_{dc}}{3} + i_{ac1} + i_{ac2} + i_{ac3} + \ldots . i_{acn} \quad (9)$$

In order to derive the circulating voltage and circulating current, the output voltage in a single phase out of three phases is:

$$V_a = \frac{V_{dc}.m.\sin(\omega_o t)}{2} \quad (10)$$

$$I_a = I_o.\sin(\omega_o t - \varphi) \quad (11)$$

Where 'm' is the modulation index of a signal.

But, the actual voltage at the output voltage is shown in Equation (12) and (13):

$$V_{acu} = N.\frac{V_{dc}}{2}(1 - m.\sin(\omega_o t))(V_{ac} + \Delta V_{cu}) \quad (12)$$

$$V_{acl} = N.\frac{V_{dc}}{2}(1 + m.\sin(\omega_o t)(V_{ac} + \Delta V_{cl}) \quad (13)$$

Therefore, the total voltage is:

$$V_{ac} = V_{au} + V_{aL} \quad (14)$$

$$= \frac{V_{dc}}{2}(1 - m.\sin(\omega_o t))(\Delta V_{cu} + V_{ac}) + \frac{V_{dc}}{2}(1 + m.\sin(\omega_o t)(V_{ac} + \Delta V_{cl})) \quad (15)$$

$$V_{au} + V_{aL} = V_{dc} + \frac{\Delta V_{cu} + \Delta V_{cl}}{2} + \frac{m.\sin\omega_o t.(\Delta V_{au} - \Delta V_{cl})}{2} \quad (16)$$

To derive the disturbance voltage in the upper and lower cell capacitor of a leg i.e. ΔV_{cv} and ΔV_{CL}.

It considers the voltage across one capacitor module as:

$$V_{c1} = \frac{1}{C_1}\int i_1(t).dt \quad (17)$$

$$V_{cu} = \frac{1}{C_v}\int i_u(t).N_u.dt \quad (18)$$

Here:

$$i_u = \sum_{n=0}^{\infty} i_{un} \quad (19)$$

$$i_L = \sum_{n=0}^{\infty} i_{Ln} \quad (20)$$

$$N_v = \frac{1 - m.\cos\omega t}{2} \quad (21)$$

$$N_L = \frac{1 + m.\cos\omega t}{2} \quad (22)$$

$$V_{cu} = \frac{1}{C_u}\int \sum_{n=0}^{\infty} i_{un}.\frac{1-m.\cos \omega t}{2} \quad (23)$$

$$V_{cL} = \frac{1}{C_L}\int \sum_{n=0}^{\infty} i_{Ln}.\frac{1-m.\cos \omega t}{2} \quad (24)$$

$$C_V = C_1 + C_2 \ldots . C_n \quad (25)$$

$$C_L = C_{n+1} + C_{n+2} \ldots . C_{2n} \quad (26)$$

The current in upper and lower limb is:

$$i_{au} = i_{dc} + i_{a1} + \sum_{n=2}^{\infty} i_{ac}n \quad (27)$$

i_{au} → The current present in the phase 'a' upper arm,i_{dc} →Dc component of the current,i_{ac} → Fundamental component of the current,$i_{ac}.n$ →Harmonic component of the current.

$$i_{aL} = i_{dc} - i_{a1} + \sum_{n=2}^{\infty} i_{ac}.n \quad (28)$$

$$i_{ac} = i_{acm}.\cos(n\omega t + \varphi_n) \quad (29)$$

∴ The total current $i_a = i_{au} + i_{aL}$ (30)

$$i_a = (i_{dc} + i_{a1} + \sum_{n=2}^{\infty} i_{ac}.n) + (i_{dc} - i_{a1} + \sum_{n=2}^{\infty} i_{ac}.n) \quad (31)$$

It conceder's about voltage for 'N' module in terms of capacitance.

$$i_a = I_o.\sin(\omega t - \varphi) \quad (32)$$

it can be written as sum of dc component and ac component as in Equation (33):

$$= (i_{dc} + i_{a1} + \sum_{n=2}^{\infty} i_{ac}.n) + (i_{dc} - i_{a1} + \sum_{n=2}^{\infty} i_{ac}.n) \quad (33)$$

The small change in capacitor voltage in upper and lower limb is shown in Equation (34) and Equation (35):

$$\Delta V_{CU} = \frac{1}{2C}.N.\int (1 - m.\sin(\omega_o t).(\frac{i_a}{2} + \frac{i_{dc}}{3} + \sum_{n=1}^{\infty} i_{acn}).dt \quad (34)$$

$$\Delta V_{CL} = \frac{1}{2C}.N.\int (1 + m.\sin(\omega_o t).(-\frac{i_a}{2} + \frac{i_{dc}}{3} + \sum_{n=1}^{\infty} i_{acn}).dt \quad (35)$$

∴The total phase 'a' voltage is sum of upper and lower voltages.

$$V_a = V_{aU} + V_{aL} \quad (36)$$

$$= V_{dc} + \left(\frac{\Delta V_{CU} + \Delta V_{CL}}{2}\right) + \left(\frac{m\sin(\omega_o t).\Delta V_{CU} - m\sin(\omega_o t).\Delta V_{CL}}{2}\right) \quad (37$$

$$= V_{dc} + \frac{1}{2C}.N.\int (1 - m.\sin(\omega_o t).(\frac{i_{aU}}{2} + \frac{i_{dc}}{3} + \sum_{n=1}^{\infty} i_{acn}).dt + \frac{1}{2C}.N.\int (1 + m.\sin(\omega_o t).(-\frac{i_{aL}}{2} + \frac{i_{dc}}{3} + n=1\infty i_{acn}).dt \quad (38)$$

$$= \frac{m\sin(\omega_o t).\frac{1}{2C}.N.\int (1-m.\sin(\omega_o t).(\frac{i_{aU}}{2}+\frac{i_{dc}}{3}+\sum_{n=1}^{\infty} i_{acn}).dt}{2} - \frac{m\sin(\omega_o t).\frac{1}{2C}.N.\int (1+m.\sin(\omega_o t).(-\frac{i_{aL}}{2}+\frac{i_{dc}}{3}+\sum_{n=1}^{\infty} i_{acn}).dt}{2} \quad (39)$$

From the above Equation (39) it concludes that, the system consists of both dc and ac components. The main important issue is steady state. To maintain it is fundamental and to eliminate the dc and ac components, some controller is required to be added in the system. The

controller should be designed in such a way that, the following Equation (40) and (41) should be satisfied.

$$=> [\int (1 - \mathrm{m}\sin\omega_o t)\frac{i_{dc}}{3} + (1 - \mathrm{m}\sin\omega_o t).\sum_{n=1}^{\infty} i_{acn}] = 0 \quad (40)$$

$$=> \frac{i_{dc}}{3} + \sum_{n=1}^{\infty} i_{acn} = 0 \quad (41)$$

From the Equation (40), it clearly shows the usage of multiple frequency controlled controller. It has been designed and its stability analysis also has been tested successfully in following section.

3. Optimal Controller Used to Compensate the Circulating Currents

By considering the Equation (39), (40) and (41), the controller should design to eliminate the lower order and higher harmonics as well. Even though the higher order harmonics are less in number, as the order of inverter increases it shows its effect on system. In order to eliminate the complete harmonics, here it has been used repetitive controller. Based on Equation (40), a closed loop repetitive controller has been proposed and showed in Figure 3. The circulating current reference is taken as zero and compared with the actual circulating current after passing through the proportional integral controller. All the even and higher order circulating currents are suppressed by employing the inner repetitive controller, which is shown in dotted lines in Figura 3. This inner and outer controllers will ensures the steady state error reach to zero. In this article, it have not shown the transfer function modeling and related analysis but one can easily obtain the transfer function and its analysis by Figure 3 block diagram. Further, it has been tested the stability of proposed controller and it's bandwidth phase and magnitude responses are shown in Figure 4. The optimum values of proportional and integral controller values are obtained by the Integral Square Error Technique (ISE) with Equation (40) as an objective function 'J'.These optimum values is shown in Table 1 for 1% step load and 10% step load.

The frequency characteristic of controller is displayed in Figure 4. Obviously, this controller has a wide range of bandwidth. Outside the region of 200/4000Hz, the gain of it decreases quickly. So, this controller only affects the harmonic currents of i_{cir} around 200/4000Hz. At the frequency of 0.001Hz, the gain of it is much below −100dB, very trivial influence on the dc component in i_{cir}. As the dc component in i_{cir} is responsible for delivering active power from the dc to the ac side, the proposed controller will suitable for wide range of harmonic components. The controller is designed by keeping the stability in view. Controller and it is stability responses as shown in Figure 3 and Figure 5 respectively. It shows the controller will be in stable conditions under any disturbance.

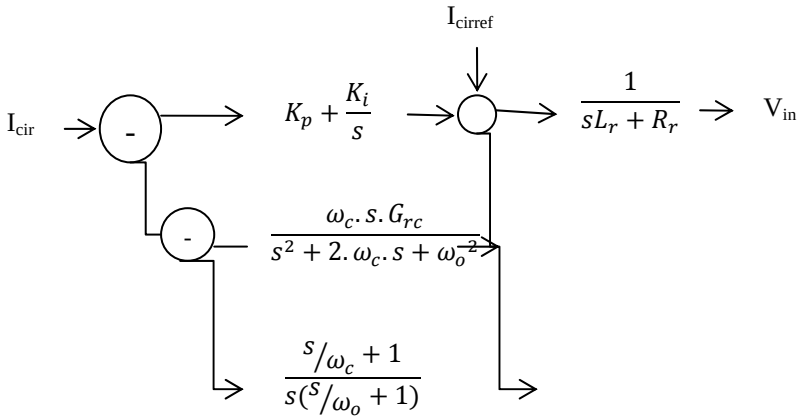

Figure 3. Repetitive Controller used for MMC

In order to make the system fully balanced, one should ensure the net energy transfer would be equal to zero.

$\omega_c \rightarrow Bandwidth\ of\ the\ controller$,
$Grc \rightarrow Gain\ of\ the\ resonant\ controller, \omega_o \rightarrow Resonant\ frequency\ of\ the\ controller$

4. Simulation and Experimental Results

In order to test the proposed method for mitigating the circulating currents of the MMC, computer simulation is carried out first and then verified experimentally as well.

Table 1. Optimum Gain for Proportional and Integral Controller

Five level MMC	Optimum integral controller gain of KI*	Optimum proportional controller gain Kp*
1% Step Load for m=1	1.4	3.6
10% Step Load	2.4	1.8

Table 2. Parameters Used For Five Level MMC Simulation and Experiment

MMC Level	Five
DC Voltage	V_{dc}=200V Dc
Circulating Current reference	I_{cref} = 0
Arm Inductors	L_1=L_2=L=3 mH
Switching frequency	S_f=100 Hz
Capacitor Value	C=16 µF/400V
Bandwidth of the controller	$\omega_c = 2000$
Load Parameters	L_f=10mH/R_f=30Ω
Gain of Resonant controller	Gr_c=1250
Resonant frequency of controller	ω_0=2000

The system has been tested with the parameters listed in Table 1 and Table 2. The experimental setup has been shown in Figure 6.

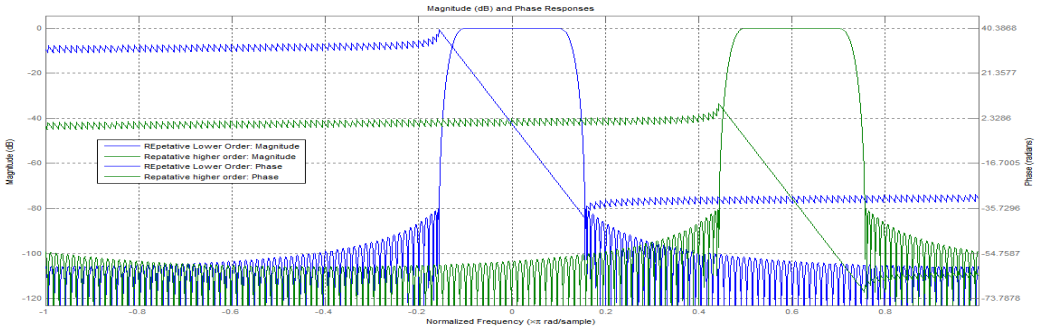

Figure 4. Repetitive Controller Used for MMI Showing Magnitude and Phase Responses

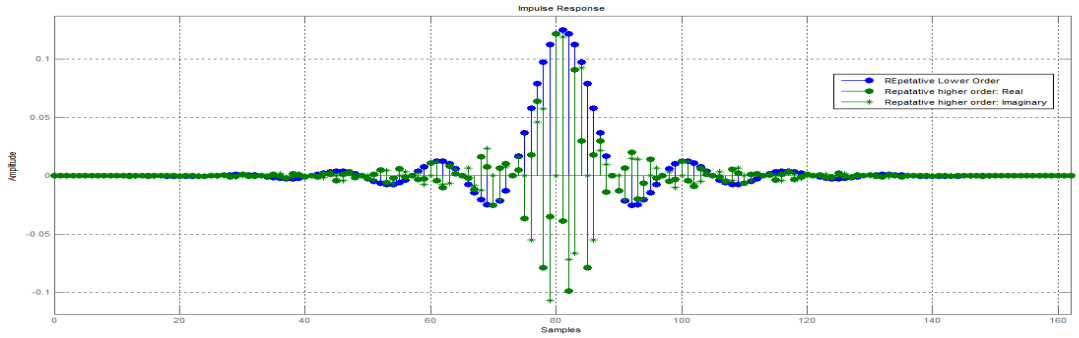

Figure 5. Repetitive Controller Used for MMC Showing Impulse Stability Responses

It has been developed a model, with proposed controller which is suitable for wide range of load with different modulation index.

Firstly, System has been investigated for its output voltage. Since, it is one of the important factor to access the controller performance. System without controller is distorted with its actual values and produce unwanted components called as harmonics in the system. As shown in Figure 7, it is clear that output voltage is distorted without controller. The RMS values of phase to neutral current are 31.4A with controller and 29.2A without controller. From those values it is clear that, output current is also distorted due to circulating currents. Please note that, each division is taken as 5ms.

Form the Figure 8, it is clear that, All harmonics up to 5000Hz are eliminated completely. Due to which, the losses in the system will drastically decreases and efficiency has been increased 14% compared with system without controller.

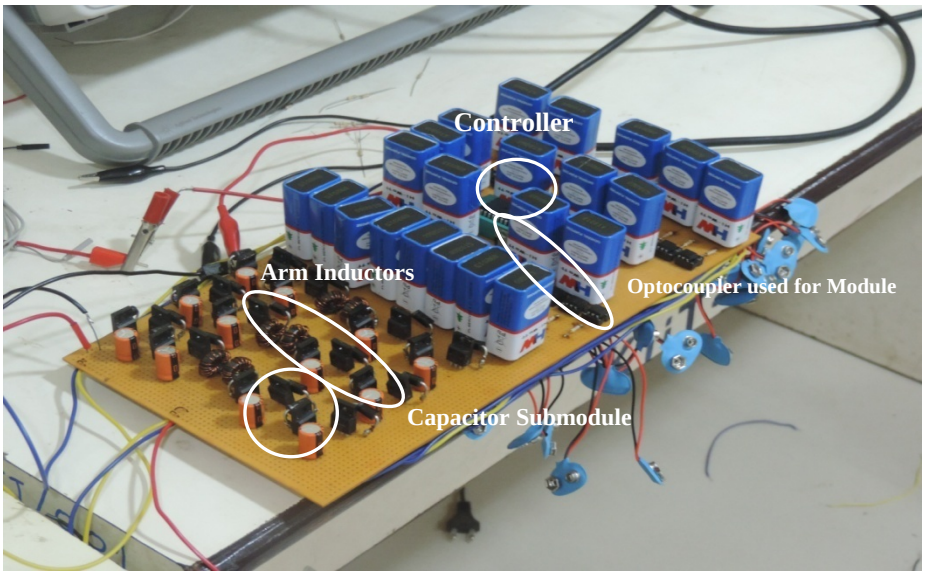

Figure 6. Experimental Setup for Five Level MMC

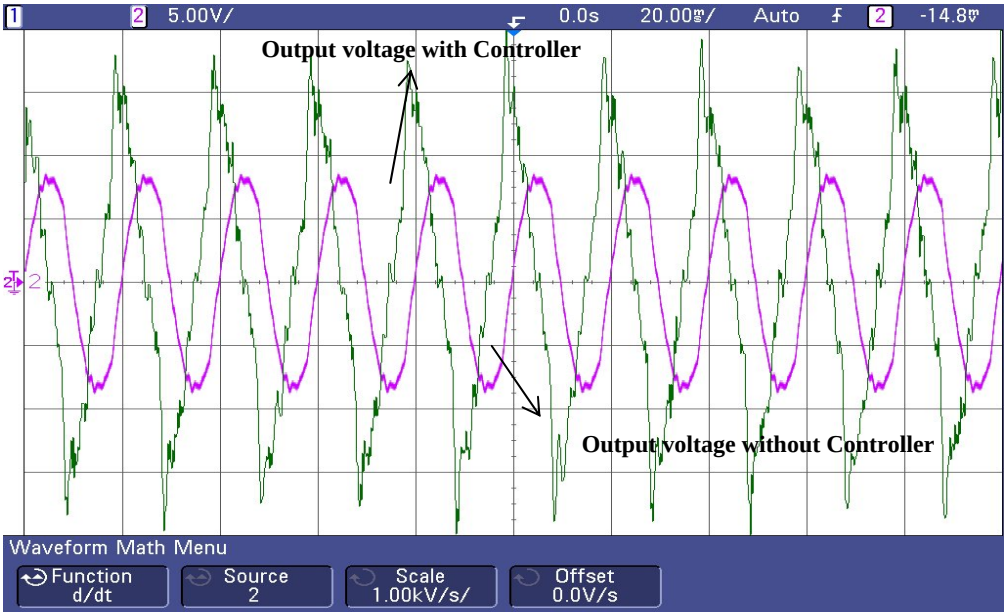

Figure 7. 'R' Phase To Neutral Voltage With and With Out Controller

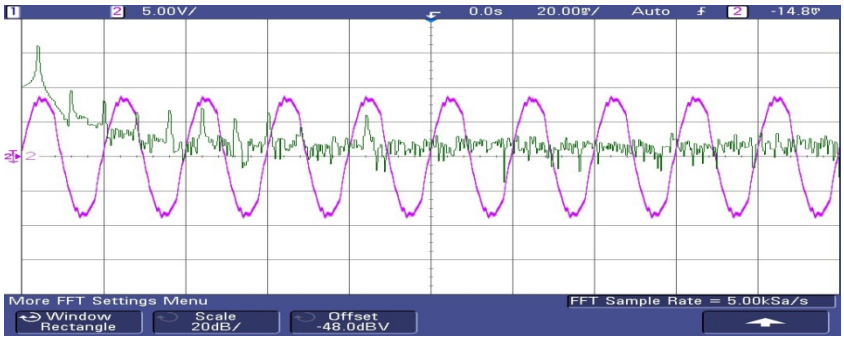

Figure 8. 'R' Phase To Neutral Voltage With it is Frequency Analysis

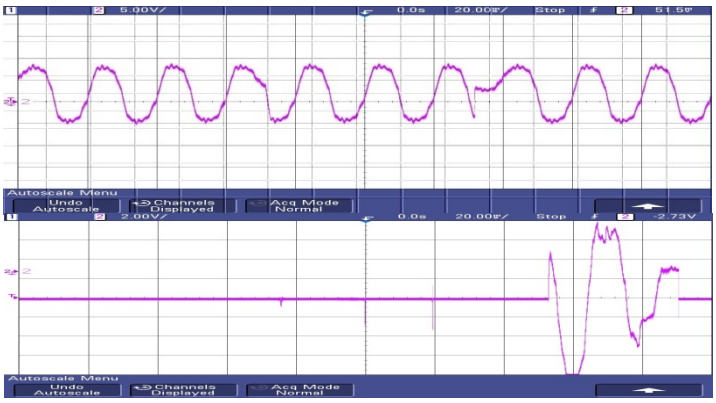

Figure 9. Sub Module Capacitor Voltage for Sudden Change in Load Of 10% and Its Controller Performance

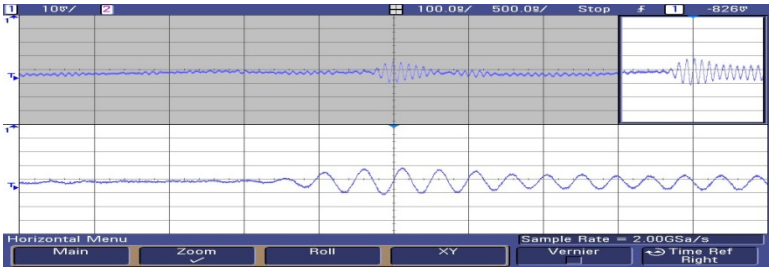

Figure 10. Controller Performance for Various Change in Loads

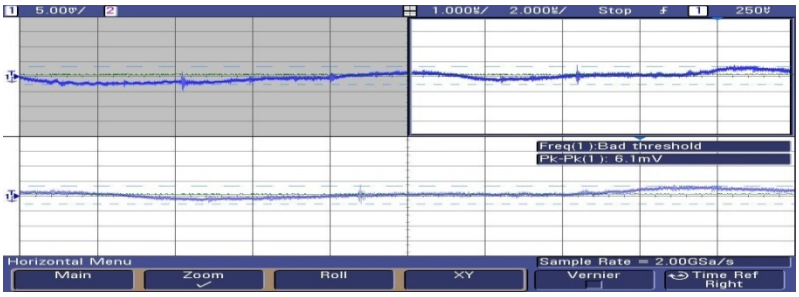

Figure 11. Controller Performance for Various Change in Modulation Indexes

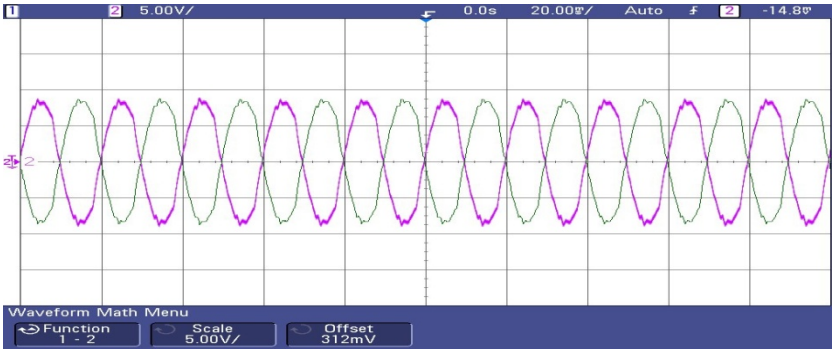

Figure 12. Circulating Currents in Upper and Lower Limb

The system is exposed to sudden change in the load of 10% from its actual value at t=0.032 sec as shown in Figure 9, due to which a sudden dip in the capacitor voltage happens at t=0.033 sec. Suddenly, controller sensed the module voltage and send it's signal to the distorted module and make it's uniform with in 0.02 sec. Then the controller reaches its steady state in 0.007 sec. From Figure 9, it's obvious that, controller is responding quickly for its sudden changes in load and reaches its stability condition as well.

The performance of the controller further investigated for various modulation indexes and various loads as shown in Figure 10 and Figure 11

At time t=20 ns, the load on the system is suddenly increased by 1%, Then controller receives the signal and reciprocates appropriate signal to module, finally settled at t=2ns. Then at time t=60ns, the load on the system is suddenly increased by 10%, Then the controller responded quickly and settled with in time t=10ns. After which, the load on the system is then increased suddenly by 30% and it is settled in t=12ns. From which it is concluded that, as load increases, the controller takes the little time to settle down. All the cases have been shown in Figure 10 and it is zoom is also shown in same. For various modulation indexes the controller response has shown in Figure 11. As modulation index changes, accordingly controller

response has been observed. From the above analysis, it concludes that, controller can be used for various loads and various modulation indexes.

At the outset, the optimimum obtained values by ISE techniques has been implemented and observed the results as shown in Figure 12. From it's clear that upper and lower limb current currents are equal and opposite to each other. The circulating currents are completely eliminated, there by the losses in the system has been decreased drasctillay and efficiency has been increased. The above obtained results are compared with [2], and shown better than those proposed technique.

5. Conclusion

This paper proposed a closed-loop control method for mitigating circulating currents of the MMC. This method is simple in design and can substantially eliminate the RMS value of the circulating current compared with the existing method [2], while the voltages of the sub module capacitors are kept well balanced. This method is very helpful for reducing power losses of the MMC in real HVDC applications. The proposed system can be applied to wide range of loads with various modulation indexes. The steady state analysis and harmonics can substantially reduce by the proposed method. Both simulation and experimental results have shown the validity and effectiveness of the proposed method.

NOMENCLATURE

F	Nominal System Frequency
I	Subscript referred to area i
*	Superscript referred to command value
$\frac{V_{dc}}{2}$	Input DC Voltage
N	Number of sub modules in a half limb
S_i	Main Switch number in a sub module 'N'
Sx_i	Auxiliary Switch number in a limb 'N'
Cx_i	Auxiliary Capacitor number in a limb 'N'
C_i	Main Capacitor number in a limb 'N'
I_{out}	Output current in a phase
I_{tr}	Current in a upper leg of a R phase
I_{br}	Current in a lower leg of a R phase
I_{cir}	Circulating Current in a line
R_{t+} R_b	Total resistance of a limb
L_{t+} L_b	Total inductance of a limb
V_{out}	Output Voltage
ΣV_{ur}	Sum of voltages of a upper limb in R phase
ΣV_{br}	Sum of voltages of a lower limb in R phase
K_i	Integral gain Constant
M	Coefficeint of coupling
K_p	Proportional gain Constant
J	Cost index
T	Sampling time period

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