

Design of matrix, distributive round robin, ping pong and enhanced ping lock arbiter for shared resources systems

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ABSTRACT

Arbiter is one of the main core elements in the network scheduler. The significant goal of this work is to design a high-speed and low execution-time arbiter with lock free and fair arbitration scheme. In this work, four types of arbiters such as matrix arbiter (MA), ping pong arbiter (PPA), distributive round-robin arbiter (DRRA) and enhanced ping lock arbiter (EPLA) are designed and analyzed area, delay, and speed of arbiters. MA is worked in square matrix format and matrix transition is performed for effective routing. The DRRA is designed by using a multiplexer and counter. Hence an, effective scheduling is carried out in DRRA. Binary tree format is used in PPA. The PPA provides low chip size and high speed than existing MA and DRRA. The PPA limits fair arbitration during uniformly distributed active request patterns. To overcome this problem, PPA is improved with some lock systems to create an EPLA. A new ping lock arbiter (PLA) leaf and PLA inter structure is proposed at the gate level to reduce the execution delay, improve the speed and achieve fair arbitration over all other existing arbiters. Resource allocation, execution delay, and speed are analyzed using the Xilinx integrated software environment (ISE) tool.

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1. INTRODUCTION

Currently, a common resource can be accessed by many requestors in several systems. This common resource can be shared memory, specific finite state machines, networking fabric switches, and optimized computational elements. It leads to scaling problems due to integrating many of the integrated circuits into a single core. Arbiter identifies which type of scheduling scheme can be used by requestors to achieve an effective resource allocation policy. A suitable size between the requestors and arbiters must be created by creating an interface between them. The synthesized results will be affected by how the code is written for a specific module. A cyclic scheduling scheme is achieved to avoid repeated routing from the same input channel. The verilog hardware description language (HDL) is used to model these arbiters' designs. Also, logical verification of these arbiters is carried out in Verilog HDL. Once modeling it in Verilog, the Xilinx software calculates the resource utilization, speed, and power utilization.

Problem formulation: initially, the normal bus arbitration scheme is followed in round robin arbiter (RRA). The equal resource allocation scheme is achieved by using a token. Every user has an individual token to make a grant signal at a particular time. One of the users gets grant signals at a specific interval in each clock cycle. An efficient resource utilization scheme will be introduced in recent days. A fast crossbar scheduler

is used for resource allocation policy [1]. In the crossbar switch, multiplexer and de-multiplexer operations are carried out. Initially, the n numbers of the input channel send the request at a time. But only one input channel gets a grant signal first based on the highest priority in the queue. After that, all other input channels are processed cyclically. Also, pipelined implementation is included to improve the speed of a scheduler. But the chip size and power consumption are very high. Previously [2], the programmable priority encoder (PPE) based RRA was used, which requires the highest gate delay. Hence, binary tree structure-based parallel round-robin arbiter (PRRA) is introduced easily and quickly. The die size and power utilization are very high in parallel processing. But the gate delay is low when compared to the crossbar scheduler.

Work contribution: this paper presents a design of four types of RRA, such as MA, distributive distributive round-robin arbiter (DRRA), ping pong arbiter (PPA), and extended ping lock arbiter (PLA) are presented with a fair scheduling policy. A new PLA leaf and PLA inter structure is proposed at the gate level to reduce the execution delay, improve the speed and achieve fair arbitration over all other existing arbiters. Resource allocation, execution delay, and speed are analyzed using the Xilinx ISE tool. Also, these results are compared with all existing other arbiters. The highest priority requestors must be routed first than any other requestor. This paper is structured as follows: in section 2, explains design of matrix, distributive round robin, ping pong and enhanced PLA for shared resources systems. We present the results and discussion in section 3 and conclude this paper in section 4.

In system-on-chip (SoC) implementations, the transaction buses are split by designing a dual RRA [3]. A non-multiplexed rip-transaction bus is constructed using an address bus arbiter and data bus arbiter for SoC implementation. The dual arbiters make certain bounded waiting times for each request. The distributed scheduler-based crossbar switch and proposed distributed arbiter are designed, and the results are analyzed [4]. The fair crossbar switch is designed by using a tiny scheduler and mask circuit. The fair crossbar switch reduces the hardware cost, critical delay, power consumption, and scheduling delay. Also, fairness is predictable. Further, to improve fairness, some other arbiters are introduced nowadays. A programmable priority arbiter is designed using a new bit-level algorithm and parallel prefix adder logic [5]. Hence the delay is reduced and consumes less energy. Also, speed is high in the new programmable priority arbiter. A parallel prefix arbiter with thermo code is designed by using two fixed priority encoders (FPE) and edge detectors (ED) [6]. Four parallel prefix adders are used, such as Brent Kung, Han Carison, Kogge Stone, and Ladner Fischer structures. Carry generation and carry propagation are carried out in three stages to make a carry look-ahead adder (CLA). AND gate operation is used in carry generation. Also, OR gate operation is included in the carry propagation term. The number of stages is reduced in parallel prefix adder. Hence the speed is very high, and the area is low.

A merged arbiter and multiplexer (MARX) structure and sorting-based arbitration algorithm are designed and included in the proposed merge switch allocation and traversal in network operations center (NoC) switches [7]. This switch is used in easy and very difficult arbitration strategies beneath generic structural design. Also, provide efficient area, delay, and energy utilization. An RRA is designed with an index that functions on the index format of key switches [8]. Logarithmic scaling operation is carried out in a number of input ports when compared to all other existing RRA. Hence the index based round robin arbiter (IRRA) IRRA offers high speed, low chip size, and low power consumption. But fairness is limited. Parallel pseudo-RRA is designed to enable multiple requests simultaneously through concurrent operation [9]. So, speed is high, but chip size and power utilization are high. A generic algorithm-based optimization is applied in weighted RRA. An appropriate weight is allocated for every input port [10]. The input channel which has the highest weight is granted first. So, the delay is minimized. But complexity is increased. Clock gating-based RRA is designed to achieve low power and low delay by reducing the switching activity of the clock signal [11]. The clock signal will be generated when the enable and clock are high. So, the number of clock cycles is reduced; hence power is low. The pipelined structure of radix-2, 4, and 8-based multipath delay commutator fast Fourier transform (FFT) is introduced to improve the throughput and speed [12]. A Kalman filter is used with a Madgwick's filter together to suit the fading issues. It involves a priori evaluation of autoregressive parameters [13]. A programmable logic controller provides the accuracy and validity of this model [14]. Median-based, root mean square-based, and P84-based procedures were implemented and investigated in a full comparison between them to find their advantage and disadvantage and the suitability of each method for a specific application [15]. Fusion of computed tomography lung image and positron emission tomography lung image using their structural similarity [16]. The two levels of the energy storage system are used as the battery at the source side and the transformer at the load side [17]. A complete review of the ongoing advances of finite impulse response (FIR) filter plan procedures in multicarrier modulation based correspondence frameworks. Initially, the essential issues are tried, considering the presentation of available data signal applicants and the FIR filter design concept [18]. A single pole double throw discrete switch design is introduced using switchable substrate integrated waveguide resonators. It is designed for the millimeter to wave multiple input multiple output transceivers [19]. It uses a multi-layered array of cells known as a

superstrate multi-layer metasurface. It is identified in front of a patch of microstrip antenna to absorb surface waves and prevent them from passing during the insulating material that minimizes the permeability of the insulator. Therefore, it enhances the antenna properties [20]. Hybrid time-power splitting relaying approach in a full-duplex decode-and-forward battery-energized relaying network [21].

The matrix arbiter (MA) resource utilization is less compared to RRA [22]. RRA, MA, and index-based round robin (IRR) arbiter is explained in [23]. Low-latency communication improves inter processing elements communication by utilizing a circuit switching method with negligible adaptive routing and a fair path resolution method to enhance bandwidth utilization [24]. The improved PPA is optimized to provide lesser delay [25]. The pipelined architecture of multi path delay commutator fast fourier transform is applied for dissimilar length system by investing the data stream of N_s at the input. It improving speed and throughput [26]. The espressif systems 8,266 node micro-controller unit is selected because it may be used as a sensor node and has the arbiter-physical unclonable function. The adoption of an artificial neural network with a resilient back-propagation training technique allows for highly accurate modeling of the non-linearity [27]. Dynamic congestion mechanism proposed forwarding rule that can be applied to select high-priority from the cloud service [28]. The role-mapping algorithm strategy reaches more saving in the amount of stored role-mapping rules that reduces the size of rule-store also minimizes the response time [29]–[31].

2. PROPOSED METHOD

2.1. Matrix arbiter

The MA produces the desired matrix for the input and output port, while every input port requests the same output port with the same priority. In that MA, locate the equivalent morsel, which is demanded the same output port. If assume the first states in the upper triangle of the MA are put to one. The diagram of the 4-bit MA is shown in Figure 1.

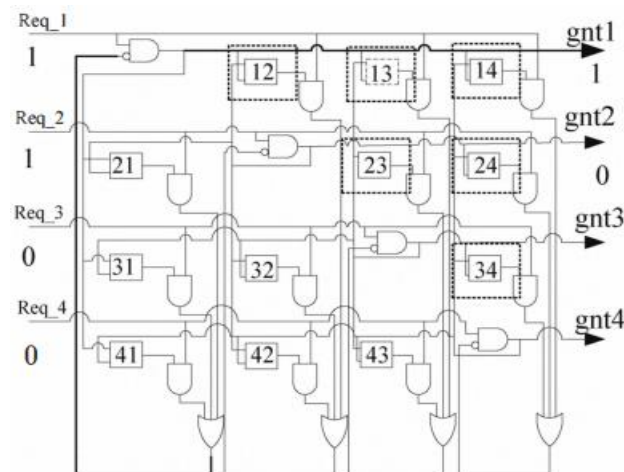


Figure 1. Matrix arbiter for 4-bit

Similarly, the elements in the lower triangle must be 0 based on the complementary principle. In the unique MA, the request 1(Req_1) has the highest priority, then request 2(Req_2), request 3(Req_3) and request 4(Req_4) has lowest precedence. MA produces control signals; hence meticulous choose line is selected, and input data is sent to the output port. The priority matrix of the arbiter is given:

$$\begin{bmatrix} X & W_{1,2} & W_{1,3} & W_{1,4} \\ W_{2,1} & X & W_{2,3} & W_{2,4} \\ W_{3,1} & W_{3,2} & X & W_4 \\ W_{4,1} & W_{4,2} & W_{4,3} & X \end{bmatrix}$$

In Figure 1, every block numbered 01, 02, 03, 12, 13, and 23 illustrate set-reset (SR) latch. Also, the position is continued in these SR latches in the higher triangular section of the matrix. All of the blocks numbered 10, 20, 30, 21, 31 and 32 in the subordinate triangular section of the matrix represent the complementary output of the transversely symmetric firm box.

2.2. Ping pong arbiter

The PPA is designed by connecting small arbiters in binary tree format. The 2-bit PPA consists of a number of AND, OR gates, and D flip-flops, as shown in Figure 2. Also, internal feedback flag signal f_i gives the past output as present input through the feedback process.

Initially, the 2-bit PPA gets a grant signal in the subsequent level; after that receives a valid grant signal in 2-bit PPA. The four-bit ping pong arbiter is created by using a three 2-bit PPA with some gates, as shown in Figure 3. So the arbiter gets a grant signal in each layer covered based on the parent arbiter's grant signal. Total arbitration time is very low in PPA.

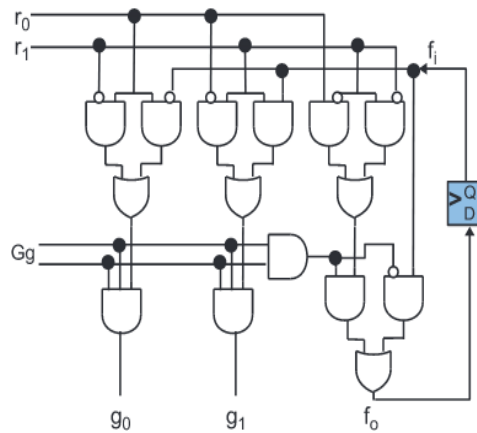


Figure 2. The 2-bit PPA

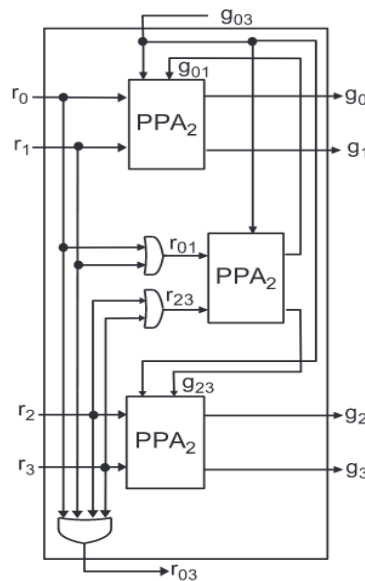


Figure 3. The 4-bit PPA

2.3. Distributive round robin arbiter

The DRRA consists of multiplexer (MUX) and counter unit, as shown in Figure 4. The selection line of the MUX is taken from the counter output. Also, the MUX output is given as enable signal of the counter. The MUX and counter size depend upon the number of input and output lanes. N number of input channels gives the request at a time. But only one input data is transmitted into the destination port based on the MUX's counter output or selection line. It provides low latency during the channel setup time when evaluated by all other classic arbiters. Only two components are used to construct the DRRA.

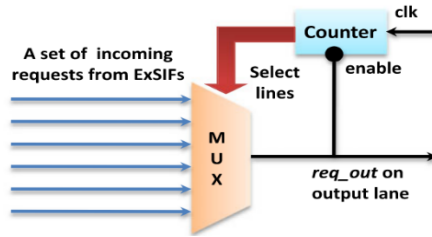


Figure 4. Circuit diagram of DRRA

2.4. Enhanced ping lock arbiter

The priority updating policy is altered in PPA and extended PPA to achieve fair arbitration. Restructure the superior level of arbiter in order to get the priority earlier than each input is processed in one round of arbitration. The uppermost index-based request is processed first to set the grant signal in order to achieve fair arbitration by conforming to the priority vector of the intermediate arbiter needs to be modernized. This work introduces novel 4-bit RRA architecture by combing a two-bit arbiter, also called enhanced ping lock arbiter (EPLA), as shown in Figure 5. The new grant updating policy is incorporated in EPLA for fair arbitration. The 2-bit PLA produces three outputs: grant signal (g), AG, eo, and lock output (lo).

This arbiter produces one extra output (i.e.) lo. Lo with AG signal is given to the parent arbiter. The grant signal is given to the parent arbiter when the AG signal is declared for lo. The priority register value is not changed in the next clock cycle. The lo signal of the 2-bit arbiter is declared to set the grant signal for any input request of the arbiter. The four-bit EPLA is constructed using two PLA2 leaf, shown in Figure 6.

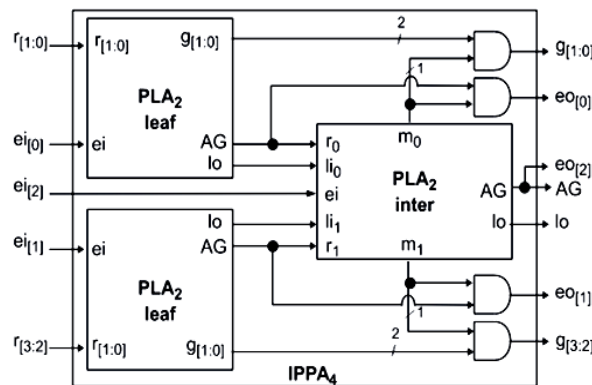


Figure 5. Circuit diagram of 4-bit extended PLA

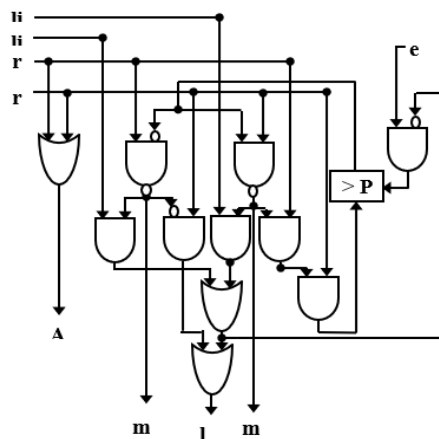


Figure 6. Circuit diagram of PLA2 inter

But the request of the next level arbiter is not granted. Because the feedback path is used in P register to control the output of EPLA. One PLA2inter is demonstrated in Figure 7 structure with four and gates. The proposed EPLA arbiter provides high speed, fair arbitration, low power, and compact chip size.

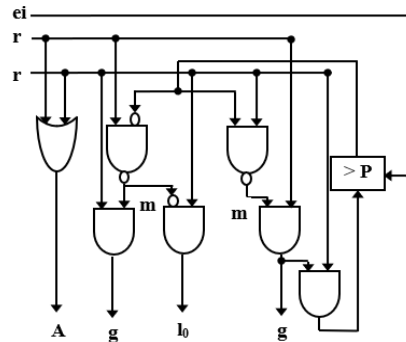


Figure 7. Circuit diagram of PLA2 leaf

3. RESULTS AND DISCUSSION

In this work, four types of arbiters, such as MA, DRRA, PPA, and EPLA, are constructed using Verilog HDL to check the functionality of all arbiters. Also, synthesized results are taken to analyze the area and delay product (ADP). The simulation output of EPLA is shown in Figure 8.

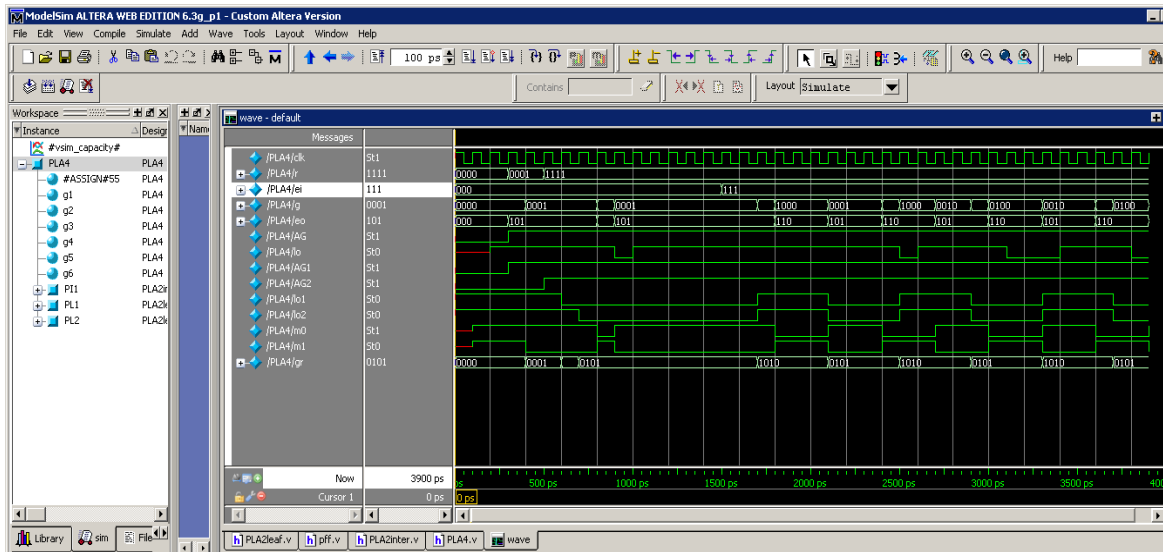


Figure 8. Simulation output of 4-bit extended PLA

From the output, clock, request (r), and input enable (ei) are inputs, and g, enable output (eo), AG, and lo are outputs. The clock signal is generated. When the entire request (r=0000) is zero, the corresponding grant is zero, and during ei is zero. After that, r=0001, and after one clock cycle, the corresponding g=0001. Finally, when the entire request is one (r=1111), and ei is one, the corresponding g is generated one by one sequentially (i.e.,) g=1000 for the first clock cycle, g=0001 for the third clock cycle, g=0010 for the fifth clock cycle and g=0100 at seventh clock cycle. Hence there is fair arbitration is achieved in EPLA. The synthesized results are evaluated to estimate the area, delay, and frequency of four types of arbiters and performance analysis is carried out based on the obtained result, as shown in Table 1. The analysis shows that the DRRA provides a smaller chip size than all other arbiters like PPA, MA and EPLA. But the speed is lower than PPA and EPLA. Furthermore, the DRRA arbiter has a lower delay compared to the EPLA and PPA arbiters. But the MA has a lower delay compared to all other arbiters.

Table 1. Comparison of four types of arbiters

Arbiters type	Slices	LUT	Parameters	
			Delay	Frequency
DRRA	11	21	3,897 ns	790,952 MHz
PPA	23	27	4,120 ns	910,345 MHz
MA	28	49	3,793 ns	-
EPLA	19	24	4,481 ns	855,918 MHz

The PPA offers high speed than all other states of art arbiters. Anyhow area is higher than DRRA and EPLA. Also, fair arbitration is limited. Matrix arbiter provides low delay, but the chip size is large. Finally, the EPLA requires a lower area than the matrix arbiter and PPA. But the chip size is more significant than DRRA. Fair arbitration (non-starvation) is fully achieved in EPLA. Also, performance is very high when compared to DRRA and MA.

4. CONCLUSION

In this paper, the high-speed compact arbiter is designed to attain fair arbitration. Several types of arbiters are studied for the common resource-sharing process. Four different kinds of arbiters MA, DRRA, PPA, and EPLA, are constructed to estimate the chip size, execution delay and speed of the arbiter. The arbiters are designed using Verilog HDL based on register transfer level implementation. The functionality of all kinds of arbiters is verified through ModelSim software. The Xilinx synthesized results calculate the area, delay, and speed. The DRRA is best for compact chip-size applications. PPA is used for high speed with fairness arbitration. MA is suited for low execution delay-based arbiter design. The EPLA is used for fair arbitration, small chip size, and high-speed applications. The ping lock RRA is incooperated with wireless network will be design in future.




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