Indonesian Journal of Electrical Engineering and Computer Science
Vol. 32, No. 3, December 2023, pp. 1476~1484
ISSN: 2502-4752, DOI: 10.11591/ijeecs.v32.i3.pp1476-1484

Improving graphics processing unit performance based on neural network direct memory access controller

Santosh Kumar[1], Neelappa[1], Saroja Bhusare[2], Veeramma Yatnalli[2]
[1]Government Engineering College Hassan, Visvesvaraya Technological University, Belagavi, India
[2]JSS Academy of Technical Education, Visvesvaraya Technological University, Belagavi, India

Article Info

Article history:

Received Jul 4, 2023
Revised Jul 19, 2023
Accepted Aug 12, 2023

Keywords:

Back propagation algorithm
Data transfer
Deep learning
Direct memory access
Graphics processing unit

ABSTRACT

In this paper proposes the design and implementation of the back-propagation algorithm (BPA) based neural network direct memory access (DMA) controller for use of multimedia applications. The proposed DMA controller work with the back propagation-training algorithm. The advantages of the BPA it will be work on the gradient loss w.r.t the network weights. So, this BPA is used as training algorithm for the DMA controller. The proposed method is test with the different workload characteristics like heavy workload, medium workload and normal workload. The performance parameters are considered here is like accuracy, precision, recall, and F1-score. The proposed method is compared with existing methods like convolutional neural network (CNN), recurrent neural network (RNN), long sort term memory (LSTM), and gated recurrent unit (GRU). Finally, the proposed design will give the better performance than existing methods.

Corresponding Author:

Santosh Kumar
Government Engineering College Hassan, Visvesvaraya Technological University
Belagavi, India
Email: skumars1803@gmail.com

1. INTRODUCTION

In the recent years, deep learning techniques are predominately used for various applications, so this will be huge attention at present in the industrial problems and academic research. For example, deep learning techniques used in many applications such as Image processing analysis for various problems either in medical [1], or used in speech recognition [2], and data analysis of various applications like sentimental analysis, predictions [3]. To use this type of deep learning techniques there will be a necessary to use the high-end intelligent systems are required for the better performance and to get accurate results. The benefit of using high-performance systems is that they can transport larger amounts of data from input/output (I/O) devices, read, and write the data to its proper destination. Most deep learning approaches necessitate frequent data transfers, which reduces the system's overall performance. To solve these problems authors proposed the many solutions; one of the solutions is direct memory access (DMA) controller. Mainly DMA will allow the certain blocks of data to transfer from peripherals to the memory unit without involving the central processing unit (CPU's). This method leads to reduce the load on the processors and there will be an improvement of system performance. In this paper, we will look at DMA controller approaches for various methods.

Aljumah and Ahmed [4] proposed the high-speed data transfer using the DMA controller. The DMA method is proposed by the advanced microprocessor bus architecture (AMBA). Here the proposed method works based on the asynchronous first in and first out. This controller is implemented in the verilog tool. The experimental result achieves the maximum frequency at 306.24 MHz and with maximum time of 3.265 ns. Lee *et al.* [5] introduced the method to improve the system performance with the help of avoiding memory channel

contention. This memory contention is removed between the CPU accesses and I/O accesses. In this work, authors also proposed the decoupled DMA. It provides the low-cost memory I/O accesses. Ponsard *et al.* [6] presented the configurable data placement mechanism. In this, authors used the adaptive DMA controller for the graphics processing unit (GPU) analysis. In this method, they have used the two-kernel model for large memory allocation for DMA operations. This method also tested for the workflow as hardware description language (HDL) synthesis. DMA engine with frequency of 266 MHz, which provides the 4K processing per 16×16 within 200 cycles, is discussed for the video codecs. The proposed DMA has less 4 nw power and showing less efficient in area [7].

Ahmed *et al.* [8] proposed the DMA based controller for multiple embedded systems. This controller has designed such way that it has integrated the system on chip (SoC) for exchange of large amounts of data. This DMA controller works based on the advanced microcontroller bus architecture (ADMA) specifications. The proposed method has made the comparison between different processors such as Cortex A8 and ZC702. The design comparison is done using the Xilinx DMA. Finally, authors made a conclusion that the proposed DMA method has alternative solution to the SoC. This proposed DMA architecture gives the good at improving the data transfer characteristics. Ma *et al.* [9] designed an efficient DMA controller for computing accelerators. The proposed method will give the high-end support to the high bandwidth during the movement of data. This method shows better performance related to the real time applications. Kobayashi *et al.* [10] shows the data movement controller using the graphics processing unit-field programmable gate array (GPU-FPGA) DMA method. The proposed method will realize the descriptor using the open computing language (OpenCL) kernel code. The proposed method shows the latency very low as 0.59 us. The method works under the high bandwidth up to 7.0 GB/s. Finally, authors concluded that the proposed method shows high performance in the GPU-FPGA computation. Hussain *et al.* [11] proposed the advanced pattern-based memory controller (APMC) for FPGAs. This controller supports for both regular and irregular memory patterns. The proposed memory controller will reduce the latency, which is caused by the irregular memory access patterns. The final results of the proposed system reduce the 20% less in hardware and 32% less on power of chips. Finally, this method achieves the 52x for regular and 2.9x speed for irregular applications.

Lu *et al.* [12] designed a DMA system using microcontroller unit to increase the data speed. This controller system will support the 8-channels system to replace the microcontroller unit (MCU) to transferring and to improve the system performance. Kobayashi *et al.* [13] shows the implementation of open enabled DMA controller for GPU-FPGA cooperative computation. This method is tested in the verilog HDL to the application of low-level components data transfer between two devices. This method achieved the latency of 0.6 μs. At last, authors concluded that the method will used for high performance GPU-FPGA systems. Song [14] and Chun *et al.* [15] successfully implemented the DMA controller for application of H.264 encoder.

In above introduction and literature review authors are discussed about the DMA controller methods for different applications. Still there is gap in the implementation of DMA control methods. So, in this work we proposed the back-propagation algorithms (BPA) based neural networks-based DMA controller to produce the adaptive structure and to increase in the data transfer in the GPUs and also the proposed method also compares with existing different DMA architectures. The paper is organized as follows: section 1 deals with the introduction to deep learning techniques and their applications, basic foundation of DMA methods, literature survey about DMA techniques with operation, benefits, and drawbacks. Section 2 will go over the proposed methodology. In section 3 will go over workload prediction and the BPA. In section 4 will go over the experimental and results analysis. Finally, in section 5, the paper is concluded.

2. METHOD

The proposed methodology having the computing system with integrated of both hardware and software tools. In the hardware system there will be FPGA based on direct memory access controller (DMAC), which is used to transfer to data to GPU. This technique has been developed in Python and implemented on the advanced RISC machine (ARM) Cortex architecture with a seamless communication interface. The module of the proposed system is shown in Figure 1.

2.1. System overview

The Figure 1 gives the full architecture of the proposed DMA system. It having two types of stages one is workload characterization and second one is memory access stage. In the first stage inputs is tuned by the low, medium and heavy workloads. It can be done by the back propagation neural network and is implemented through ARM Cortex core and its proposed DMA is designed in the FPGA [16].

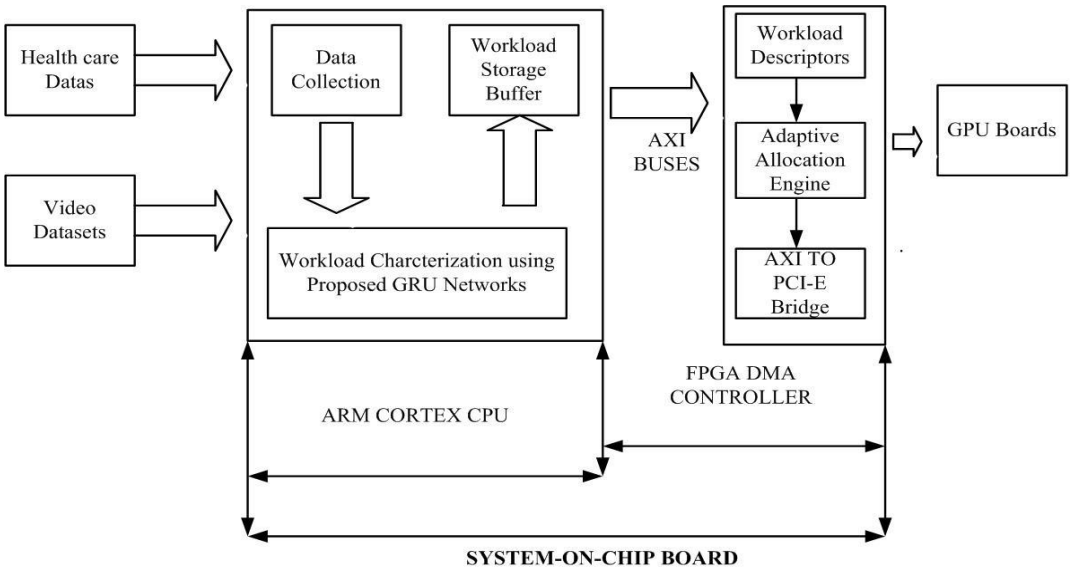

Figure 1. Block diagram for the proposed hybrid DMA controllers

2.2. Software based workload characterization

In the first phase of DMA workload system, increasing the load between the 10% to 50% of the maximum workload. The software tool is designed to enhance and delivers the maximum nominal type workload to achieve desired quality of service. To achieve this, we have used the parameter called scaling of operating frequency proportional w.r.t. to the nominal workloads with consider the reduction of power dissipation without breaking the required output. In the maximum operating frequency of the total system will be set to depending on the critical path delay, which corrects the reliability of the computation. Due to the scaling down of the frequency there will leads to delay in the critical path less than the clock toggle rate. The work load characterization methods also used in the workload prediction and variation scaling techniques.

3. WORKLOAD PREDICTION

To provide the accurate quality of service (QoS) as well as resource constraint privileges need consider the important parameters such work load. This work load should be predicted with respect to the each time. In general case the frequency and operating voltage of the system is predicted using the work loads. The various methods are used for the allocation of work load characterization like deep learning techniques [17], [18]. It this method authors classified as two types one is proactive and reactive. In this paper, BPA based neural network (BPA-NN) technique is used to in workload characterization to predict the suitable workloads for the GPU mechanism [16]. The authors used internet of medical things (IoMT), electronic design news magazine (EDN) embedded microprocessor benchmark consortium (EEMBC), and video analyzer data sets to train the proposed BPA-NN. The Table 1 shows the types of data sets and its features. To do the workload characterization and prediction analysis, the data set are should be arranged in such way that it should be instruction mix, with cache size, considering CPU time, prediction time and instruction pipelining are determined. Finally, these parameters are used to train the proposed BPA-NN. In the Table 2 shows the different workload parameters.

Table 1.Work loads using for training in BPA

Sl. No	Parameters of work load	Features of parameters
1	IoMT	It has features like heart rate variability, electrocardiogram (ECG), blood pressure, QRS (Q, R, S waves) detection, and standard sleep apnea detection
2	EEMBC	It has features of controller area network protocol (CAN) protocol, fast fourier transform (FFT), finite impulse response (FIR) filter, and pulse width modulation (PWM)
3	Video analyzing workbench	Institute of Automation, Chinese Academy of Sciences (CASIA) data sets

Table 2. Characterization of workload parameters

Sl. No	Workload parameters	Parameter terms
1	Usage of register	Uses the number of registers in the different work loads
2	Instruction mix	It is used for the addition of operations, storing of load and multiplication
3	Predictability of branch	It used for the branch statements in workloads
4	CPU cycle	It will take care the number of memory size used for storing the workload
5	Instruction pipelining	It is used as input workloads in pipelining stages

3.1. Backpropagation algorithm

In the neural networks, BPA is used and applied for various applications. The main advantage of the BPA is it will compute and calculated the gradient of loss function with to the network weights. Figure 2 shows the proposed networks with back propagation training algorithm its overview with working principle. The BPA work based on the gradient loss function for to each weight using the chain rule, finding gradient error for layer by layer and finally iterating backward form output layer to the input layer to reduce the redundant computation. The Figure 3 shows the basic structure of the neural network with BPA. It mainly consists of input layer, hidden layer and final output layer. It also uses the activation function with weight functions to train the network [19], [20].

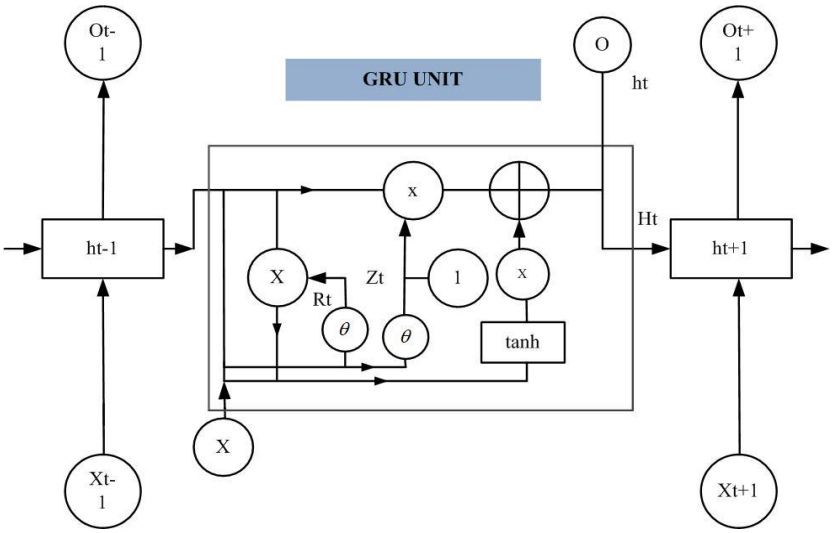

Figure 2. Proposed networks with back propagation training algorithm its overview with working principle

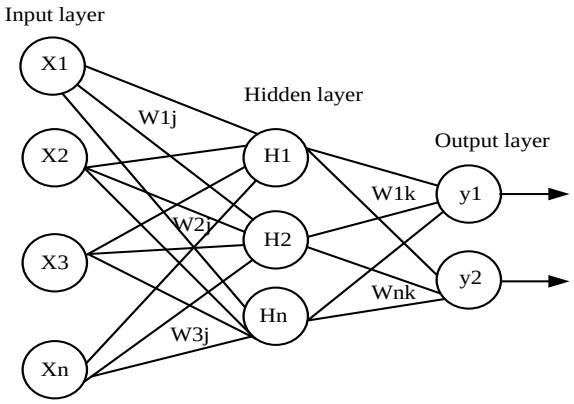

Figure 3. Structure of neural network with BPA

The steps involved in the neural network training using back propagation as follows. In the step 1 involves the initialization of weights with random values. In step 2 will do the stopping condition for the step 3 to step 10. In step 3 involves the feed forward training form input layers to the output layers. Transmitting

the input signals from input layer to the next layer will be done in the step 4. In step 5 calculated the weighted sum for each hidden layer which is used to calculated final net input. In step 6 shows the outputs w.r.t to each input and error should be calculated in the next steps. In step 7 calculated the output values from the output layer to the hidden layer to input layers along with weight values with activation function. In step 8 involves the updating of weight functions. In step 9 Test the stopping, condition which can be the minimization of error, number of epochs [21]–[24].

4. EXPERIMENTAL AND RESULT ANALYSIS

4.1. Experimental evaluation

To evaluate the experimental results for the proposed method, here Zynq-SoC-7000 series of FPGA is used. In this we have collected the different types of data sets which having the both videos and data. In first step, the data is formulated with fusion process with the video. This will be suited with other standards like IoMT and EEMBC, which is, benchmarked around 350,000 data sets. In the network, to solve the over fitting parameter to improve the performance generalization used the early stopping method. This stopping method is used to stop the training network when it is required to stop the training network. The experimental evaluation is done in two stages, one is first performance of proposed method with different workloads are calculated and analyzed. In the second stage, the proposed DMA structure is compared with the other different methods. The parameters are used for the comparative analysis is accuracy of training, time of computation, throughput and finally energy parameter.

4.2. Result analysis

4.2.1. Workload characterization metrics

The workload characterization parameters are analyzed for the proposed network is evaluated and compared with existing methods. The following parameters are considered to analyze the proposed method. The parameter is accuracy, recall, specificity, precision and F1-score. The formulation of these parameters is shown in Table 3. Here the true positive (TP) indicates the TP; true negative (TN) indicates the TN values, false positive (FP) and false negative (FN) shows as FN.

The proposed algorithm is analyzed using different performance metrics, which is in the form of workload characterization. The performance metrics considered in these works is like accuracy, recall, specificity, precision and F1-score. In Table 3 shows the performance metrics along with the mathematical formula. The Figure 4 shows the comparison of different algorithms with various parameters for heavy workload. Figure 5 shows the comparison of different algorithms with various parameters for medium workload. Figure 6 shows the comparison of different algorithms with various parameters for normal workload to analyze the proposed method characteristics the comparison of different algorithms like convolutional neural network (CNN), recurrent neural network (RNN), long short-term memory (LSTM) algorithm and gated recurrent unit (GRU) method. In case 1 shown in Figure 4 shows the performance of the heavy work load characterization for different algorithms. The accuracy of the CNN is 86, for RNN is 84 and F1-score of the CNN is 94.2. Kumar and Kumar [25] proposed for the GRU method F1-score is 96.1 but while taking the account of the proposed back propagation technique the accuracy is 85, precision is 87 and F1-score is 96.1. Therefore, for the heavy workload characterization the proposed has better performance than exiting methods.

The Figure 5 gives the workload characterization of medium workloads with considering the performance metrics. The accuracy of the proposed back propagation neural network for the medium workload is 84 and its precision is 86.2. Finally, F1-score of the proposed algorithm is 96.08. By observing, all the parameters the proposed BPA will give the good workload characterization performance. The Figure 6 shows the charts of normal workloads characterization, the accuracy of proposed algorithm is 94.5 and for the same precision parameter is 86.2. The F1-score for the proposed one is 95, which is good than the existing methods like CNN, RNN, LSTM, and GRU methods.

Table 3. Mathematical formulas for performance parameters

Sl. No	Metrics	Mathematical equation
1	Accuracy	$\frac{TP+TN}{TP+TN+FP+FN}$
2	Recall	$\frac{TP}{TP+FN} * 100$
3	Specificity	$\frac{TN}{TN+FP}$
4	Precision	$\frac{TN}{TP+FP}$
5	F1-score	$2.\frac{Precision*Recall}{Precision+Recall}$

In Figure 7 gives the comparative analysis of different methods with communication overhead w.r.t. batch sizes. By observing the waveforms in Figure 7 the existing direct memory access (E-DMA) method performance is little less while increasing the batch sizes. When compared to DMA methods the proposed method will give the better performance while increasing the batch sizes. The proposed method has less communication overhead while increasing the batch sizes from low values to high values. By comparing all the characterization workloads in different modes and waveform of communication overhead with different batch sizes, we concluded that proposed BPA will gives the best performance for the required inputs.

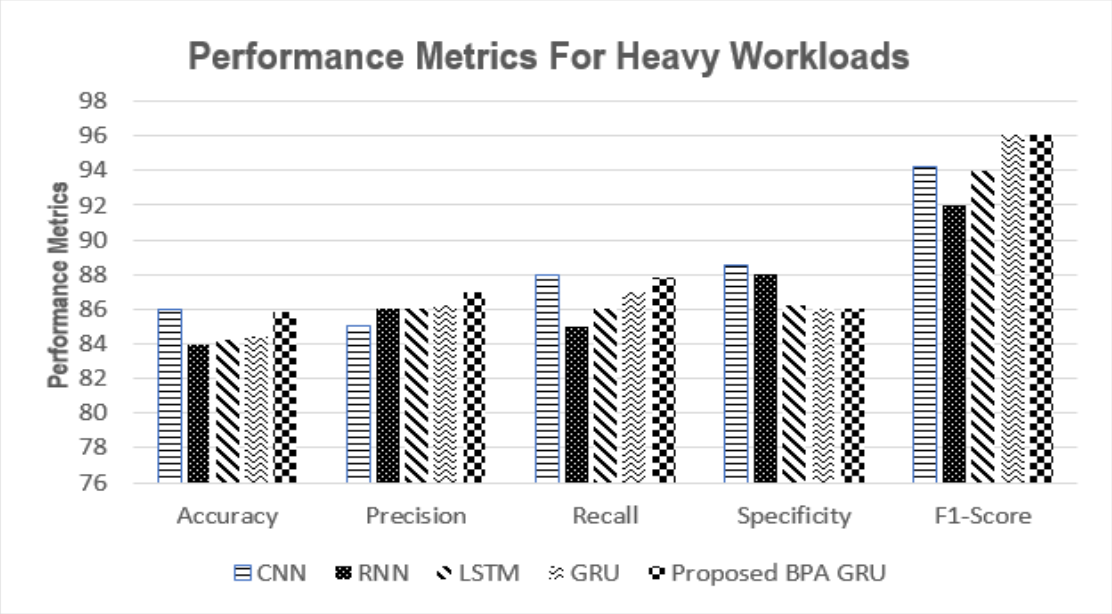

Figure 4. Comparison of different algorithms with various parameters for heavy workload

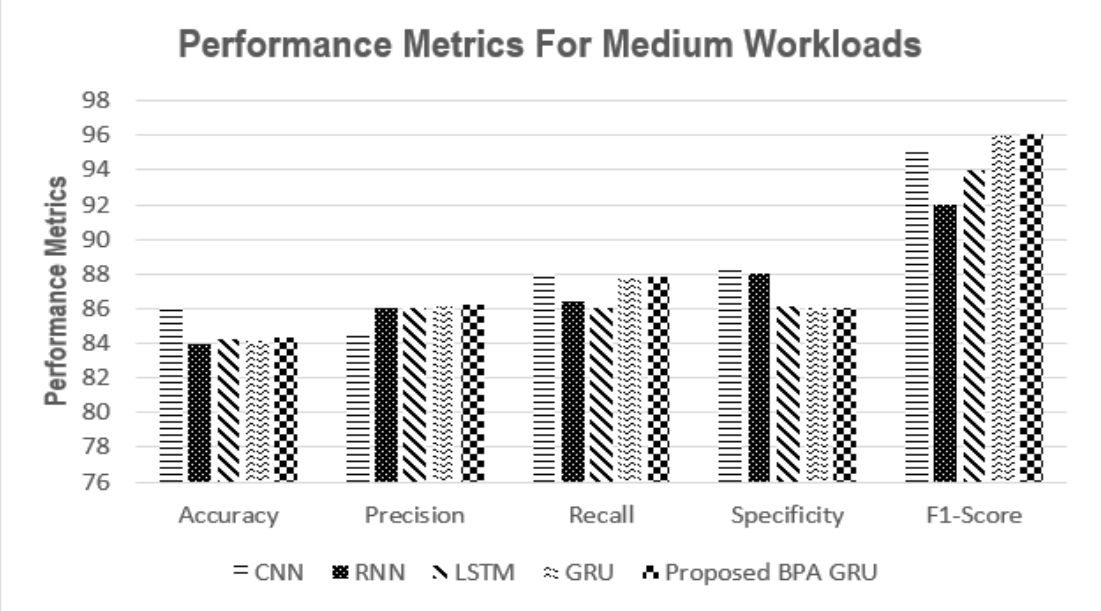

Figure 5. Comparison of different algorithms with various parameters for medium workload

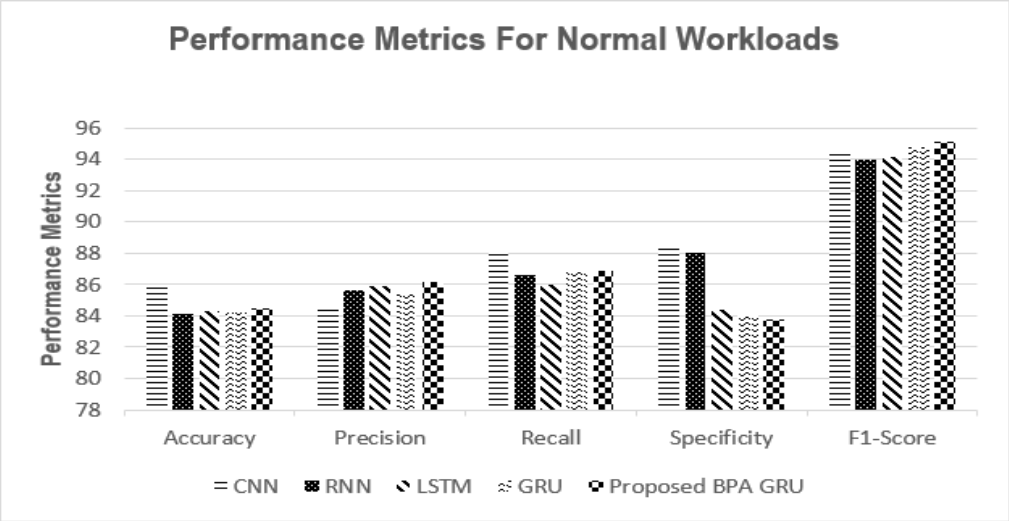

Figure 6. Comparison of different algorithms with various parameters for normal workload

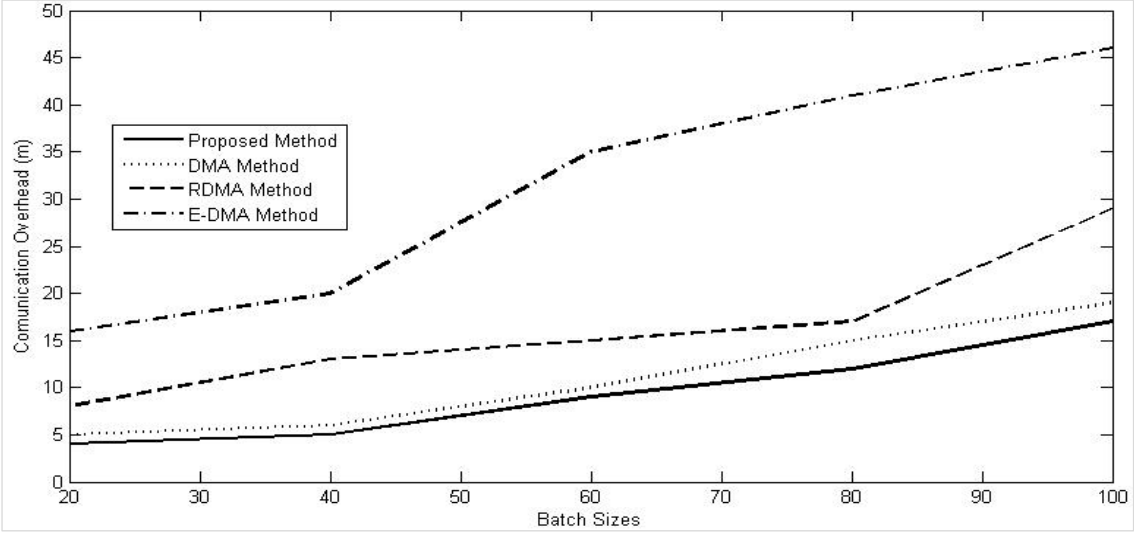

Figure 7. Analysis of communication overhead of different DMA's with the workload characterization

5. CONCLUSION

This work proposes a new DMA controller using the BPA neural network for the use of multimedia applications. The proposed system will used for the gradient decent formulation to train the network. In the performance metrics are used like accuracy, precision, and F1-score for the different characterization loads. Here three characterization types are considered one is a heavy work load characterization, medium work load and normal work load. The F1-score, accuracy of the different work load conditions for the proposed method are around 94.2 to 95. The accuracy of the proposed method is around 85 to 94.5 for different work load conditions. The proposed method also possesses the less communication overhead for small to large batch sizes than other exiting methods like CNN and RNN. So, because of these reasons the proposed methodology based DMA controller will has the very good response than other methods.

REFERENCES

[1] A. Krizhevsky, I. Sutskever, and G. E. Hinton, "ImageNet classification with deep convolutional neural networks (double)," *Communications of the ACM*, vol. 60, no. 6, pp. 84–90, May 2017, doi: 10.1145/3065386.

[2] G. Hinton *et al.*, "Deep neural networks for acoustic modeling in speech recognition: the shared views of four research groups," *IEEE Signal Processing Magazine*, vol. 29, no. 6, pp. 82–97, Nov. 2012, doi: 10.1109/MSP.2012.2205597.

[3] R. Collobert and J. Weston, "A unified architecture for natural language processing," in *Proceedings of the 25th international conference on Machine learning - ICML '08*, 2008, pp. 160–167, doi: 10.1145/1390156.1390177.
[4] A. Aljumah and M. A. Ahmed, "Design of high speed data transfer direct memory access controller for system on chip based embedded products," *Journal of Applied Sciences*, vol. 15, no. 3, pp. 576–581, Feb. 2015, doi: 10.3923/jas.2015.576.581.
[5] D. Lee, L. Subramanian, R. Ausavarungnirun, J. Choi, and O. Mutlu, "Decoupled direct memory access: isolating CPU and IO traffic by leveraging a dual-data-port DRAM," in *Parallel Architectures and Compilation Techniques - Conference Proceedings, PACT*, Oct. 2015, pp. 174–187, doi: 10.1109/PACT.2015.51.
[6] R. Ponsard, N. Janvier, D. Houzet, V. Fristot, and W. Mansour, "Online GPU analysis using adaptive DMA controlled by softcore for 2D detectors," in *Proceedings - Euromicro Conference on Digital System Design, DSD 2020*, Aug. 2020, pp. 436–439, doi: 10.1109/DSD51259.2020.00075.
[7] N. Nandan, "High performance DMA controller for ultra HDTV video codecs," in *2014 IEEE International Conference on Consumer Electronics (ICCE)*, Jan. 2014, pp. 65–66, doi: 10.1109/ICCE.2014.6775910.
[8] M. A. Ahmed, A. Aljumah, and M. G. Ahmad, "Design and implementation of a direct memory access controller for embedded applications," *International Journal of Technology*, vol. 10, no. 2, p. 309, Apr. 2019, doi: 10.14716/ijtech.v10i2.795.
[9] S. Ma, L. Huang, Y. Lei, Y. Guo, and Z. Wang, "An efficient direct memory access (DMA) controller for scientific computing accelerators," in *Proceedings - IEEE International Symposium on Circuits and Systems*, May 2019, vol. 2019-May, pp. 1–5, doi: 10.1109/ISCAS.2019.8702172.
[10] R. Kobayashi, N. Fujita, Y. Yamaguchi, A. Nakamichi, and T. Boku, "GPU-FPGA heterogeneous computing with OpenCL-Enabled direct memory access," in *Proceedings - 2019 IEEE 33rd International Parallel and Distributed Processing Symposium Workshops, IPDPSW 2019*, May 2019, pp. 489–498, doi: 10.1109/IPDPSW.2019.00090.
[11] T. Hussain, O. Palomar, O. Unsal, A. Cristal, E. Ayguade, and M. Valero, "Advanced pattern based memory controller for FPGA based HPC applications," in *Proceedings of the 2014 International Conference on High Performance Computing and Simulation, HPCS 2014*, Jul. 2014, pp. 287–294, doi: 10.1109/HPCSim.2014.6903697.
[12] C. Lu, H. Yang, and Q. Wu, "Design and implementation of a direct memory access controller based on microcontroller unit," *Journal of Physics: Conference Series*, vol. 2221, no. 1, p. 012016, May 2022, doi: 10.1088/1742-6596/2221/1/012016.
[13] R. Kobayashi, N. Fujita, Y. Yamaguchi, and T. Boku, "OpenCL-enabled high performance direct memory access for GPU-FPGA cooperative computation," in *ACM International Conference Proceeding Series*, Jan. 2019, pp. 6–9, doi: 10.1145/3317576.3317581.
[14] I.-K. Song, "A design of direct memory access (DMA) controller for H.264 encoder," *The Journal of the Korean Institute of Information and Communication Engineering*, vol. 14, no. 2, pp. 445–452, Feb. 2010, doi: 10.6109/jkiice.2010.14.2.445.
[15] I.-J. Chun, C.-G. Lyuh, T. M. Roh, and M.-S. Lee, "Performance improvement method of multi-port memory controller using an effective multi-channel direct memory access management," *Journal of the Institute of Electronics and Information Engineers*, vol. 51, no. 4, pp. 33–41, Apr. 2014, doi: 10.5573/ieie.2014.51.4.033.
[16] B. S. Kumar and E. K. Kumar, "Improving GPU performance in multimedia applications through FPGA based adaptive DMA controller," *International Journal of Pervasive Computing and Communications*, Oct. 2022, doi: 10.1108/IJPCC-06-2022-0241.
[17] K. Chen, D. Zhang, L. Yao, B. Guo, Z. Yu, and Y. Liu, "Deep learning for sensor-based human activity recognition: overview, challenges, and opportunities," *ACM Computing Surveys*, vol. 54, no. 4, pp. 1–40, May 2021, doi: 10.1145/3447744.
[18] T. Zhang, T. Zhu, K. Gao, W. Zhou, and P. S. Yu, "Balancing learning model privacy, fairness, and accuracy with early stopping criteria," *IEEE Transactions on Neural Networks and Learning Systems*, vol. 34, no. 9, pp. 5557–5569, Sep. 2021, doi: 10.1109/TNNLS.2021.3129592.
[19] N. Kamal, M. Andrew, and M. Tom, "Semi-supervised text classification using EM," in *Semi-Supervised Learning*, The MIT Press, 2013, pp. 32–55.
[20] Krizhevsky, I. Sutskever, and G. E. Hinton, "ImageNet classification with deep convolutional neural networks," *Communications of the ACM*, vol. 60, no. 6, pp. 84–90, 2017. doi:10.1145/3065386.
[21] A. V. Ooyen and B. Nienhuis, "Improving the convergence of the back-propagation algorithm," *Neural Networks*, vol. 5, no. 3, pp. 465–471, Jan. 1992, doi: 10.1016/0893-6080(92)90008-7.
[22] R. Rojas, "The backpropagation algorithm," in *Neural Networks*, Berlin, Heidelberg: Springer Berlin Heidelberg, 1996, pp. 149–182.
[23] L. Manjun and S. Zhu, "Improved back-propagation algorithm for neural networks," in *Proceedings of 1994 IEEE International Conference on Industrial Technology - ICIT '94*, 2002, pp. 293–296, doi: 10.1109/icit.1994.467110.
[24] J. Li, J. H. Cheng, J. Y. Shi, and F. Huang, "Brief introduction of back propagation (BP) neural network algorithm and its improvement," in *Advances in Intelligent and Soft Computing*, vol. 169 AISC, no. VOL. 2, 2012, pp. 553–558.
[25] S. Kumar B and E. K. Kumar, "A novel utilization-aware and power-delay-aware intelligent DMA controller for video streaming used in AI applications," *International Journal of Pervasive Computing and Communications*, vol. 18, no. 3, pp. 335–346, Jun. 2022, doi: 10.1108/IJPCC-11-2021-0280.

BIOGRAPHIES OF AUTHORS

Mr. Santosh Kumar received the Bachelor's degree in Electronics and Communication Engineering from Amritha Institute of Technology and Sciences of VTU in 2007. He received the Master degree in VLSI and Embedded Systems from Reva Institute of Technology of VTU in 2015. Currently he is Research Scholar of Department of Electronics and Communication Engineering, Government Engineering College, Hassan, Visvesvaraya Technological University. His research interests include embedded systems, IoT, artifical intelligence, and DMA controllers. He can be contacted at email: skumars1803@gmail.com.

Dr. Neelappa is an associate professor and head of the department at the Department of Electronics and Communication Engineering, Government Engineering College Hassan Karnataka, where he has been a faculty member since 2010. Dr. Neelappa graduated with a first-class B.E. degree in Electronic Engineering from Gulbarga University, Karnataka, in 1996, and an M.Tech. in Electronics Engineering from VTU in 2006. He completed his Ph.D. in VLSI and Signal processing from the VTU in 2017. His research interests are primarily image processing, signal processing and VLSI. He can be contacted at email: neel.m.dy@gmail.com.

Dr. Saroja Bhusare is an associate professor in ECE Department, JSS Academy of Technical Education, Bengaluru. She has done her M. Tech. in the year 2005 BMS College of Engineering, Bangalor and Ph.D. from VIT, Chennai in the year 2020. Her area of research interests includes, low power VLSI, and embedded systems. Several papers in international conferences and journals, mainly in VLSI, AI and ML, and embedded systems, add to her credit. She can be contacted at email: sarojasbhusare@jssateb.ac.in.

Dr. Veeramma Yatnalli is an associate professor in ECE Department, JSS Academy of Technical Education, Bengaluru. She has done her M.E. in the year 1998, from BVB College of Engineering, Hubli, Karnataka University Dharwad and Ph.D. from VTU in the year 2018. She is currently working as an associate professor in the Department of Electronics and Communication Engineering, JSS Academy of Technical Education Bengaluru, Karnataka, India affiliated to Visvesvaraya Technological University, Belagavi. Her area of research interests includes digital signal processing, communication and image processing. Several papers in international conferences and journals, mainly in image compression and reconstruction domain, add to her credit. She can be contacted at email: veerammayatnalli@jssateb.ac.in.