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Design analysis of moth-flame optimized fault tolerant technique for minimally buffered network-on-chip router

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ABSTRACT

A network on a chip is a solitary silicon chip utilized to perform the communication characteristics of large-scale (LSI) to very large-scale integration (VLSI) systems. Network-on-chip (NoC) architecture includes links, network interfaces (NI), and routers to unite with external memories or processors. NoC is designed to flow messages from the source module to the destination module through several links involving routing decisions. The design of NoC is complex and the buffer section's expensiveness creates problems while providing secured data service. Moreover, routers and links in NoC setups are liable to faults. This work introduces a minimal buffered router, and the faults in the network are optimized using moth flame optimized (MFO) fault-tolerant technique. The software named Xilinx ISE design suite 14.5 is employed for the minimum buffered router model. The suggested scheme is operated with less area, low power (0.241 mW), and high speed (965.261 Megahertz (MHz)) when matched with previous works.

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1. INTRODUCTION

The upsurge in VLSI advancements permitted the incorporation of high-level components and gate-level complexity in circuits over counters, register, multiplier, floating point unit, and arithmetical and logical unit (ALU) [1]. Another development named system-on-chip (SoC) is a VLSI chip framework with all required analog and advanced circuits, processors, and programming [2]. SoC innovation is utilized in little, progressively complex consumer electronic gadgets [3]. Such gadgets have more power in addition to memory than a common 10-year-old personal computer [4]. To meet the signal integrity and design efficiency difficulties of next-generation frameworks, an organized and adaptable interconnection design, named network-on-chip (NoC), has recently been suggested to moderate the SoC statement issue [5]. SoC communication is packet switched network (PSN) structured via a divisional approach termed NoC [6]. The packets are utilized to direct the data starting from source to goal in NoC [7]. Processing elements utilizing network topology comprise network interfaces (NI), interconnection links, and routers [8]. NoC enhances the scalability and power efficacy of complicated SoCs compared with additional communiqué subsystem models [9]. The architecture of NoC limits the area, number, length, power consumption of point-to-point connections, and interconnection wires [10].

Problem description: the general structure of the NoC router consists of many buffers, which occupy more area and consume more power [11]. Multiple cell upsets (MCU) is an isolated event that encourages

numerous bits in integrated circuits to fail simultaneously. A growing issue of MCU's caused by radiation and electromagnetic interference heavily affects the buffer section [12]. Plenty of solutions are available to overcome this issue and thus protect data storage [13]. But, most of them raise design complexity and expense of buffer section while providing secured data service [14]. In order to overcome this drawback minimally buffered router is used. Thus, reduced buffer usage reduces cost and improves design complexity [15]. NoCs are more susceptible to faults [16]. Faults in the NoC router are of 2 types [17]. They are transient faults and permanent faults. Many faults must be tolerated to sustain chip production yield and reliable operation [18]. Meanwhile, this emphasis on permanent NoC faults significantly influences routine [19].

Since the major portion of the router constitutes the cross-bar and the buffer, most faults occur there. This paper proposes an optimized fault-tolerant technique called moth flame optimization (MFO) to overcome faults. Hence the chief goal of this article is to boost the cost and security of data kept in buffers utilizing a low-performance effect. The remaining portion of this article is structured in the following way. Section 2 explains the proposed methodology. Subdivision 3 describes the results and discussion. Lastly, subdivision 4 specifies the overall conclusion. The contributions of this paper are as follows:

- To propose a minimal buffered router design that supports many faults in the network topology. NoC system should be fault-tolerant. This router occupies less area; it utilizes low power and provides high speed.
- When the packet comes across the faulty node, an alternate path is chosen by MFO fault-tolerant routing technique. Every moth has its fitness function esteem. The present node distance to the destination is calculated using the fitness function.
- The node's position is updated when the node identifies any fault in the route. The lowest fitness outcome selects the next node. If the node identifies no other faults in the network, it reaches the destination node without any loss. The process is repeated if a fault is identified until the destination node is reached.
- The Xilinx platform simulates the proposed techniques to analyse and verifies the proposed work by comparing it with several existing techniques. The proposed method was compared in terms of latency, average hops, and power consumption besides throughput and performed well when compared with existing methods.

The MFO algorithm represents a population-based nature-motivated process [20]. Venkataraman and Kumar [21] proposed an ant lion optimization (ALO)-based buffered router to diminish the consumption of power as well as area using extraordinary speed. The router design occupies less area, less power, and high speed. The abstraction model of NoC can be upgraded by means of ALO concerning the area as well as power. The number of flip flop, slices, and LookUp tables (LUTs) is with less value when compared to other techniques. NoC networks with large sizes remain susceptible to faults in routers and links. Priya *et al.* [22] developed fault-tolerant routing using the bypass route technique. The proposed system supports many faults, and an alternate bypass path between the immediate neighbours was formed around the faulty node. This technique has reduced latency and better reliability when compared to the baseline network. Thus, the routing methodology efforts to enhance the latency by way of creating a bypass path nearby a faulty node. Beechu *et al.* [23] proposed an efficient energy fault alert, fundamental mapping procedure. The mapping area was reduced, also measurement of communication vitality was performed by this approach. Identification of the faulty core is completed by failure probability if the occurrence of faults is identified in the mapping procedure. The overall communication vitality with essential metrics was minimized using the proposed algorithm. A routing process based on ALO performed in the bufferless router was proposed by Venkataraman *et al.* [24] to achieve reduced power. Predictable methodologies estimated the ALO-bufferless procedure. However, removal of the buffer of the router, there exists a steady decline in the area as well as power with the rise in functional speed. Thus, the bufferless-ALO design offers enhanced characteristics than the existing processes. To optimize the traffic in network, work-load aware routing (WAR) algorithm was proposed by Pano *et al.* [25] proficient in modifying hot spots in the network.

2. PROPOSED METHOD

In this work, minimal buffered router is proposed. If a dual number of packets deals with identical links, one among them gets diverted. The proposed router stocks the deflected flits per cycle. The routers at the corner, in addition to the edge transmit less traffic as considering the overall traffic load than the dominant ones. The schematic diagram representing the different steps of the minimal buffered router is shown in Figure 1. The proposed router utilizes a negligible pool of buffers to cope with the segments of misrouted flits. The input flits are conveyed via four interior flit networks through different elements of the pipeline router. The flits are put away in the resultant register pipeline around each clock cycle completion. The functioning of different units in the minimal buffered router is mentioned in the subsequent areas.

This is the diagrammatic portrayal of the two-phase router. Stage 1 comprises of hybrid ejection unit (HEU), flit pre-emption unit (FPU), and dual injection unit (DIU). Three units are there in stage 1. Furthermore, in arrange 2 there is a priority fixer (PF), a quadrant routing unit (QRU), permutation deflection network (PDN), and the buffer ejection unit (BEU). In this way, these are the two phases and the different practical units of the new router. The negligible buffered router incorporates 4 information ports, particularly N, S, E, and W. The pipeline registers are named A, B, and C. The design likewise incorporates 4 internal flit channels that encourage flits' movement via different pipeline router entities.

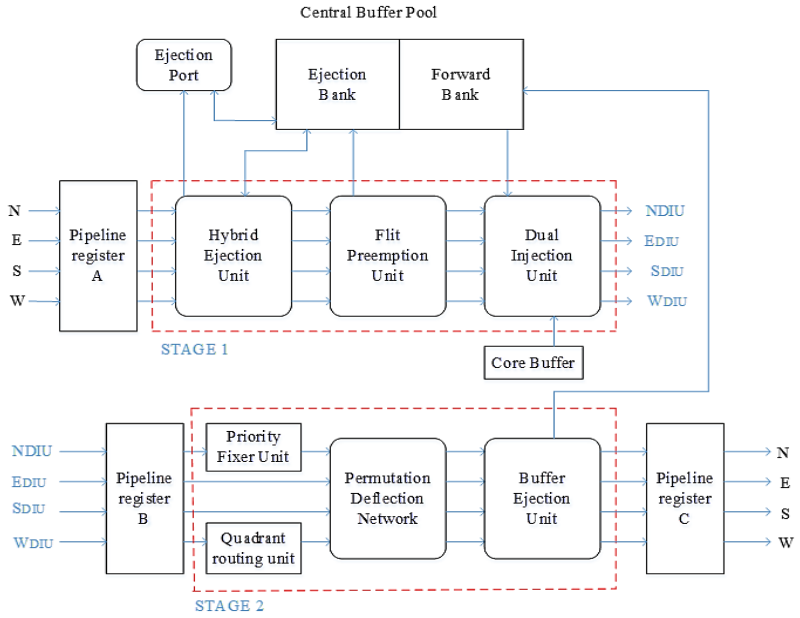

Figure 1. Minimal buffered NoC router

a) Stage 1

- HEU: towards the start of each cycle, flits commencing a few adjacent routers achieve information register pipeline A. Principal capacity of the pipeline register is to hold the data created in the past cycle. The flits moved to utilize the inside flit channel to the HEU. The hybrid ejection unit determines whether a flit is to be ejected, regardless of whether they are going toward the neighbourhood center. If the present cycle has a single ejection flit, the flit will be expelled after the interior flit channel and sent toward the discharge port. central buffer pool (CBF) is a mixture of an ejection bank (EB), just a forward bank (FB). If the EB is unfilled, HEU can deal with all considered dual flit ejections in a similar cycle. The flit to be emitted is moved towards the nearby discharge port and the next one to the ejection bank. At last, flits in EB move in the direction of the ejection port in the following process immediately.
- FPU: FPU takes an excess of one flit commencing the internal flit channel and puts it in CBP's forward bank. Then these pre-empted flits, in the end, come back to the router pipeline. By this acquisition, an unfilled opening is made in the inside flit channel with the goal that infusion or reinjection from the individual buffer can be restarted. This limit-based pre-emption avoids the overflow of the CBP and the center buffer.
- Core buffer and side buffer: core buffer stores flits from the neighbourhood hub. Center buffer flits are infused into the pipeline router by methods for the dual injection unit. Side buffer is utilized to store the pre-empted as well as diverted flits. The CBF will perform as a side buffer.
- Core buffer and side buffer: core buffer is utilized in order to store flits from the neighbourhood hub. Center buffer flits are infused into the pipeline router by methods for the dual injection unit. Side buffer is utilized to store the pre-empted as well as diverted flits. The CBF will perform as a side buffer.
- DIU: flits infused to DIU from the CBP's center buffer and forward bank. DIU infuses flit to the pipeline when any innermost flits remain inactive via a hybrid ejection unit. If there are at least two inactive spaces in the inward flit channel, also infused to the router from these buffers, thereby carrying out double infusion. In any case, if there is just one inactive space, preference is given for infusion from the forward

bank of CBP in odd cycles and from the center buffer in even cycles. DIU finishes stage 1 of pipeline router, and the flits achieve the pipeline register B.

b) Stage 2

- Priority fixer unit (PFU): these units guarantee the action and equity of the considerable number of flits in the pipeline register B. PFU figures priority value also destination statement for every flit in register pipeline B. Highest priority is given to flits close to the goal. PFU allots three various priority levels to be specific: priority level-1 (for flits inside 2-hop distance), need level-2 (for flits somewhere in the range of 2 and 4-hop distance), and priority level-3 (for flits more than 4-hop distance).
- QRU: the QRU performs like PFU. The destination address field is separated from every one of the flits in the pipeline register B. This unit is utilized to process the yield ports notwithstanding yield vector esteem. The yield vector determines the possible profitable ports for the flit.
- PDN: the priority esteems from FPU and the yield vector esteems from QRU are given to the PDN. PDN comprises 2×2 crossbar switches as well as is a parallel port designation unit. The yield port allotment happens in the PDN. Each switch in this system permits maximum priority flit to obtain hold of mentioned port, while others might be denied because of port conflict. Such flits will be taken away from the destination. With the end goal of diminishing the avoidance rate, one among such flits gets shifted to a side buffer.
- BEU: this unit utilizes the deflected flits. After the port allotment by PDN, the router recognizes the flits which are to be diverted. One of the redirected flits is moved to the side buffer with the target that it might get the ideal port in ensuing cycles. Remaining flits transfer to separate yield ports via register C pipeline. Flits are set apart to demonstrate which are allocated non-productive ports removed from the destination. Flits turning out from priority deflection network, buffer ejection unit to choose all things considered one checked flit for storing into side buffer. By this, we diminish the average deflection rate of the system, consequently cutting down undesirable flit movements in the system.

2.1. Rounding algorithm

The routing technique guarantees the message transfer from start to goal. The communication requirements of large SoCs are met by an emerging NoC design. While designing the circuit, faults tend to occur. Faults occur in the network frequently, which might link two routers defective. Hence, the situation is very challenging to avoid or else eliminate faults. The main objective is to make the NoC fault-tolerant.

2.1.1. Algorithm implementation

This article optimizes the routing procedure utilizing the moth flame algorithm. Hence to optimize the faults in the network, MFO fault-tolerant technique is proposed. MFO is the nature-inspired model. The navigation process of moths at night time is discussed here. Moth upholds a stable angle regarding the moon called transverse orientation. These moths are also trickled by false lights and attempt to keep up a comparative edge to the light source, and due to the nearby separation they get captured in a winding way.

The MFO allots moths to various arrangements in arrangement space of optimization issues, with every moth having its fitness function esteem. Every moth has a glow that stores the finest arrangement set up by that moth. In every cycle, the moths examine the arrangement space by flying via a winding way proximate to their glow and updating their positions. MFO begins with the positions of moths arbitrarily modified inside the arrangement space. The fitness estimations of moths are determined and considered the best individual fitness ideals. The proposed work is matched with the MFO algorithm. Here, moths are interchanged as nodes; for example, one moth is for each node, and the node's position is deliberated as moth position. The flame represents the position of the best node. The nodes consist of dimension D=3. The matrix equation for representing the position of the moth based on nodes as.

$$S_T = \begin{bmatrix} S_{T_{1,1}} & S_{T_{1,2}} & S_{T_{1,3}} \\ S_{T_{2,1}} & S_{T_{2,2}} & S_{T_{1,4}} \\ \vdots & \vdots & \vdots \\ S_{T_{n,1}} & S_{T_{n,2}} & S_{T_{n,3}} \end{bmatrix} \quad (1)$$

where number of nodes is 'n'. The present node distance to the destination is calculated using the fitness function. The fitness evaluation using (2) and the equivalent matrix for fitness calculation is given as (3) and the flame matrix offers the position of the neighbour node given in (4),

$$S_{T_1} = \sqrt{\left(S_{T_{d,1}} - S_{T_{1,1}}\right)^2 + \left(S_{T_{d,2}} - S_{T_{1,2}}\right)^2 + \left(S_{T_{d,3}} - S_{T_{1,3}}\right)^2} \quad (2)$$

$$U_{S_T} = \begin{bmatrix} U_{S_{I_1}} \\ \vdots \\ U_{S_{I_n}} \end{bmatrix} \quad (3)$$

$$P_T = \begin{bmatrix} P_{T_{1,1}} & P_{T_{1,2}} & P_{T_{1,3}} \\ P_{T_{2,1}} & P_{T_{2,2}} & P_{T_{1,4}} \\ \vdots & \vdots & \vdots \\ P_{T_{n,1}} & P_{T_{n,2}} & P_{T_{n,3}} \end{bmatrix} \quad (4)$$

the fitness value matric of the updated node is given in (5), the node position selected next in the route is given in (6) and the distance matric is given in (7);

$$U_{P_T} = \begin{bmatrix} U_{P_{P_1}} \\ \vdots \\ U_{P_{I_n}} \end{bmatrix} \quad (5)$$

$$S_{S_i T_j} = \left|T_j - S_i\right| * e^{bt} * \cos(2\Pi t) + T_j \quad (6)$$

$$D_{S_T} = \begin{bmatrix} D_{S_{S_1}} \\ \vdots \\ D_{S_{r_n}} \end{bmatrix} \quad (7)$$

The expression of power consumption during data transmission is given as (8), where, E_L denotes the energy consumption of interconnection links and E_R represents the energy consumption of interconnection routers. Finally, the nodes with lower values get selected as an alternative route if there is a faulty route. The procedure is repeated until the node reaches the target.

$$P = NE_R + E_L(N-1) \quad (8)$$

Figure 2 shows the representation of the MFO fault-tolerant technique. Let P be the packet that tend to move from source (0, 0) to destination node (3, 2) by taking subsequent path (0, 0) (1, 0) (2, 0) (3, 0) (3, 1) (3, 2). While considering the selected path, packet loss will occur if any of the nodes fails. When packet P is presented in (1, 0) and (2, 0) is a faulty node, the optimized fault-tolerant MFO will choose another path to avoid packet loss. By using the optimized fault-tolerant technique, the new path of packet P will be (0, 0) (1, 0) (1, 1) (1, 2) (2, 2) (3, 2). Congestion occurs in the network if the network's capacity is smaller than the number of packets sent to the network.

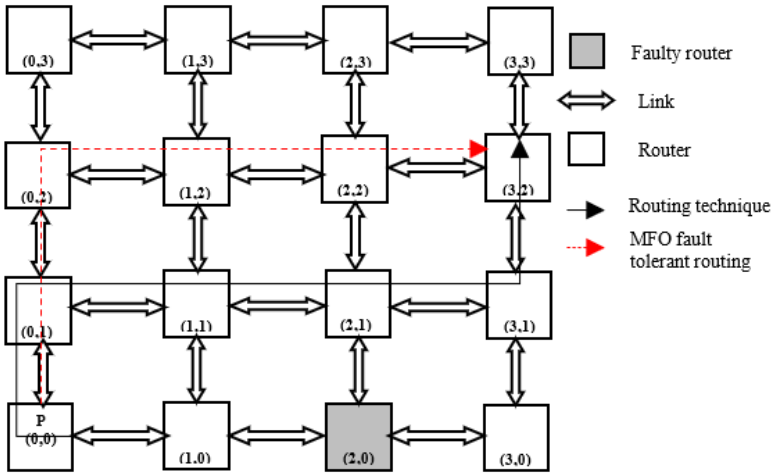

Figure 2. Routing process

The optimized fault-tolerant technique will classify congestion into 3 different levels: minimum, moderate, and maximum. When the packet P is in the node (1, 0), and so the node (2, 0) is faulty, the packets will choose another path (1, 0) (1, 1) to avoid packet loss. When the packet P is in a node (1, 1) the packets have two routes to reach the destination node. The optimized fault-tolerant technique will compare the congestion level of (1, 2) in addition to (2, 1) and choose (1, 2) as the minimum congested node than (2, 1). Thus, the path selected is (1, 1) (1, 2). Now if the packet P is in a node (1, 2) and the destination of the packet will also be in the same column, the packet will choose the path (1, 2) (2, 2). Finally, the packets will reach the destination node (3, 2).

2.1.2. Proposed method procedure

The proposed work ensures the transmission of packets without any loss. A network is initialized in the first step. The fitness value of each node is calculated using (2). The node's position is updated when the node identifies any fault in the route. The next node is selected utilizing the lowest fitness outcome. If the node identifies no other faults in the network, it reaches the destination node without any loss. The process is repeated if a fault is identified until the destination node is reached.

3. RESULTS AND DISCUSSION

The execution of suggested work is done on the structural register transfer level (RTL) using verilog; then simulation analysis is executed by Xilinx ISE 14.5 design suite. Virtex 4 XC4VLX80 is utilized for designing the suggested router. RTL observation of this model is shown in Figure 3.

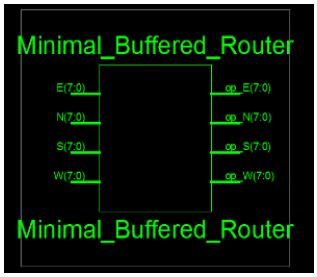

Figure 3. RTL view of minimal buffered router

The grouping of inputs in the proposed methodology is done by communication volume. This is obtained with transmission message competency. The packets tend to move from source to destination. When anyone node fails, another route is selected based on the node with a low congestion level. The packets will reach the destination node without any loss if no other fault is identified. Figure 4 shows the simulation result of minimal buffered NoC.

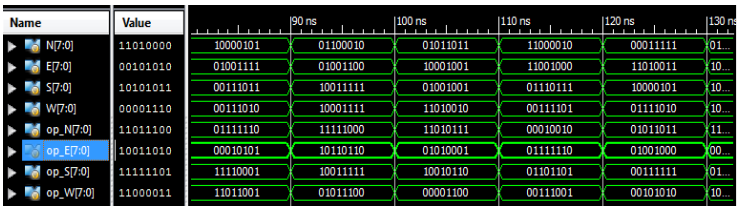

Figure 4. Proposed NoC simulation

Figure 5 displays an area and frequency comparative analysis. The analysis of the area in addition to frequency comparison, is exposed in Figures 5(a) to 5(d). It is obvious from the above-mentioned graphs that the proposed method shows improved performance. A total number of slices, in addition to LUTs, and flip flops, is the logic employed to evaluate the area. This assessment shows that the proposed method offers less area and high operational frequency (965.261 MHz) while related to existing approaches, namely bypass route-based fault-tolerant routing [22] with frequency 215.825 MHz, ALO-based buffered routing [21] with frequency 426.995 MHz, ALO based bufferless routing [24] with frequency 780.153 MHz.

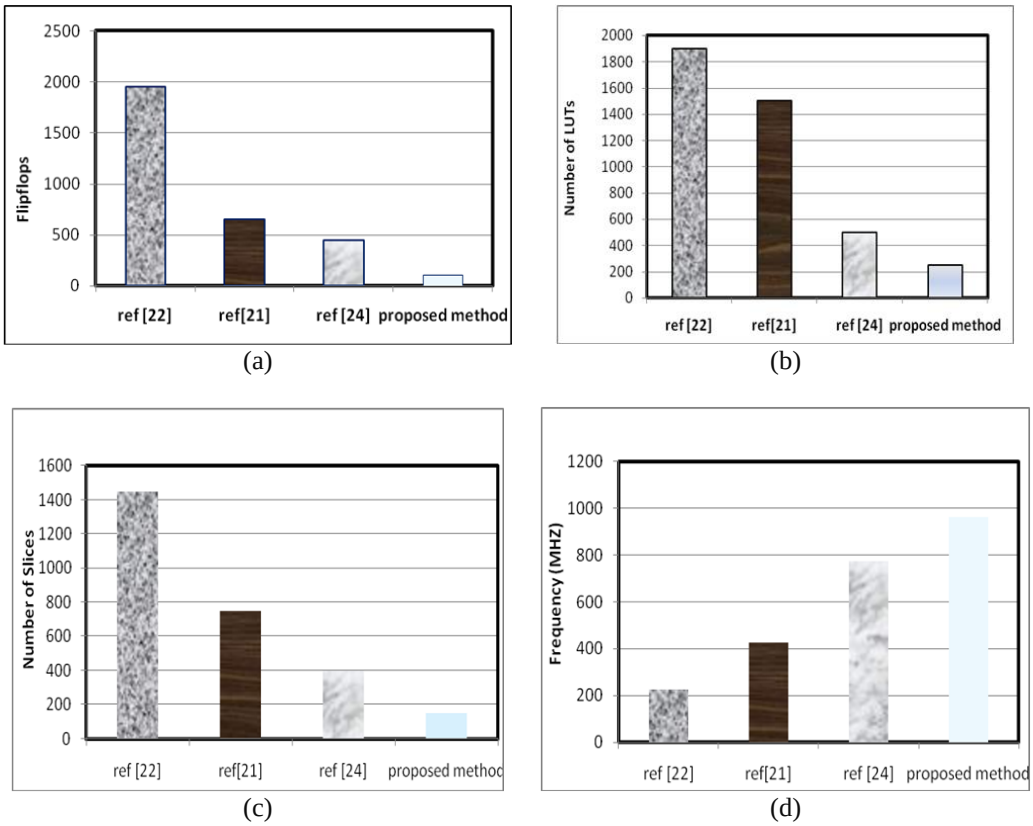

Figure 5. Area and frequency comparative analysis; (a) number of flip flops, (b) number of look-up tables, (c) number of slices, and (d) frequency

Figure 6 shows the power consumption compared with various techniques and Figure 7 shows the representation of throughput vs fault rate. From Figure 6, the proposed MFO fault-tolerant routing consumes a power value of 0.241 mW. In addition, the power values of the existing techniques include bypass route-based fault-tolerant routing (0.978 mW), ALO buffered routing (0.752 mW), and ALO bufferless routing (0.413 mW). From the given graph, it is evident that the proposed work consumes less power.

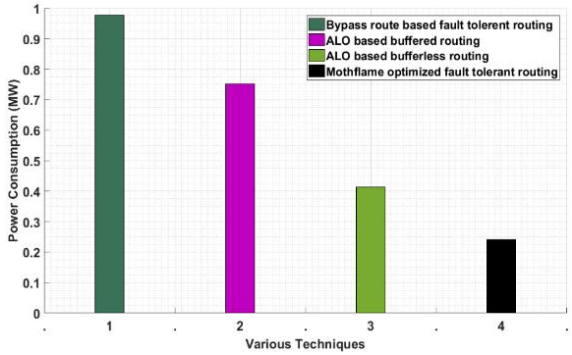

Figure 6. Power consumption vs various techniques

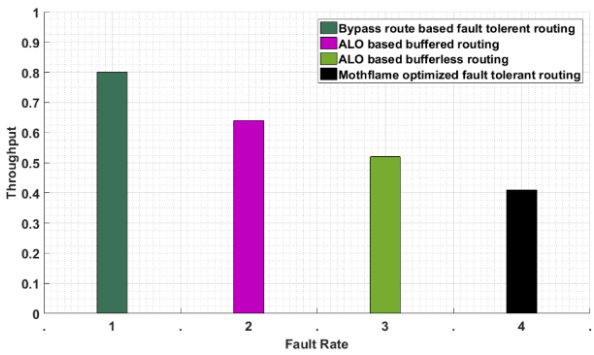

Figure 7. Throughput vs fault rate

From Figure 7, the throughput value increases depending on the fault rate. The throughput is higher if there is no fault in the network. In the presence of faults, the throughput is lower. However, the proposed MFO fault-tolerant routing works better regarding throughput. Figure 8 illustrates the average hop count vs fault rate. The measure of two host networks expresses hop count. In the presence of a faulty node, the packet cannot reach its destination. So, the node will choose another route depending on the fitness value.

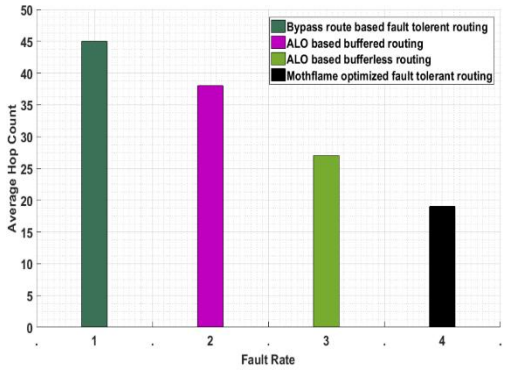

Figure 8. Average hop count vs fault rate

Figure 9 represents the average packet latency vs packet injection rate. The packet injection rate is the amount of packets every node injects during each cycle. The average packet latency is the average latency of packets. Figures 9(a) to 9(c) represents the number of faults 1, 2, and 3. For every fault in the network, the average packet latency is varied concerning packet injection rate.

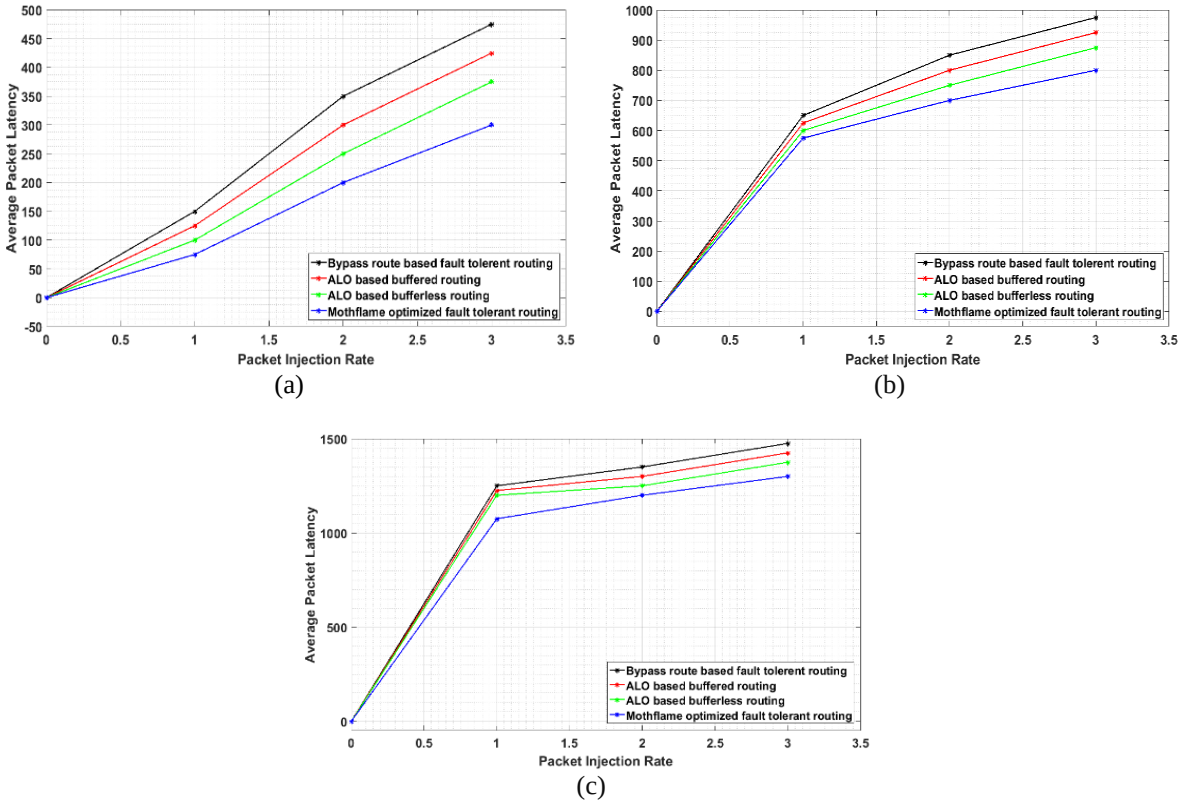

Figure 9. Represents the average packet latency vs packet injection rate; (a) 1 fault, (b) 2 fault, and (c) 3 fault

Loss in packets causes errors in data transmission. Packet loss is measured as a percentage of packets lost concerning packets sent. Figure 10 is the packet loss rate vs a number of faults. If the packet fails to reach the destination, then packet loss occurs. The packet loss rate is less when compared with the existing methods. Table 1 displays the performance improvement of planned work compared to previous techniques. Parameters like latency, average hops, power consumption, and throughput is compared with existing methods, namely fault-tolerant routing based on bypass route, ALO-based buffered routing, then ALO-based buffered routing.

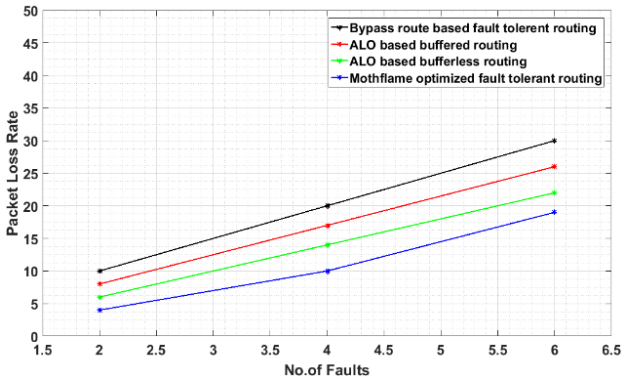

Figure 10. Packet loss rate vs number of faults

Table 1. Comparison of various parameters

Existing vs proposed method	Latency	Average hops	Power consumption (mW)	Throughput (Gbps)
Bypass route-FTRc [22]	0.93%	1.92%	0.978	26%
ALO-buffered routing [21]	0.72%	1.76%	0.752	19.6%
ALO-bufferless routing [24]	0.51%	1.63%	0.413	14%
MFO fault-tolerant routing	0.32%	0.08%	0.241	10%

4. CONCLUSION

Faults occur in the network frequently, which might link two routers defective. Hence, the situation is very challenging to avoid or else eliminate faults. The main objective is to make the NoC fault-tolerant. This paper discusses the design of a minimal buffered router with MFO fault-tolerant routing that supports many faults in the network topology. When the packet comes across the faulty node, an alternate path is chosen by MFO fault-tolerant routing technique. The router's design occupies less area, has low power, and has high speed. The frequency scope of the proposed scheme is extremely high (965.261 MHz), latency is low (0.32%), low average hops (0.08%), low throughput (10%) and power consumption is low (0.241 mW) observed from this work. The abstraction model of NoC is upgraded by power and area using the MFO technique. XilinxISE14.5 design suite is utilized for designing the proposed scheme. The proposed method was compared in terms of latency, average hops, and power consumption besides throughput and performed well when compared with existing methods. In the future, testing multi-level and 3D topologies and analysing additional workloads will be done for further enhancement.

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