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Cascaded H-bridge multilevel inverter-based DSTATCOM with an artificial neural fuzzy inference systembased controller

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ABSTRACT

In this paper, a voltage source inverter is utilized as a distributed static compensator (DSTATCOM). The DSTATCOM is used for the elimination of harmonics caused by the nonlinear load. The reference currents of DSTATCOM were estimated with a synchronous reference frame (SRF). Conventionally, the SRF uses voltage, load current and filter current to compute the reference current to track desired source current for DSTATCOM. The sliding mode controller and feedback linearization are used to design the current controller. The feedback linearization technique and sliding mode control are used to cancel nonlinearities and offer invariant stability due to modeling uncertainties due to the DSTATCOM parameter and external load disturbance. The sliding mode controller requires a rigorous mathematical model of the system. To overcome this, an artificial neuro-fuzzy inference system (ANFIS) is devised for the control of DSTATCOM. The training data of the ANFIS controller is generated from the sliding mode controller algorithm. The overall system of DSTATCOM including the ANFIS algorithm is implemented in MATLAB/Simulink SimPower block sets. The simulated response of DSTATCOM was found to be improved and better than the sliding mode controller scheme.

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1. INTRODUCTION

Multilevel inverters (MLIs) are now frequently used in situations requiring medium to high power conversion [1]. The multilevel inverter offers low voltage stress on the switching devices, low total harmonics distortion and improved electromagnetic compatibility [2]. Multilevel inverters can be categorized as voltage source inverters or current source inverters based on their configuration [3]. The current source inverter-based multilevel inverter has a high fault-tolerant capability. Any short circuit does not lead to complete damage to the inverter and a short circuit is incomplete by the dc link inductor [4]. However, the current source inverter requires a bulky inductor and commutation capacitor, which will make the system bulky [5]. The voltage source inverter based multilevel requires only a capacitor on its dc side and the size of the inverter system is less as compared to the current source inverter.

Hence, voltage source inverter-based multilevel inverters are used in most medium to high-power applications. The voltage source inverter base can be categorized as: i) a cascaded H-bridge MLI (CHB MLI), ii) a neutral point clamped MLI (NPC MLI), and iii) a flying capacitor MLI (FC MLI) [6], [7]. The CHB-MLI is most preferred due to the complexity posed by the neutral point clamped and flying capacitor multilevel inverter [8]–[10]. The advantages of the CHB MLI are that any number of voltage levels can be realized with the addition of small voltage sources [11]–[13]. The cascaded multilevel inverter reduces the

requirement of the switching device and the modular structure makes the system more suitable for high-power and high-voltage applications [14]. Some of the applications of the cascaded multilevel inverters are reactive power compensation, photovoltaic conversion, active power filter, magnetic resonance imaging, and synchronous compensator [15]. Potential applications are electric and hybrid trains [16].

In literature, many control schemes have been reported for the distributed static compensator (DSTATCOM) [17]. Most of the control strategies are includes Fryze power theory, synchronous reference frame (SRF) theory, p–q theory, nonlinear control technique and Lyapunov function based control theory [18]. Numerous soft computing methods, such as the fuzzy logic approach, neural network (NN), and artificial neuro-fuzzy inference system (ANFIS), have been developed in addition to these, estimation of the reference current and generation of switching signals of DSTATCOM [19]. To power, the voltage source inverter-based bespoke power devices, Hopfield NN, iterative learning control, the quantized kernel least mean square, radial basis function networks, and feed-forward training are used. Among them, the most commonly used control schemes for DSTATCOMs are SRFs and instantaneous reactive power theory. In this paper, the SRF is used for the reference current estimations of DSTATCOM. In this paper, an ANFIS-SRF-based reference scheme is proposed for the elimination of harmonics and reactive for DSTATCOM. A control theory based on the ANFIS-SRF-based algorithm used is for the control of DSTATCOM. The performance of DSTATCOM with a sliding mode controller-based algorithm is evaluated through a computer MATLAB simulation study.

2. TOPOLOGY OF DSTATCOM

The distributed static compensator topology based on the CHB MLI is shown in Figure 1. Figure 1(a) shows the single diagram for DSTATCOM. Figure 1(b) shows the CHB MLI. The three-phase coupling inductor, six dc link capacitors, and twenty-four insulated gate bipolar transistors make up the DSTATCOM circuit. The DSTATCOM is linked to the PCC through an interfacing inductor. The interfacing inductor suppresses the switching ripple caused by the operation of DSTATCOM. The dc link capacitor is used to minimize the ripple caused by the DSTATCOM. Additionally, harmonics current elimination and reactive power correction use the inductor and capacitor's energy balance. The three-phase diode bridge rectifier implements the non-linear load circuit. The diode bridge rectifier generates the stepped waveform, which contains triple harmonics currents. The current caused by the diode bridge rectifier is used to create the lagging power factor [20].

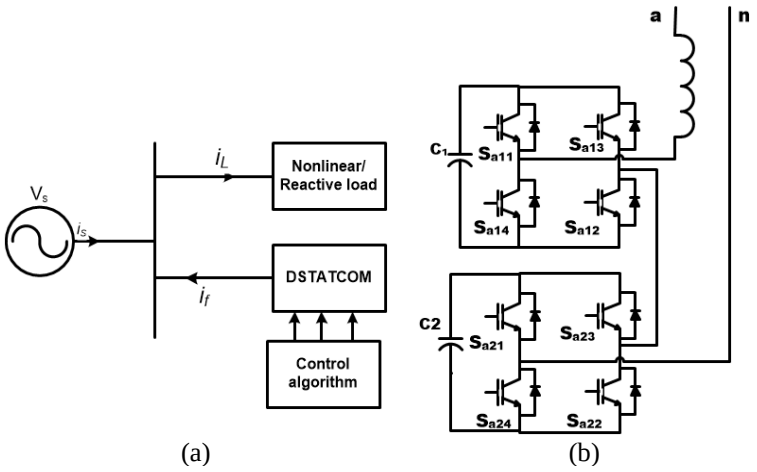

Figure 1. CHB MLI-based DSTATCOM topology (a) single line diagram of DSTATCOM and (b) CHB MLI

The DSTATCOM inverter circuit, which is used for the compensation of harmonics pollution caused by nonlinear, is realized with CHB MLI multilevel inverter. The CHB MLI multilevel inverter is realized with the addition of small voltage sources in series/parallel combinations. The power circuit of DSTATCOM is realized with an insulated gate bipolar transistor, interfacing inductor, and capacitor. The filtering of switching frequency harmonics brought on by the functioning of the CHB MLI inverter is done using the interface inductor.

3. SYNCHRONOUS REFERENCE FRAME

Figure 2 shows the SRF theory, this theory used for controlling the DSTATCOM. The Iaf, Ibf, and Icf are the compensating currents, IaL, IbL, and IcL load currents. Voltage regulator regulated voltage and balanced DC-link voltage. The low pass filter reduced low-order harmonics. The comparator compared the reference and actual values. The clarks and inverse clark transformation theory is used for abc to dq and dq to abc transformation.

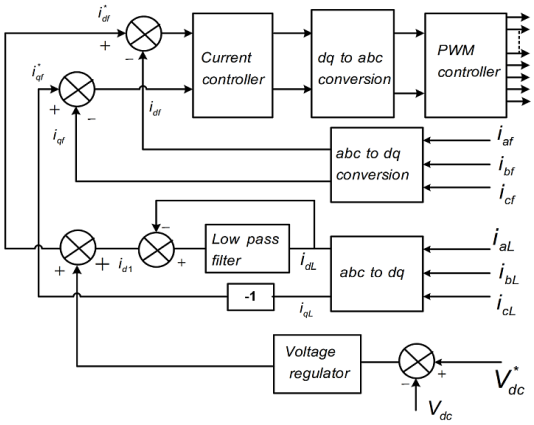

Figure 2. Synchronous reference frame

$$L_2 \frac{d}{dt} i_{af} = e_a - R_2 i_{af} - v_{af} \quad (1)$$

$$L_2 \frac{d}{dt} i_{bf} = e_b - R_2 i_{bf} - v_{bf} \quad (2)$$

$$L_2 \frac{d}{dt} i_{cf} = e_c - R_2 i_{cf} - v_{cf} \quad (3)$$

Where R_2 and L_2 stand for the active power filter line reactors' respective resistance and inductance. Three-phase voltages, currents, and switching operations can be converted to a d-q-o spinning frame. This outcome,

$$\begin{bmatrix} x_d \\ x_q \\ x_0 \end{bmatrix} = \begin{bmatrix} sin\,\theta_e & sin\left(\theta_e - \frac{2\pi}{3}\right) & sin\left(\theta_e + \frac{2\pi}{3}\right) \\ cos\,\theta_e & cos\left(\theta_e - \frac{2\pi}{3}\right) & cos\left(\theta_e + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \quad (4)$$

where x stands for currents, voltages, or switching functions, and is the θespinning frame's transformation angle. The state model in the revolving frame can be expressed as follows using (1) through (4):

$$L_2 \frac{d}{dt} i_{df} = e_d - R_2 i_{df} + \omega_e L_2 i_{qf} - v_{df} \quad (5)$$

$$L_2 \frac{d}{dt} i_{qf} = e_q - R_2 i_{qf} - \omega_e L_2 i_{df} - v_{qf} \quad (6)$$

where ω_e is the location of the power system's frequency, and what does it mean when "d" and "q" are used to indicate, respectively, the parts of the d- and q-axis in the revolving frame equations. The active power fitter's block diagram and the power converter's input voltage instructions will be derived using (5) and (6). Let the phase voltage angle equal the transformation angle, e. Assume that the voltages in the three phases are balanced [21]–[24]. These result in the voltage components: e_d=V_m and e_q=0, where V_m denotes the maximum utility phase voltages. When the power system's phase voltages are balanced, the only variables that affect pL and qL, respectively, are i_{dL} and i_{qL}. The IRP P_s and reactive power q_s from the power system can be written as follows for an active power filter system that fully compensates for harmonic current:

$$P_s = \frac{3}{2} V_m i_1 \& q_s = 0 \tag{7}$$

when using a low pass filter, the basic component of the load current can be extracted from the d-axis current (i_{dL}). The active power filter's matching reference currents in the rotating frame is (8):

$$i^*{}_{d\,f} = i_1 - i_{dL} \& i^*{}_{q\,f} = -i_{qL} \tag{8}$$

the (8) is derived from the innovative calculation approach for reference currents of the active power filter that is proposed, using a digital low pass filter, reference frame transformation, and load current feedback. It should be emphasized that regardless of whether the load is balanced or not, the reference currents can be determined by simply deducting the fundamental component from the measured load currents.

3.1. Feedback linearization to design the current controller

The dynamic mathematical model of CHB-MLI-based DSTATCOM in the d-q reference frame is as follows:

$$V_{dinv} - R_f i_{ds} - L_f \frac{di_{ds}}{dt} + \omega L_f i_{qs} - V_{ds} = 0 \tag{9}$$

$$V_{qinv} - R_f i_{qs} - L_f \frac{di_{ds}}{dt} + \omega L_f i_{ds} - V_{qs} = 0 \tag{10}$$

where, V_{dinv} and V_{qinv} are inverter voltages, i_{ds}, i_{qs} and V_{ds}, V_{qs} are source voltage and current respectively. Consider the standard linear state space equation as (11).

$$\frac{dx_d}{dt} = w_d(x) + z_d(x) u_d \tag{11}$$

The highly coupled and non-linear CHB-MLI DSTATCOM mathematical model can be converted into the linear decoupled mathematical model (9) and (10) using the state space model (11). Therefore, the state space model consisting of the system matrix, input matrix, variable matrix and input control matrix are represented as:

$$w_d(x) = \begin{bmatrix} -\frac{R_f}{L_f} i_{ds} & +\frac{X_f}{L_f} i_{ds} & -\frac{1}{L_f} V_{ds} \\ -\frac{R_f}{L_f} i_{qs} & +\frac{X_f}{L_f} i_{qs} & -\frac{1}{L_f} V_{qs} \end{bmatrix} X = \begin{bmatrix} i_{ds} \\ i_{qs} \end{bmatrix}$$
$$z_d(x) = \begin{bmatrix} \frac{1}{L_f} & 0 \\ 0 & \frac{1}{L_f} \end{bmatrix} U_d = \begin{bmatrix} V_{dinv} \\ V_{qinv} \end{bmatrix} \tag{12}$$

after feedback linearization, the CHB-MLI-based DSTATCOM system can be represented for obtaining inverter control input U_d as:

$$U_d = \left(-z_d^{-1}(x) \times w_d(x)\right) + \left(-z_d^{-1} \times \lambda_d\right) \tag{13}$$

where, λ_d is used to represent the state vector matrix as:

$$\lambda_d = [\lambda_{11} \quad \lambda_{12}]^T \tag{14}$$

for the CHB-MLI-based DSTATCOM system, the output states are as:

$$Y_d = [i_{ds} \quad i_{qs}]^T \tag{15}$$

3.2. ANFIS model overviews

The mixed ANFIS model has been used to address the nonlinear load's power quality issue. The expert and flexible learning capabilities of neural networks are combined in the ANFIS model. To get rid of the harmonics brought on by the non-linear, the model generates toggling control pulses. Here, the error

signal is calculated by contrasting the reference signal with real signals that have been measured. Moharana and Dash [25] the ANFIS uses hybrid modulation to control the error signal and produce the necessary switching sequence. The proposed ANFIS represents an error (E) and the rate of change in error CE or d(E/dt) are the inputs. A common rule set for a zero-order Sugeno fuzzy model is created with two fuzzies, and it is described below.

f1=A1 (E)+B1 (CE)+C1 if X1 and CEV is Y1, and f2=A2 (E)+B2 (CE)+C2 if EV is X2 and CEV is Y2. X1, X2, Y1, and Y2 are used to indicate the nonlinear parameters in place of M1, M2, N1, N2, C1, and C2 which are used to represent the linear parameters. The fuzzy reasoning is depicted in the following figure. The five tiers that make up the ANFIS system, in general, are the fuzzy layer, product layer, normalized layer, defuzzy layer, and total output layer. The five layers of the ANFIS and their respective activation stages are listed in subsection 3.2.1 - 3.2.5. Figure 2 shows how the logic is flexible. The ANFIS structure is shown in Figure 3 which is included.

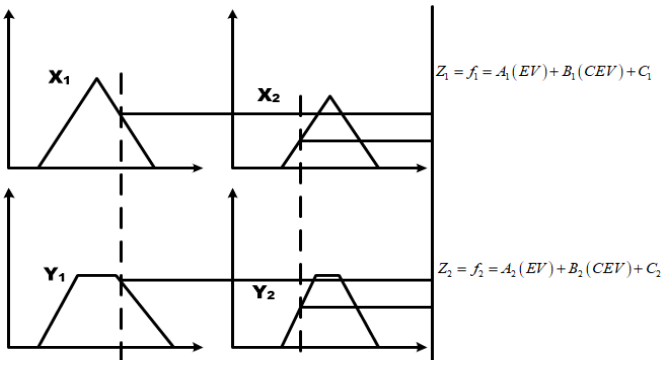

Figure 3. ANFIS model overviews

3.2.1. Layer1

This layer is referred to as the fuzzy layer or the fuzzification layer. Fuzzy data is created from the input data. The fuzzy linguistic labels used by the fuzzy theory to divide the membership functions are X1, X2, Y1, and Y2, where X1, X2, Y1, and Y2 are the nodes' errors (E) and rates of change in errors (CE). The following equations give the fuzzy layer's output.

$$F_{1,i} = \mu X_i(a) i = 1,2 \& F_{L1,j} = \mu Y_j(a) j = 1,2 \quad (16)$$

where F_{1j} and F_{2j} are the output of the fuzzy layer $\mu X_i(a)$ and $\mu Y_j(a)$ are the membership function of the fuzzy layer.

3.2.2. Layer2

The product layer, also known as the product of the input membership function, is the layer that executes the logical "and" operation. The output of this mode is the next node's input weight function, denoted by W1 and W2. The following equations can be used to represent the output of this layer:

$$Z_1 = F_{2,i} = \mu X_i(a).\mu Y_i(a) i = 1,2; Z_2 = F_{L2,j} = \mu X_j(a).\mu Y_j(a) j = 1,2; \quad (17)$$

where Z_1 and Z_2 are the outputs of the product layer.

3.2.3. Layer3

Layer normalized, each node in the third layer, which is set, represents the IF part of the fuzzy rule. This layer is used to perform the "AND" operation after normalizing the input weights. The accompanying equations help to represent the output of this layer, labeled N:

$$\overline{Z_1} = F_{L3,i} = \frac{Z_i}{Z_1+Z_2} i = 1,2; \overline{Z_2} = F_{L3,j} = \frac{Z_j}{Z_1+Z_2} j = 1,2; \quad (18)$$

where $\overline{Z_1}$ and $\overline{Z_2}$ are the outputs of the normalized layer.

3.2.4. Layer4

Defuzzification layer: sometimes known as the defuzzification layer, this layer is used to compute defuzzified values. The output connection function base on the predefined fuzzy rules is computed using this. The following equations give the defuzzification layer's output:

$$\overline{Z_1}f_i = F_{L3,i} = \frac{Z_i}{Z_1 + Z_2}(M_1(E) + N_1(CE) + C_1) i = 1,2;$$
$$\overline{Z_2}f_j = F_{L3,j} = \frac{Z_j}{Z_1+Z_2}(M_2(E) + N_2(CE) + C_2) j = 1,2; \quad (19)$$

where M_1; M_2; N_1; N_2; C_1 and C_2 are used to represent the linear parameters. The outputs of the defuzzification layer are $\overline{Z_1}f_i$ and $\overline{Z_2}f_j$respectively.

3.2.5. Layer5

Output layer overall, the fuzzy rule's then clause is represented by the output layer. It is possible to calculate the sum of the input signals, which is denoted by the symbol. The following equation gives the layer's overall output:

$$f = F_{L5,i} = \sum \overline{Z_1}f_i = \frac{\sum \overline{Z_1}f}{\sum Z_i} \quad (20)$$

where f is used to represent the total output.

4. SIMULATION RESULTS AND DISCUSSION

The overall power system of DSTATCOM with an uncontrolled rectifier is modeled with MATLAB/Simulink. The control schemes, which is used for the generation of tracking signal also modeled in the MATLAB/Simulink environment using the SimPower system block sets. To study the characteristics of DSTATCOM, the nonlinear current waveform is obtained with three phase diode bridge rectifiers. The waveform generated with the diode bridge rectifier consists of an R-L load is an almost lagging power factor. The simulation characteristics obtained with the IRPT scheme of DSTATCOM are depicted in Figure 4. The simulated characteristics obtained with the LMS algorithm of the DSTATCOM are shown in Figure 4. The source current total harmonic distortion (THD) without compensation is 18.77% and can be evident from the load current THD spectrum as depicted in Figure 5. The current contributed by the DSTATCOM is used to eliminate the harmonics and the source current tends to be sinusoidal. At this instant, its THD value is reduced to a value of 2.99% and can be evident from the load current THD spectrum as depicted in Figure 6. Which is within IEC 61000-1-1 compatibility limits. As the source current tends to be sinusoidal, and the source current in synchronous with the source voltage and power factor is almost unity. The DSTATCOM waveforms corresponding to the ANFIS controller are depicted in Figure 7. The source voltage, source current, load current, compensating current injected by DSTATCOM, and DC-link voltage are all represented by the spectrum of waveforms from top to bottom.

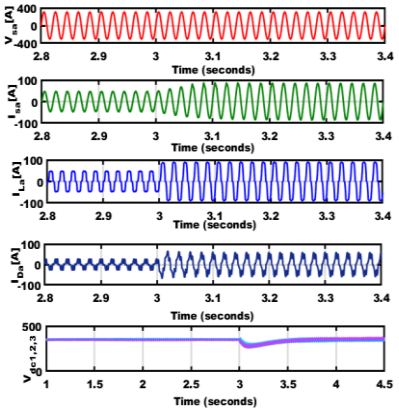

Figure 4. Performance of the DSTATCOM with sliding mode controller (SMC)-SRF

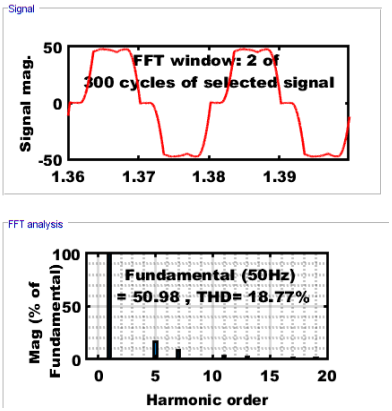

Figure 5. THD value without compensation

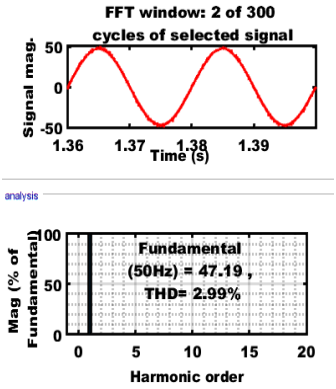

Figure 6. THD value with SMC-SRF algorithm

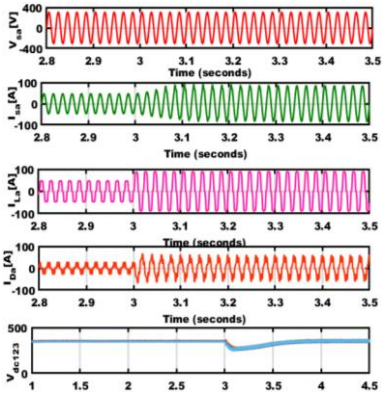

Figure 7. Performance of the DSTATCOM with ANFIS-SRF

The harmonics current is now being removed using the DSTATCOM current. Source current will therefore tend to be sinusoidal, in phase with source voltage, and the power factor will reach unity. The source current follows the source voltage because the power factor tends to be sinusoidal. The source's current THD, which is high and has a value of about 18.77% before compensating using DSTATCOM, is 18.77%. This value of THD is observed from the spectral waveform as evident in Figure 5 after compensation with DSTATCOM, the source current THD is reduced to 2.85% with the ANFIS controller as shown in Figure 8.

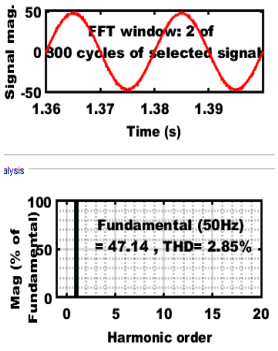

Figure 8. THD value with ANFIS-SRF algorithm

5. REAL-TIME VALIDATION

The experimental results of CHB-based DSTATCOM are exposed in Figure 9. The figure shows steady-state and transient current waveforms. The current waveforms characteristics of the CHB-based DSTATCOM with improved voltage balancing are shown in Figure 9(a). The steady-state current waveform of the CHB-based DSTATCOM with improved voltage balancing control scheme is improved than that of the conventional control scheme of CHB-based DSTATCOM. The transient current waveforms of the CHB-based DSTATCOM with an improved voltage balancing scheme are made known in Figure 9(b). The step change in load current waveform causes the equivalent changes in the source current and compensation current of the DSTATCOM and CHB-based DSTATCOM with improved voltage waveform restored the source current within two cycles than that of the conventional voltage balancing control scheme based on SMC controller. The steady-state dc link voltage of DSTATCOM with an improved voltage balancing control scheme integrated with the SMC controller is shown in Figure 9(c). The transient dc link voltage of CHB-based DSTATCOM with an improved voltage balancing scheme using the ANFIS control strategy is shown in Figure 9(d). The step change in load voltage causes the corresponding change in the dc link voltage of CHB-based DSTATCOM. The decrease in dc link voltage is used to meet the load demand and the dc link voltage with an improved voltage balancing scheme restore to the reference value. The transient performance of the improved voltage balancing scheme of DSTATCOM is better than that of the conventional voltage balancing strategy.

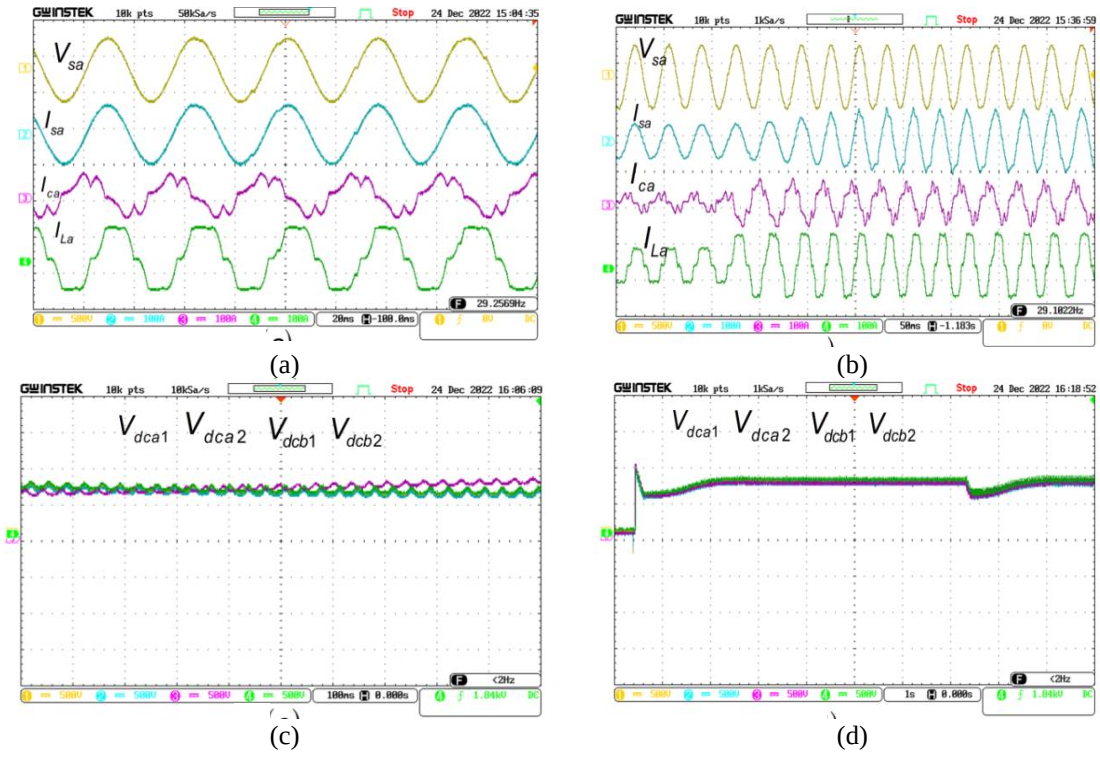

Figure 9. Improved voltage balancing scheme with ANFIS-controlled CHB DSTATCOM (a) steady-state current waveform, (b) the step change in load current waveform, (c) the steady-state dc link voltage, and (d) the step change in load voltage

6. CONCLUSION

ANFIS-based DC voltage regulator for multilevel inverters is suggested in this article and is simulated using the MATLAB platform. The proposed ANFIS generates voltage error for the suitable voltage variations using the improved knowledge rules base. The performance of the suggested approach was compared to the THD of the MLI output voltage with and without the SMC controller. The results of the simulation show that the proposed ANFIS controller works better than the SMC. Additionally, it can be seen that the suggested method has a lower THD under different load scenarios. The comparison result demonstrates that the suggested method is a well-improved technique to get rid of harmonics and is superior to other methods in this regard.

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