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The Optimal Design of Communication Module for Campus Smart Card

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Abstract

Campus Card is an important part in the digital campus life. However, due to the problems of current network design, in the course of card using, the signal channels are seized by a large number of communication tags, which leads to the phenomena of blocked communication process and unsmooth communication. In order to solve this problem, the communication module of card system has been optimized in this paper. The module consists of two parts, which are writing system and reading system. A multi-tasking multi-point mapping decomposition technique was introduced to the designation of communication module. Using the method based on the combination of Map and Reduce function to make the task decomposition which is from a sudden increase of network traffic characteristics and database, obtain a large number of sub-tasks, and accomplish the management of mutation network traffic. Experimental results show that in the task scheduling of optimized module, the solution time is short and response is fast. It can solve the communication blocked problems in the process of card using. Furthermore, it provides theoretical references for the improvement of communication system design of smart card, and promotes the construction of digital campus evolving.

Keywords: *smart card, hardware platform, software design. multi-point mapping*

1. Introduction

With the development of computer technology, the computer-based network and communication developed quickly. From the development of the campus network to a variety of applications spread, the digital campus construction is moving forward at an unprecedented rate. The essence of Digital Campus is to optimize the integration of fragmented information resources to achieve data sharing, thereby increasing the level of management within the campus and teaching. Among them, the campus card system construction is the basis for digitization projects. It plays an important role in the progress of intelligent university campus construction. Campus Card is a unified set of the entire school community financial services, internal micro-payment transactions, authentication, and business management in one of the school-wide unified campus card system. It takes advantage of the powerful features card and offline transactions of smart IC. And under the environment of campus network or campus card private network, the one card can be available throughout the campus. Campus card system has become an important means for the variety of institutions and universities to enhance the management level and improve campus services.

However, as the number of campus card user and function increases, the number of network nodes also increased, the network structure is becoming more complex, and each management systems run on the networks platform have different performance requirements. Therefore, the contradiction of significant increase in network size and existing network service capabilities and environment has become increasingly prominent. This is mainly due to the disadvantage design of communication module in campus card. Since nodes with limited resources, there are a large number tags to seize the communication channel, which leading to dynamic scheduling management tasks are affected, causing blocked communication process and unsmooth communication, limiting the scope of application of the card.

Currently, researchers have used various methods to deal with the resource scheduling of virtual network system. General speaking, it can be divided into two kinds algorithms which are static algorithm and dynamic algorithm. In static algorithm, the virtual network map does not change with time, resulting in low utilization of physical resources. While in the dynamic

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algorithm, it can reallocate the mapped resources in the running process of virtual network to optimize the use of the underlying physical network resources to ensure network connectivity [1]. Literature proposed to re-configure the virtual network mapping periodically and selectively to optimize the physical network overload parts. However, the number of virtual network resource reallocation will affect the stability of the network and computational overhead [2]; literature also designed a redistribution of resources mapping algorithm. The algorithm remaps the lower priority request of virtual network on bottleneck nodes and bottleneck link to improve the acceptance ratio of virtual network and reduce the pressure on the use of resources However, in this algorithm, only in the event of a virtual network requests cannot be mapped, it makes remapping adjustment of virtual network. In the migration of a virtual node, it is also need to migrate virtual link connected to the node. Thus, the overall pays for calculation of the algorithm is still large [3]. Literature presented a dynamic adaptive virtual network mapping algorithm for a customized Internet. The algorithm is executed periodical reallocation in multiple virtual gateways to share the bandwidth between the virtual links of the same physical link. However, the algorithm does not consider the allocation of virtual network nodes, and in this algorithm, physical network link need to know the performance objective function of all virtual networks in advance [4, 5]. Literature presents a distributed autonomy resource management mechanisms based on self-organization of technical, in the mechanism, the physical node can identify of the overload traffic a physical link, and migrate through the virtual nodes to minimize such flow experienced by the number of physical links, to maintain load balancing and bandwidth savings of resources used. But this mechanism does not explain the virtual host node selection method of objectives to be migrated [6]. VMCTune is a dynamic resource allocation based on the virtual cluster load balancing mechanism, which can be monitored in real-time virtual machines and physical machines resource utilization, and then by calling the resource re-allocation algorithm, on the same physical machine, to obtain partial load balancing of virtual machines; simultaneously, on multiple physical machines, virtual machine live migration to obtain the global load-balancing virtual cluster. This mechanism can effectively allocate resources to virtual machines, but also improve the utilization of physical resources. But this algorithm to select the target host, did not consider the impact of migration on link load [7, 8].

To solve these problems, we propose a decomposition method based on the multi-tasking and multi-point mapping [9]. In this method, the introduction of MapReduce function is applied in the task decomposition of mutations traffic in campus card network to complete the resource scheduling of virtual network nodes and the simulation experiments so as to optimize the communication module design of current campus network card and thereby solve the blocked problems in the network communications. A new and convenient modern life is brought to students and teachers, so as to enhance working efficiency, and improve the modern management level of school [10, 13].

2. Overall Designs of Campus Smart Card

2.1. Design Philosophy of the System

Digital campus card system needs to reflect the dominant idea of integrated design sufficiently, all the data sources of informationized campus are from the shared database, when the various departments are processing data maintenance in future, only the data of shared database need to be maintained, all the information sources of each application subsystem are from the shared database, when constructing the subsystems, the integration and unification of shared data center, smart card systems and portal information systems should be considered, in order to achieve consistency of information from top to bottom and unify identity authentication. System architecture should consider the principle of independence, which means it is not restricted by specific types adopted, like databases, operating systems, programming languages, card type, communication networks, and can be adapted to various operational environments and make full use of existing resources.

2.2. Requirements of System Design

Smart card technology for universities is a close integration of computer and high-tech means based on intelligent recognition principle. The inherent information characteristics and attributive character of the card are used to process related operation. According to the

characteristics of embedded technology and two-dimensional code reader technology and its application in the field of testing, the study determined the overall structure of the smart card reader system based on embedded system. The entire system is divided into three parts: the reader, embedded processing platform and LCD display. The entire process of the universities card reader systems is accomplished by embedded system. The main work process includes information read & written, information compared, located and operated.

By constructing smart card projects to form network operating environment which is suitable to school campus card system, build a basic card system software and hardware architecture. Card data center and card management center basis platform are constructed, campus card service center, bank transfer system, settlement systems and self-service systems are built; campus card personal identification and electronic purse payment functions are used to achieve campus dining charges, supermarket or small business district shopping charges, Library fees, clinic fees and other unified consumption and settlement; identity authentication is realized, like sign-in for meetings, student attendance, physical exercise; integration of computer room management, library management, and other third-party systems are completed, in order to achieve a comprehensive unified campus card.

3. Hardware Design of System

Background system construction of the smart card is divided into hardware and software construction. The system selects a Samsung ARM9 processor and framework of Linux systems, and the output module and communication module are attached, the card information is collected, processed and run identifying information, information extraction, and subsequent operations independently. The proposed system selects systems based on ARM9 & LINUX and dual USB interface reader which contains the function of tag identification and is started at the same time to ensure the synchronous operation of the system. A SDRAM memory architecture is adopted, software design includes three parts: information reading, information comparison, and information operation. Where the sample is selected by the CUP automatically, related operations are processed according to the different types of information, part of the card tags with same size are selected as the training samples and samples to be identified, the two-dimensional information in the card is read by the card reader, and recognized by querying comparison information in the database, then the final identification result is output. The device is portable, low power consumption and can be applied to other areas by means of software design, such as card loss reporting, card dynamic modification.

Hardware circuit is the foundation of the embedded card read system, and the carrier to achieve its various functions. S3C2440 is a high-quality processor belongs to ARM9 series manufactured by Samsung, which uses a five-stage pipeline structure, has high efficiency of instruction running. It supports multiple operating systems including LINUX. The information is stored using SDRAM and FLASH memory. The FDS network controllers embed the TCP / IP protocol into the controller for the first time, and realize Internet surfing through the TCP / IP. It is convenient to access the Internet network and easy to achieve network management. The controller uses a high-performance real-time operating system, and supports multi-task operation while ensure the real-time feature of the task. Display part uses Sharp's 3.5-inch TFT LCD, communication interface uses the RS-232 and USB to realize human-computer interaction.

3.1. S3C2440 Chip

S3C2440 processor is developed by the Samsung with ARM9 as its core. In order to improve the compatibility with traditional von Neumann architecture, ARM920T uses Harvard Cache structure. With great expansibility, the processor can meet the requirement of future system upgrading. ARM9 microprocessor has the following characteristics:

(1) Five pipeline: fetch, decode, execute, storage and write operation. Instruction execution efficiency is high
(2) Provides a Harvard architecture
(3) Supports dual instruction set
(4) Supports 32-bit high-speed AMBA bus interface
(5) Support Linux and other embedded systems
(6) MPU supports real-time operating system;

3.2. The Card Reader Selection

RFID (radio frequency identification) technique is employed in reading and writing system of campus card. The technology is an automatic identification technique, wireless non-contact method is used to communicate in two-way, so as to enable reading in batch and remote, and identify fast moving objects, each object has a unique identifier to meet the needs of increasing flow of information and the increasing speed of information processing, thereby increasing efficiency and reducing costs. RFID technology adopts a large scale integrated circuit calculation, electronic identification, computer communication technology, to achieve non-contact carrier identification and data exchange by the reader and the RFID tag mounted on a carrier. RFID technology has the advantages which bar code does not have, like waterproof, antimagnetic, remote read distance, large storage capacity of labeling data, etc.

Typical RFID reader system consists of three parts: the electronic tags, readers and computer communications center. The system block diagram is shown in Figure 1.

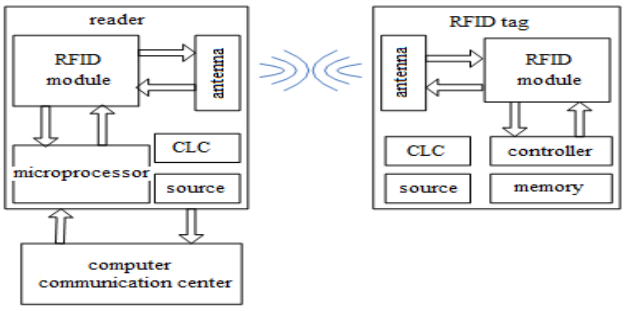

Figure 1. RFID System Block Diagram

(1) Electronic tag

Electronic tag is known as radio-frequency tag or transponder, and it is the data information carrier of the RFID system, which is usually installed on the identified object used to store the object information. According to different application environments, the electronic tag has different shape, size and operating frequency, and space coupling with RF signal is achieved to complete data communication and energy transfer through coupling elements and reader. Due to the method of power supply, electronic tag can be divided into active tag and passive tag.

(2) Reader

The reader, also known as a read head, is responsible to communicate with electronic tag, read or write electronic tag information, and send the data to the computer communication network. In the process of work, the establishment of the communication, anti-collision and authentication are completed by the reader.

(3) Computer communication center

The computer communication center is mainly responsible to send commands to the reader, collect data received by reader, and then process data in accordance with different requirements. Usually it achieves data transfer with the reader through RS-232, RJ-45, USB, Ethernet and Wi-Fi.

3.3. LCD Display

S3C2440 contains internal built-in LCD controller which supports 4, 8 and 16-bit color LCD, such as STN and TFT. Taking the effectiveness and cost into account, the proposed system selects Sharp 3.5-inch 320X240 TFTLCD. The expansion is convenient because of the LCD controller and driver of S3C2440. (1) VD0-15: 16-bit data line; (2) VCLK: LCD clock signal, which is used to send the data of each point into the shift register; (3) VLine: line signal used to indicate completion of the data-in-line transmission from the shift bit registers to the display driver chip, and makes the line pointer. In the mode of TFT 16, that is, the horizontal synchronization signal; (4) VFrame: frame signal is used to indicate the start of personnel

information, while the row pointer is put in the first line of the display. In 16-bit mode of TFT, it is a vertical synchronizing signal; (5) LCD_PWREN: In 16-bit mode of TFT, the enable signal is output. A data signal for indicating the synchronization of the clock signal, the latch to the pin.

3.4. Communication Interface and Storage Module

The communication interfaces of hardware system include RS-232 serial interface and USB interface. The CLIENT TO HOST serial data transmission can be achieved easily through the RS-232 serial port which is used by most embedded instruments and computer data transmission. In order to connect the RS-232 serial port to TIL level device, MAX232 integrated circuit chip is employed to switch S3C2410 serial level. The character median of UART transceiver is configurable and can be 5 to 8. In transition, 32-byte data written from data bus is transmitted to FIFO, and then is fed to the shift register and converted to serial data output through TXD pin. Data is received from RXD pin serial. It first enter the receive shift register, and then fed into the FIFO with half-word depth. The receiving and transiting of FIFO have maskable interruption which could be issued when data of the FIFO reaches a pre-set amount. At the same time, the receiving and transiting of FIFO can request the DMA. UART transmit baud rate depends on the input divider which have configurable clock and software. The UART also have unit circuit for baud rate self-detection which could be used to configure the stop bit and parity check. Linux operating system supports most common hardware devices and provides the appropriate drivers, so all of OHCI compliant USB device interface can be driven. The system supports the USB interface. Storage equipment selects SDRAM (synchronous DRAM) which can be synchronized with the external clock of the CPU. The SDRAM and system CPU use the same clock, so if the CPU external clock is 100MHZ the frequency sent to memory is also 100MHZ. Through this way memory efficiency can be improved. The system hardware platform uses K4S561632-TC75 chip manufactured by SAMSUNG, with monolithic capacity 32M * 16bit and SDRAM modules. CUP comes with FLASH electrically erasable, and information is not lost when power-down. The hardware design of the system is shown in Figure 2.

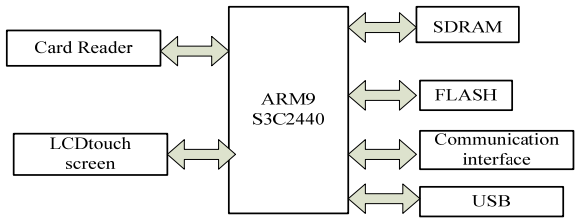

Figure 2. Hardware Design of the Communication System

4. Software Design of the System

4.1. Initialization Design

The main program accomplishes initialization work according to the background command.

If the RF module receives sending commands, it will call the initialization subroutine. When CONFIG register PRIM_RX bit is 0, the transmit mode is begin, users should set the address of the sending & receiving and the minimum address width of the lowest two bits of SETUP_AW register ("01" means 3 bytes, "10" represents 4 bytes, "11" is 5 bytes, "00" is an invalid state). If the reader communication has tag of nRF24L01, the last bit of EE_AA register will be set 1 to open automatic ACK function. If reader communicate with the other models' compatible tags (nRF2401, nRF240, nRF24E1, nRF24E2), this bit must be set to "0" to turn off the automatic ACK. Part of the code is shown as follows:

```
void TX_Mode()
{
   IO_Clear_CE();
```

```
  SPI_Write_Buf(WRITE_REG + RX_ADDR_P0, TX_ADDRESS, TX_ADR_WIDTH);   // Set
the sending and receiving addresses
    SPI_RW_Reg(WRITE_REG + EN_AA, 0x01); // Start the automatic ACK function
    SPI_RW_Reg(WRITE_REG + SETUP_AW,0x02); // Set the width of the address
    SPI_RW_Reg(WRITE_REG + RF_SETUP, 0x0F); // Set the data rate and output power
    SPI_RW_Reg(WRITE_REG + CONFIG, 0x0A); // Set the sending mode
    IO_Set_CE(); // Set CE at high level, enable sending device
  }
```

If the RF module receives receiving commands, it will call the receiver initialization routine. The CONFIG register PRIM_RX bit is set to 0, and enter receive mode. The initialization of the other registers and send program are the same. Part of the code is as follows:

```
  void RX_Mode()
  {
    IO_Clear_CE();
    SPI_Write_Buf(WRITE_REG + RX_ADDR_P0, TX_ADDRESS, TX_ADR_WIDTH); //Set
the sending and receiving addresses
  SPI_RW_Reg(WRITE_REG + EN_AA, 0x01); // the automatic ACK function
    SPI_RW_Reg(WRITE_REG + SETUP_AW,0x02); // Set the width of the address
    SPI_RW_Reg(WRITE_REG + RF_SETUP, 0x0F); // Set the data rate and output power
    SPI_RW_Reg(WRITE_REG + CONFIG, 0x0B); // Set the receiving mode
    IO_Set_CE(); // Set CE at high level, enable receiving device
  }
```

4.2. Reading Program Design

The collected tag information is sent from nRF24L01 to microcontroller through SPI port, and then to PC, finally processed by the background programs.

MSP430F149 writes the data to be sent and the receiving address into the TX_FIFO register of nRF24L01, then sent CE to high, at this time, nRF24L01 begin to send data. When completed, the transmitting device waits for ACK from the reception side. If the ACK is not received within a certain time, the data will be automatically retransmitted. Retransmission interval and the number of retransmission are determined by the high four ADR and the low four ARC of SETUP_RETR register. The number of retransmission is up to 15. If ACK successfully received or the retransmission is timeout, the device enters standby mode to wait for the next data transmission.

In the transmission, 7 to 4 bits of OBSERVE_TXP register are defined as packet loss counter PLOS_CNT used to record the number of data packets lost in the transmitted. 3 to 0 bits are defined as data retransmission counter ARC_CNT reset when new data packet is available. The success rate of data received can be obtained through PLOS_CNT record value which can be used to assess the reliability of the equipment.

4.3. Multi-task Multi-point Mapping Decomposition Algorithm

Virtual network mapping is to request for distribution of the corresponding underlying physical network resources to the virtual network which has different virtual nodes and virtual link resource constraints and topology requirements. From the perspective of infrastructure providers, mapping should as much as possible to meet the needs of the virtual network in the case of spending minimum resource cost. Virtual Network Mapping is just a sub-function of Network virtualization, how to use the shortest possible time to complete the resource mapping is a necessary condition to ensure smooth deployment of services and applications. Virtual Network Mapping Problem is also NP-hard even in the condition of static demand In the early studies, researchers used various of method in varying degrees, to limit the problem, such as ignoring the virtual node or virtual link resource requirements, or suppose all of the virtual network requests are known, or only concerned with a particular virtual network topology request, or the assumptions underlying physical network has sufficient resources, without regard to the requested virtual network resources limit, or to ignore the position of the virtual node requirements Therefore, researchers have proposed a number of heuristics to study such

problems. These heuristic strategies can be divided into two categories: the demand based on static mapping problem and needs based on dynamic mapping problem.

The smart cards' label management method for information mutation decomposition based on multi-point multi-task decomposition technique, complete decomposition on Hadoop platform which is composed mainly by the distributed file system and MapReduce task parallel computing model. The platform parallel calculates card task behavior data, without considering single node task scheduling and data storage problems.

(1) Card label information extraction

In the task decomposition process, first, the label is collected and transmitted to the network, to be restored to the connection records of TCP / IP layer, and its features are extracted. The details of which are described below

1) The network communication module is set to open, so that it can conduct surveillance on tag read and connect card monitoring system and communication network.
2) Pre-process of the operating structure of the tag data, and capture data according to the data packets converted from tag operation data.
3) Extract data packet of network operations from the module and convert its format, then store in the database.
4) According to the above procedure to iterative process the card label until it reaches the stop condition to end the operation.
5) The card communication module is configured to normal mode, receiving data in buffer to obtain network operating characteristics and provide accurate data foundation for management of decomposition of network traffic mutation.

(2) Mutations assignments decomposition Management

Card tag data collected are initialized to constitute a data collection that contains the central node and serial number. Among them, the central node records the name stored location of the file system and client access traces, and serial number is used to store manipulating data in the network and the user's request for processing. According to the serial number of the network operational data, we can create, delete, and copy the data. The data processing for network feature set above has a strong fault tolerance and throughput.

The combination of Map function and the Reduce function transfer data set composed by label feature to the distributed network file system, thereby reducing network file storage time. The main steps of data processing method are that: first divide the larger tasks into a large number of sub-tasks; then carry out independent data operation to sub-tasks and collect the results; finally get the initial process results.

During the process of tag data with Map function, the tasks should be decomposed. The sizes of obtained sub-tasks are similar which can be described as $split$. Each independent sub-task can be divided into corresponding key value pair $(key1, value1)$ which will be transmitted to Map function. After the process, we can get the new key value pair $(key2, value2)$ which is also the input of Reduce function. After processing the input data, the corresponding key-value pairs $(key3, value3)$ can be obtained, and then according to the actual needs of users during operation, the pairs are outputted to the target location in HDFS database.

The steps of method combining Map function with the Reduce function to pass data set constituted by network characteristic to the distributed network file system are shown as follows:

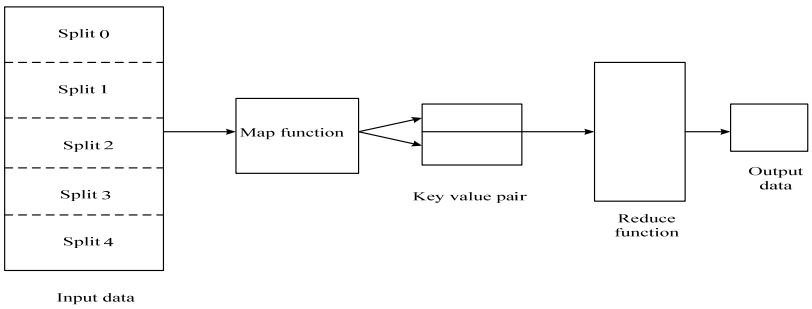

Figure 3. Initialization of Data Processing

According to the method described above, the multi-tasking multi-point mapping decomposition technique can be used in mass label card matching tasks and perform calculations. Data packets corresponding to the network operating characteristics are extracted from HDFS cache, and the similarity matching process is carried out on the remaining elements in the database. The results obtained are reordered and re-divided to obtain the similarity sorting of the keys. The first P key value pairs are extracted from the above data then written to the HDFS.

5. Test Analyses

The purpose of testing is to verify the feasibility of the system. This paper takes a vocational college for example to verify the proposed strategy of allocation of acquired tasks and node communication resource scheduling.

Management module selects task with the highest priority from the scheduling task table Task_list and publishes task to able CA1, CA2, and CA3 according to the information in the knowledge base by multicasting way.

Once the CA1, CA2, and CA3 receiving task information of a card issued, the information will be stored in Task_list as a record. Reference database tasks related data, pre-scheduling results of processing unit CA1 is shown in Figure 6

Through a scheduling, three unit Agent return bidding information to the Management Agent (including bid value, the load rate and completion time), the process is shown in Figure 1. Finally, Management Agent selects and notifies unit CA1to complete Order1. When get the reply from CA1, CA1 will be formally assigned to complete the task. The simulation results are shown in Figure 7.

Management Agent select one of two losing Agent units as a backup process, and the relevant information will be saved, in order to reduce the processing time of the accident and reduce the accident damage. Meanwhile, the management Agent also notices unit CA2 and CA3 to end the mission negotiation assignment.

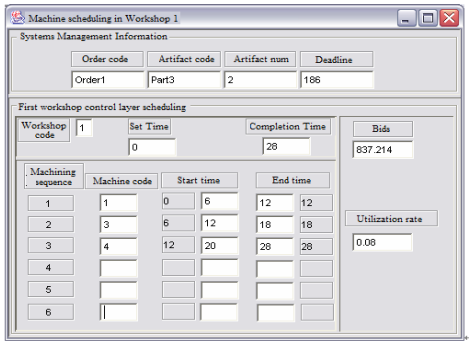

Figure 4. Unit Cell Agent1 Scheduling Process

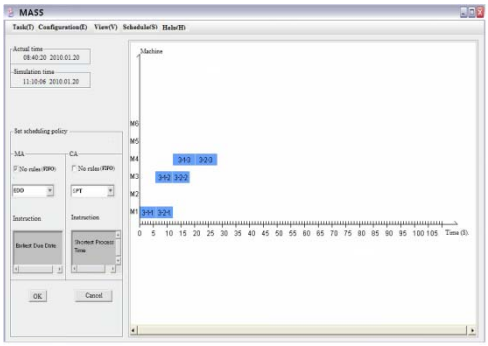

Figure 5. Card Task Scheduling Simulation Results

Experimental results show that the smart card system is able to complete the expected scheduled tasks. Although the results are not the best scheduling, the solution and communication time of MASS scheduling problem are contained in the whole processing course of the workpieces, the solution time is short and has fast response, so it has certain advantages when applied to dynamic scheduling.

6. Conclusion

Campus card system is a large-scale information integration system which is the system of software-based and hardware and terminal equipment supplemented. It is an important part of digital campus. At this stage, sine the number of campus card user increase, tasks is more and more diversity, and in the specific period the usage peak emerges. Therefore,

it can easily lead to large-scale signal tags to seize the communication channel and impact the campus life and the transaction management. It indicates that traditional network architectures cannot fully adapt to the new era of the development needs of the campus card. It is an urgent need to establish a flexible, agile network service environment. So, it is very necessary to use a reasonable calculation method to optimize the resource scheduling of virtual network card.

This paper introduced a multi-tasking and multi-point mapping decomposition technique. It mainly uses the MapReduce computing model to quickly decompose the information of mutations tags in the card network. MapReduce is a programming model proposed by Google for distributed parallel computing of large-scale data. MapReduce model is inspired by map and reduce functions commonly used in functional programming. A Map／Reduce job usually splits the input data set into independent chunks which are processed by the map tasks in a completely parallel manner. The reduce tasks merge all intermediate values generated by the map tasks. Users only devote themselves to how to specify the map functions and reduce functions. The details of partitioning the input data, scheduling the program's execution across a set of machines, handling machine failures, and managing the required inter-machine communication are taken care of by the runtime system of MapReduce. It reduces the overall difficulty of programming in a large extent.

MapReduce function has three distinct advantages: first, compared to the other parallel programming models, MapReduce has higher programming efficiency, which has transparent details when calculating the parallel, load balancing and fault tolerance of tasks; second, it can fully and efficiently utilize the resources of each machine in the cluster, and is suitable for processing computing tasks of large-scale data in the cluster, it makes the gigabit-level data can be operated in an ordinary PC, which could only be operated in large commercial hardware formerly; third, good fault handling mechanism allows MapReduee with high reliability. These advantages make it become the mainstream programming model of a variety of computing platforms increasingly, when facing large-scale data computing task, MapReduce programming model will play a more important role.

Simulation results show that this decomposition technique used in this mapping can be an effective solution to analyze large data sets and other problems. And the speed of solution is quick and the response time is short. It is capable of rational management and configuration of network resources. It can also reduce network traffic disruption, provide a reference for the resource scheduling of virtual network and offer new ideas to optimization design of card communication module. Thus, there is certain practical application significance. Meanwhile, the system can effectively promote the process of school education informatization and digital campus construction, improve management level of school, enhance service quality of back office, achieve downsizing to improve efficiency, and become an integral part of staff and students' working, studying and living.

However, due to the research of resource management and mapping method of campus card network is still in early stage, and the constraints of research level and energy limited, there must be also many issues that need further study and improvement in this paper. Future research will be available from the following two aspects:

(1) This paper presents a multi-tasking and multi-point mapping of virtual resource scheduling method, but the details of the design is not sufficient, such as for troubleshooting, mobility management, dynamic resource scheduling algorithms. In many usage scenarios, the basic principle of the resource scheduling is the same, but the speed and stability performance are very different, So for troubleshooting, mobility management application scenarios, the development of appropriate resource scheduling algorithm has great research value, but also the one of next step in this research work.

(2) The effective distinguish between physical resources is the important factor for improvement of virtual network mapping algorithm. This paper studies the link node-based pressure and the pressure of the virtual network optimization mapping algorithm, and making the virtual network mapping process can be based on the characteristics of the virtual network to allocate more than ten pairs of physical resources. Therefore, to improve the performance of virtual network mapping algorithm is the next step of this work.

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