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Low Leakage Circuits Design with Optimized Gate-length Biasing

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Abstract

With the technology process scaling, leakage power dissipation is becoming a growing number of percentage in total power dissipation. This study presents a new method in the gate-length biasing technique to achieve a cost-effective gate-length with a most benefit between leakage reduction and delay increasing. With the optimized gate-length, typical combinational and sequential circuits are realized and simulated using HSPICE with the BSIM4.6.4 predictive models at a 45nm COMS process. The results show that leakage currents of typical combinational circuits reduce more and delay increase less. Moreover, leakage currents of mirror adder and transmission gate adder decrease 13.9% and 8.90%, respectively; and leakage power of 4-bit binary counters using C^2MOS D Flip-Flop and Transmission-Gate D Flip-Flop reduce 38.36% and 20.05%, with the frequency of 5M, respectively. Therefore, the optimized gate-length biasing technique is an attractive approach in low power circuits design.

Keywords: *low leakage, gate-length biasing, cost-effective gate-length, HSPICE simulation*

1. Introduction

With the ever increasing demand and popularity of portable electronics, designers are striving for small silicon area, higher speed, high reliability and low power dissipation [1]. The power dissipation of circuits affects the battery life of portable electronics. There are three main power dissipations in circuits: dynamic power dissipation, short-circuit power dissipation and leakage power dissipation [2].

Recently, CMOS technology develops into micro-nanometer regime, leakage power dissipation accounts for an increasingly larger portion of total power dissipation in CMOS circuits. It is reported that the portion of leakage power has increased from 18% at 130 nm to 54% at the 65 nm node [3].

Leakage reduction methods include standby techniques and runtime techniques. Standby leakage reduction techniques decrease the leakage when the circuits are not in operation, while runtime techniques decrease the leakage when the circuits are in active mode. Several standby leakage reduction techniques have being proposed, such as dual threshold CMOS, variable threshold CMOS, input vector control, and stacking transistor technique, power gating technique, etc [4]. The runtime leakage reduction techniques include multi-V_{th} manufacturing process and gate-length biasing [3, 5, 6].

These methods have advantages and disadvantages, such as, multi-V_{th} method reduces the leakage power effectively, but additional steps and masks raise its process cost. Gate-length biasing technique reduces the leakage without extra mask and extra process, and it is reported that small biases in gate-length of transistors can afford significant leakage savings with small performance impact [3]. A method of gate-length biasing was proposed in [3], and reduced leakage by 24%-38% for most commonly used cells, while incurring delay penalties of fewer than 10%.

In this work, we propose a new method to optimize the gate-length. We get a relatively cost-effective gate-length with a most benefit between leakage reduction and delay increasing, that is maximizing the leakage reduction with minimal delay penalty. Then, several combinational logic circuits and sequential circuits are used to verify the cost-effective gate-length. Moreover, as the battery life of portable electronics is mainly determined by average power, we take the averaging to measure the results in this paper.

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This paper is organized as follows. In Section 2, leakage current of MOS devices is described, and the gate-length biasing technique is reviewed. In Section 3, we propose a cost-effective gate-length optimization method. Basic combinational and sequential circuits with the optimized gate-length are implemented and simulated in Section 4 and 5, respectively. The conclusion is dedicated in Section 6.

2. Review of Gate-length Biasing Technique

2.1. The Leakage of MOS Devices

In nanometer regime, a significant portion of total power dissipation in high performance digital circuits is due to leakage currents [4, 7, 8].

The leakage current in MOS devices is mainly due to (1) sub-threshold conduction, (2) gate direct tunneling current, (3) junction tunneling leakage, (4) gate induced drain leakage (GIDL), (5) hot carrier injection current, (6) punch-through current, etc [7].

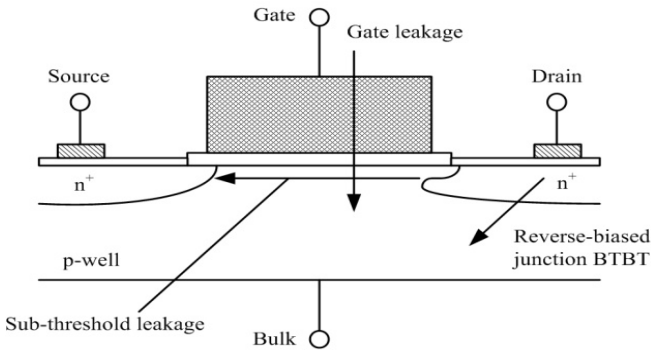

Figure 1. Major Leakage of MOS Device

Among them, the major leakage currents are: sub-threshold leakage current, gate leakage current and reverse-bias junction band-to-band tunneling leakage current as shown in Figure 1 [9]. With the technology scaling, sub-threshold leakage current has becoming the main source of leakage power dissipation.

2.2. Gate-length Biasing Technique

There are many leakage power reduction techniques, such as transistor stacking technique, dual-threshold technique, etc. It is found that, as the gate-length increases, the leakage power dissipation will decline exponentially and the delay only increase linearly [3, 10]. The fact provides a possibility for the gate-length biasing technique: an appropriate increase of gate-length can significantly reduce leakage power dissipation while performance of the circuit will not lose too much. Moreover, the technique doesn't increase the extra process cost because it needn't extra mask and extra process.

In nanometer CMOS device, as gate-length becomes shorter, V_{th} shows a greater dependence on gate-length [11], due to the short-channel effect (SCE) and drain induced barrier lowering (DIBL). V_{th} change due to SCE and DIBL is modeled (1).

$$\Delta V_{th}(SCE, DIBL) = -\theta_{th}(L_{eff}) \cdot [2(V_{bi} - \Phi_s) + V_{ds}] \quad (1)$$

Where $V_{bi,}$ is known as the built-in voltage of the source/drain junctions, V_{ds} is the source/drain voltage, Φs is the surface potential. The short channel effect coefficient θ_{th} (L_{eff}) in (1) has a strong dependence on the channel length given by:

$$\theta(L_{eff}) = \frac{0.5}{\cosh(L_{eff}/l_t) - 1} \quad (2)$$

l_t is the characteristic length of devices.

And the impact of threshold voltage in sub-threshold leakage [12] is expressed as (3). We can see that decrease of threshold voltage will result in sub-threshold leakage raise exponentially.

$$I_{on-sub} = \frac{W}{L_{eff}} \times \mu_{eff} \times C_{ox} \times (m-1) \times v_T^2 \times \exp(\frac{V_{gs} - V_{th}}{m \times v_T}) \times [1 - \exp(-\frac{V_{ds}}{v_T})] \quad (3)$$

W/L_{eff} is the width-to-length ratio of the transistor, $\mu_{eff}C_{ox}$ is the process trans-conductance parameter, $v_T = kT/q$ is the equivalent temperature voltage, m is the threshold rate coefficient, V_{gs} is the gate/source voltage, and V_{th} presents the threshold voltage of MOS device.

According to (1), (2) and (3), with gate-length increasing, the threshold voltage increases, so that the leakage current decreases exponentially. Therefore, it is possible to slightly increase the gate-length to take advantage of the exponential leakage reduction.

Figure 2 shows the variation of leakage with gate-length (L_{Gate}) at a 45nm CMOS process. The nominal length is 50nm, and the width of PMOS and NMOS transistors is 1000nm. The supply voltage of the transistors is 1.0V.

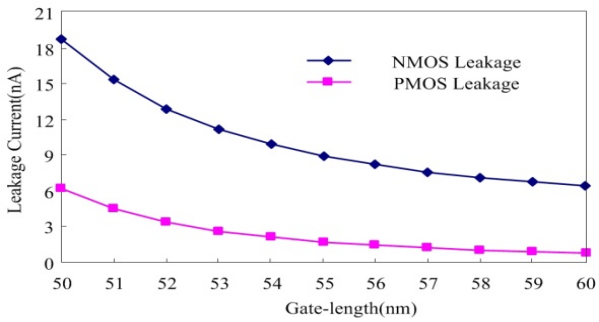

Figure 2. Leakage Variation with Gate-length

It can be noted that leakage decreases exponentially with slightly increase of gate-length. The leakage current of NMOS reduces by 52% and 66% at L_{Gate}=55nm and L_{Gate}=60nm compared with that of nominal length NMOS, respectively. The leakage current of PMOS reduces by 72% and 87%, respectively. In addition, the increase in gate-length decreases the leakage effectively; and the longer gate-length, the slower in leakage decrease.

3. The Gate-length Optimization for Efficiency Leakage Reduction

In this section, we propose a cost-effective gate-length optimization method based on HSPICE simulation by using a 12-stages inverter ring oscillator at a 45nm CMOS process. The inverter ring oscillator is presented in Figure 3. The ratio of PMOS over NMOS in the inverters is 40λ/20λ, where λ =25nm at 45nm process. The variation of delay and leakage with gate-length are shown in Figure 4 and Figure 5.

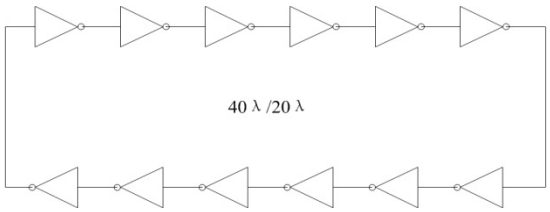

Figure 3. 12-stages Inverter Ring Oscillator

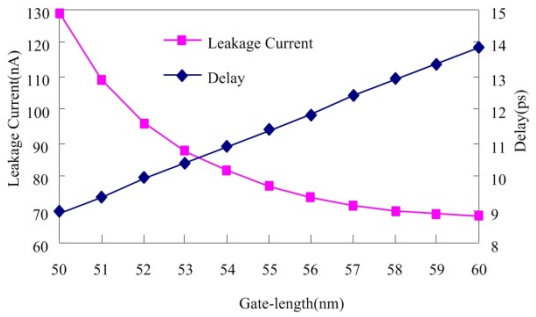

Figure 4. Variations of Leakage Current and Delay

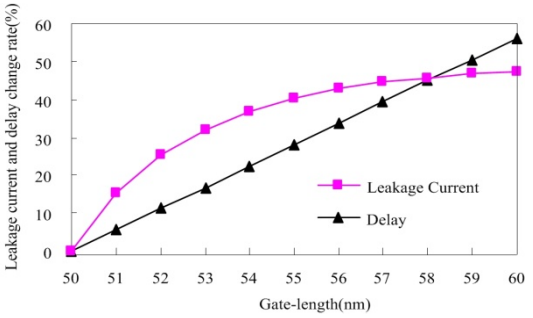

Figure 5. Variation Rate of Leakage Current and Delay

Figure 4 shows that as the gate-length increases, the leakage current declines exponentially, and the delay only increases linearly. Therefore, we increase the gate-length to get the maximum benefit between leakage and delay.

Here dynamic programming algorithm is utilized to determine the value of L_{Gate} for transistors. The benefit $f_c(L_{\text{Gate}})$ is defined as follows:

$$f_c(L_{\text{Gate}}) = \left|\Delta I_l / I_{l0}\right| - \Delta T_d / T_{d0} \quad (4)$$

Where I_{l0} and T_{d0} are the leakage current and delay of nominal L_{Gate} ring oscillator, respectively.

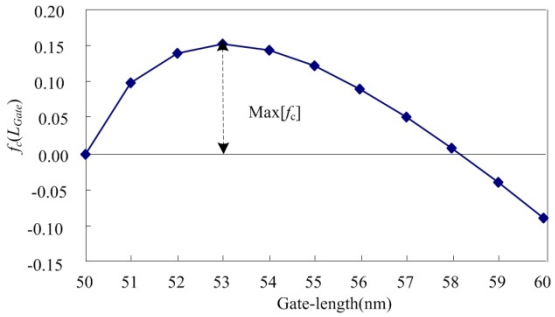

Figure 6. Benefit with Gate-length Variation

The result indicates that the maximum benefit is the max $f_c(L_{\text{Gate}})$, and the cost-effective gate-length is 53nm. It provides one of the best tradeoffs between leakage power dissipation and performance in low power applications.

4. The Combinational Circuits Design with the Optimized Gate-length

In this section, the basic combinational circuits with gate-length biasing technique are presented. All the circuits are simulated with HSIPCE at 45nm process. The nominal gate-length is 50nm, and the optimized gate-length is 53nm. The supply voltage of the circuits is 1.0V.

4.1. The Basic Gates with Gate-length Biasing Technique

The basic gates such as inverter, NAND, NOR and XOR are important elements in digital circuits. Here we test the basic logic gates with gate-length biasing. The width of NMOS and PMOS in NAND, NOR and XOR is shown in Figure 7, where λ =25nm at 45nm process. The leakage and delay of 2NAND, 2NOR, and 2XOR are shown in Table 1 and Table 2.

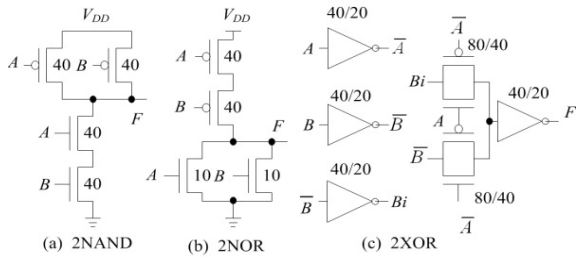

Figure 7. Basic Gates

Table 1. Leakage Current of Basic Gate Circuits

Input	Leakage current(nA) 2NAND		2NOR		2XOR	
	L=50nm	L=53nm	L=50nm	L=53nm	L=50nm	L=53nm
00	12.3	12	16.4	12.8	76.5	61.9
01	25.9	18.5	6.21	2.66	86.8	73.2
10	16.7	13.1	2.98	1.5	76.3	61.7
11	12.3	5.19	0.30	0.22	66.1	51.5
Average	16.8	12.2	6.47	4.3	76.43	62.08
Δ/%		-27.4		-33.6		-18.8

Table 2. Delay Characteristics of Basic Gate Circuits

	2NAND		2NOR		2XOR	
	L=50nm	L=53nm	L=50nm	L=53nm	L=50nm	L=53nm
T_d(ps)	13.2	14.7	15.2	17.15	32.8	34.3
ΔT_d%		11.36		12.83		4.57

The results show that the basic gates with gate-length biasing have lower leakage. As is shown that the leakage currents of basic gates: 2NAND, 2NOR, and 2XOR decrease 27.4%, 33.6% and 18.8%, respectively. However, as the gate-length increases, the load capacitance of basic gates increases, and delay, respectively, increases by 11.36%, 12.83% and 4.57%.

4.2. Full Adder with Gate-length Biasing Technique.

The adder is an important logical unit in digital systems. The power and speed of adder will greatly affect the performance of digital system [13]. Figure 8 shows two typical adder circuits: mirror adder and transmission gate adder. The size of transistors is also included in Figure 8, where λ =25nm at 45nm process. Two adders have symmetric structure and the same number of transistors. The simulation results are listed in Table 3 and Table 4.

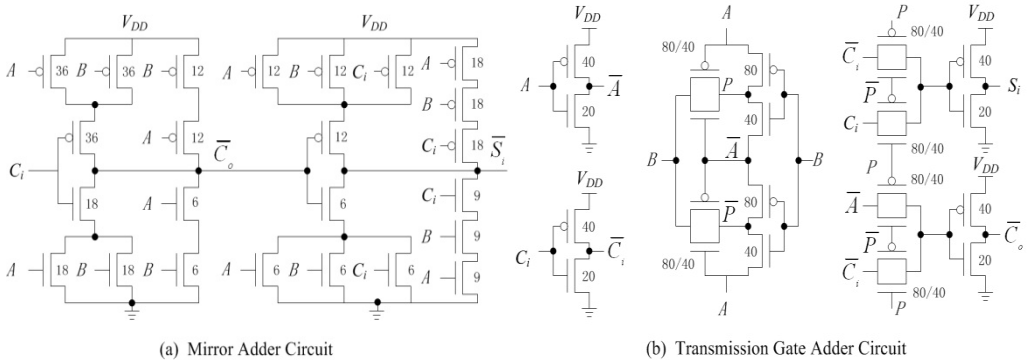

Figure 8. Two Different Models of Adder Circuit

Table 3. Leakage Current of the Two Adders

Input	Leakage current(nA)			
	Mirror adder		Transmission gate adder	
	L=50nm	L=53nm	L=50nm	L=53nm
000	204	188	737.4	680.69
001	199	150	784.93	701.6
010	241	196	749.98	696.1
011	239	193	790.92	709.51
100	235	196	821.75	740.37
101	214	197	760.89	707.03
110	215	201	786.56	703.25
111	223	203	731.89	677.06
Average	221.25	190.5	770.54	701.06
Δ/%		-13.90		-8.90

Table 4. Delay Characteristics of the Two Adders

	Mirror adder		Transmission gate adder	
	L=50nm	L=53nm	L=50nm	L=53nm
T_d(ps)	42.88	48.5	55.67	59.52
ΔT_d%		13.12		6.92

It is clear from Table 3 and Table 4 that leakage current of the gate-length biasing adders has decreased by 13.90% and 8.90%, respectively, than the nominal gate-length adders. Otherwise, delay of the gate-length biasing adders, increased by 13.12% and 6.92%, respectively.

5. The Sequential Circuits Design with the Optimized Gate-length

In sequential circuits design, Flip-Flops are the most important building blocks [14, 15]. Power and performance analysis of Flip-Flops have always been critical due to its applications in data path [2]. In this Section, D Flip-Flop and a 4-bit binary counter with the gate-length biasing technique are discussed. The circuits are simulated using HSIPCE with the frequency of 5M at 45nm process technology. The nominal length is 50nm, and the optimization length is 53nm.The supply voltage of the circuits is 1.0V.

Analysis of combinational logic circuit and sequential logic circuit are different, especially in power and time metrics analysis. The power metric used here is the average leakage power consumed over a constant time interval for various input states and transitions [16, 17].The timing metrics considered includes the clock-to-output propagation delay, setup time and hold time [16].

5.1. D Flip-Flops Design with Gate-length Biasing Technique

This part we analysis the leakage power and time metric of the D Flip-Flop. Two structures of D Flip-Flop are described in Figure 9, and the width of transistors is also presented, where λ =25nm at 45nm process.

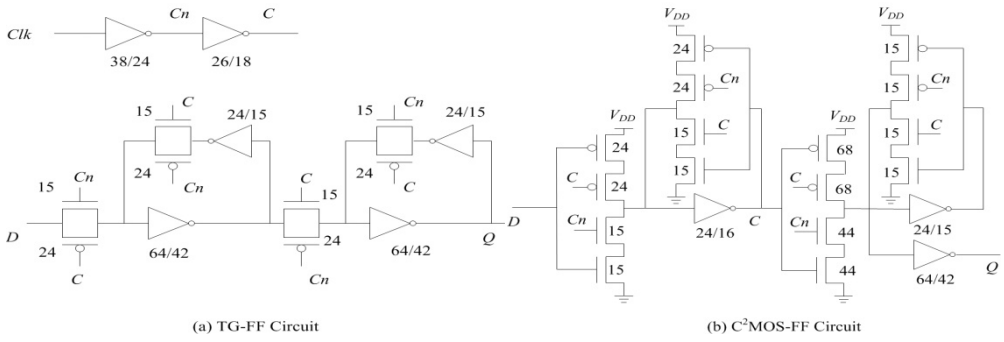

Figure 9. Two Different Structures Model of D Flip-Flop

The leakage power is shown in Table 5. The timing parameters are shown in Table 6. Due to the hold time remain 0 in the design, the parameter isn't listed in Table 6.

Table 5. Leakage Power of D Flip-Flop

Output	Leakage Power(pW)			
	C^2MOS-FF		TG-FF	
	L=50nm	L=53nm	L=50nm	L=53nm
0	0.33	0.22	0.150	0.132
1	0.09	0.08	0.085	0.076
Average	0.21	0.15	0.118	0.104
Δ*Leak-Power*%		-28.57		-11.49

Table 6. Time Characteristics of D Flip-Flop

	Clock-to-out time(ps)		Setup time(ps)	
	L=50nm	L=53nm	L=50nm	L=53nm
C^2MOS-FF	66.496	85.881	50.566	53.318
ΔT_d%		29.15		5.86
TG-FF	41.811	48.755	35.517	36.517
ΔT_d%		16.61		1.66

It can be observed that leakage power of the gate-length biasing Flip-Flops has declined. The average leakage power of C^2MOS-FF and TG-FF with optimized gate-length decreases 28.57% and 11.49%, respectively. The clock-to-out time of the two structures increases 29.15% and 16.61%, respectively. The setup time of the two structures increases 5.86% and 1.66%, respectively.

5.2. A 4-bit Binary Counter with Gate-length Biasing

This part we design a 4-bit binary counter using D Flip-Flops described in 5.1. The structure of a 4-bit binary counter is presented in Figure 10.

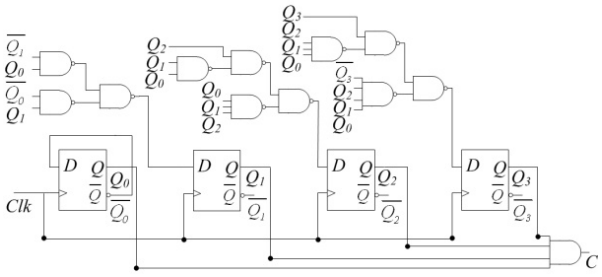

Figure 10. A 4-bit Binary Counter

In Figure 10, combinational gates as for NAND gate and AND gate implemented in this design are using the gate-length biasing technique. The size of the gates is same as in section 4.1. The simulation is carried out with the frequency of 5M at 45nm process technology. The active leakage power and clock-to-out delay are presented in Table 7 and Table 8, respectively.

The average leakage power of 4-bit binary counter using C^2MOS and Transmission Gate D Flip-Flops decrease 38.36% and 20.05%, respectively. At the same time, the clock-to-out delay increase 24.43% and 14.34%, respectively.

Table 7. Active leakage power of the 4-bit binary counters

Output	Active leakage power(fW)			
	C^2MOS-counter		TG-counter	
	L=50nm	L=53nm	L=50nm	L=53nm
0000	254.9	167.9	169.76	134.71
0001	330.3	189.1	193	154.64
0010	309.8	181.4	164.8	129.8
0011	342.2	195.3	208.7	166.8
0100	251	169.8	169.5	134.5
0101	329.6	191.8	198.7	159.5
0110	306.3	191.4	166.6	130.9
0111	362.3	207.7	231.1	184.5
1000	253	170.2	172.1	137.4
1001	327	190.5	195.3	157.5
1010	309	185.5	167.9	133.7
1011	340	197.9	211.9	170.8
1100	253	175.8	174.6	140.2
1101	331	198.9	204.5	165.6
1110	313	203.5	177.5	141.7
1111	264	189	246.6	198
Average	304.775	187.856	190.773	152.516
Δ*Power*%		-38.36		-20.05

Table 8. Clock-to-out Delay of the 4-bit Binary Counters

	C^2MOS-counter		TG-counter	
	L=50nm	L=53nm	L=50nm	L=53nm
T_d(ps)	137.477	171.058	45.047	51.507
ΔT_d%		24.43		14.34

Also, the total power and power-delay product (or PDP) of the 4-bit binary counters are presented in Table 9 and Table 10.

Table 9. Power Dissipation of the 4-bit Binary Counters

	C^2MOS-counter		TG-counter	
	L=50nm	L=53nm	L=50nm	L=53nm
Power(pW)	9.9563	7.1217	4.01556	3.4107
Δ*power*%		-28.47		-15.06

Table 10. PDP of the 4-bit Binary Counters

	C^2MOS-counter		TG-counter	
	L=50nm	L=53nm	L=50nm	L=53nm
*PDP*10^9(fJ)*	1368.762	1218.224	180.889	175.675
Δ*PDP*%		-10.99		-2.88

The simulation results show that the total power dissipation of the counters decreases 28.47% and 15.06%, respectively. The PDP decreases 10.99% and 2.88%, respectively. The PDP can be considered as a quality measure for a switching device [13]. The decrease in PDP means the performance increasing. Therefore, the optimized gate-length biasing is an effective method to improve the performance of circuits.

6. Conclusion

The gate-length biasing technique has discussed by many researchers. A new method to optimize the gate-length is implemented in this work. With the optimized gate-length (L=53nm), typical combinational and sequential circuits are developed and simulated. The HSPICE simulation results show that the leakage of combinational logic circuits and sequential circuits declined with time metrics increasing. Leakage of basic logic gates, 2NAND, 2NOR and 2XOR, decrease 27.4%, 33.6% and 18.8%, respectively. Meanwhile, delay of them increases 11.36%, 12.83% and 4.57%, respectively. Two structures of adder, mirror adder and

transmission gate adder decrease 13.9% and 8.9%. Along with that delay of the adders increases 13.12% and 6.92%, respectively. In addition, sequential circuits like C^2MOS D Flip-Flop and Transfer-Gate D Flip-Flop reduce the leakage power 28.57% and 11.49%, respectively. At the same time, the clock-to-out time of them raises 29.15% and 16.61%, respectively. A 4-bit binary counter with different structures decline the total power dissipation 28.47% and 15.06%, among them the leakage power dissipation decrease 38.36% and 20.05%, respectively. Otherwise, the clock-to-out time of the 4-bit binary counters raises 24.43% and 14.34%, respectively. The results indicate that it is effective for the standby power dissipation reduction of electronic equipment with the optimized gate-length. Moreover, the PDP is decreased when the sequential circuits work while frequency is 5M. It is also obvious for saving power dissipation while the electronic equipment is working in low-frequency.

Acknowledgements

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References

[1] Kavita Mehta, Neha Arora, BP Singh. *Low Power Efficient D Flip Flop Circuit.* Proceedings of the International Symposium on Devices MEMS, Intelligent Systems & Communication. 2011; 16-19.
[2] Ch Daya S agar, T Krishna Moorthy. Design of a Low Power Flip-Flop Using MTCMOS Technique. *International Journal of Computer Applications & Information Technology*. 2012; 1(1): 19-21.
[3] Puneet Gupta, Puneert Sharma. Gate-Length Biasing for Runtime-Leakage Control. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems.* 2006; 25(8): 1475-1485.
[4] Puneet Gupta, Andrew B Kahng, Puneet Sharma, Dennis Sylvester. *Selective Gate-Length Biasing for Cost-Effective Runtime Leakage Control.* Proceedings of the Design Automation Conference (DAC'04). 2004; 7(11): 327-330.
[5] Amit Agarwal, Saibal Mukhopadhyay, Arijit Raychowdhury, Kauchik Roy, Chris H.Kim. *Leakage Power Analysis and Reduction for nanoscale Circuits*. IEEE Computer Society. 2006; 26(2): 68-80.
[6] A Agarwal, S Mukhopadhyay, CH Kim, A Raychowdhury, K Roy. *Leakage Power Analysis and Reduction: Models, Estimation and Tools.* IEE Proceedings on Computers and Digital Techniques. 2005; 152(3): 353-368.
[7] Liqiong Wei, Zhanping Chen, Mark Johnson, Kaushik Roy. *Design and Optimization of Low Voltage High Performance Dual Threshold CMOS Circuits.* Proceedings of the Design Automation Conference (DAC'98). 1998; 489-494.
[8] Gang Yang, Jin Liu. An Algorithm for Quantitatively Calculating I/Q Gain and Phase Mismatch. *TELKOMNIKA Indonesian Journal of Electrical Engineering*. 2012; 10(4): 812-817.
[9] Naran Sirisantana, Liqiong Wei, Kaushik Roy. *High-Performance Low-Power CMOS Circuits Using Multiple Channel Length and Multiple Oxide Thickness*. Proceeding of the International Conference on Computer Design (ICCD'00). 2000; 227-232.
[10] Amit Agarwal, Chris H Kim, Saibal Mukhopadhyay, Kauchik Roy. *Leakage in Nano-Scale Technologies: Mechanisms, Impact and Design Considerations*. Proceedings of the Design Automation Conference, (DAC'04). 2004; 6-11.
[11] Xi X, Dunga M, He J, et al. BSIM4.6.4 MOSFET model user's manual. Available in http://www-device.eecs.berkeley. edu/~bsim3/bsim4.html.
[12] Narendra SG, Chandrakasan A. Leakage in nanometer CMOS technologies. New York: Springer. 2006.
[13] Jan M Rabaey, Anantha Chandrakasam, Borivoje Nikolic. Digital Integrated Circuits: A Design Perspective, Pearson Education, Inc, Prentice-Hall, Second Edition. 2003.
[14] M Janaki Rani, S Malarkann. Leakage Power Reduction and Analysis of CMOS Sequential Circuits. *International Journal of VLSI design & Communication Systems (VLSICS'12)*. 2012; 3(1): 13-23.
[15] D Harikrishna, NV Srikanth. Dynamic Stability Enhancement of Power Systems Using Neural-Network Controlled Static-Compensator. *TELKOMNIKA Indonesian Journal of Electrical Engineering*. 2012; 10(1): 9-16.
[16] R Ramanarayanan, N Vijaykrishnan, MJ Irwin. *Characterizing Dynamic and Leakage Power Behavior in Flip-Flops*. Proceeding of the 15th Annual IEEE International ASIC/SOC Conference. 2002.
[17] Dejan Marković, Borivoje Nikolić, Robert W. Brodersen. *Analysis and Design of Low-Energy Flip-Flops.* Proceeding of the International Symposium on Low Power Electronics and Design (ISLPED'01). 2001; 52-55.