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Improved Performance of Four Switch Three Phase with SEPIC-Based Inverter

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Abstract

The proposed novel four-switch three-phase (FSTP) inverter is to design to reduce the rate, difficulty, mass, and switching losses of the DC-AC conversion system. Here the output line voltage cannot exceed half the input voltage in the out-dated FSTP inverter and it operates at half the DC input voltage. Single-Ended Primary-Inductance Converter (SEPIC) is a novel design for the FSTP inverter proposed in this paper. In this proposed topology the necessity of output filters is not necessary for the pure sinusoidal output voltage. Related to out-dated FSTP inverter, the proposed FSTP SEPIC inverter raises the voltage utilization aspect of the input DC supply, where the suggested topology delivers the higher output line voltage which can be extended up to the full value of the DC input voltage. In the proposed topology a control used called the integral sliding-mode (ISM) control and this control is used to enhance its dynamics and to ensure strength of the system during different operating conditions. Simulation model and results are used to authorise the proposed concept and simulations results show the effectiveness of the proposed inverter.

Keywords*: SEPIC converter, Integral Sliding mode control, FSTP*

1. Introduction

The conventional six-switch three-phase (SSTP) voltage source inverter shown in Figure 1 has found well-known industrial tenders in different forms such as lift, cranes, conveyors, motor drives, renewable energy conversion systems, and active power filters. However, in some low power range applications, reduced switch count inverter topologies are considered to alleviate the volume, losses, and cost. Some research efforts have been directed to develop inverter topologies that can achieve the aforesaid goal. By the results obtained it shows that it has a possibility to implement a three-phase inverter with the usage of only four Switches [1]. In four- switch three-phase (FSTP) inverter, two of the output load phases are sustained from the two inverter legs, while the middle point of the DC-link of a split-capacitor bank is connected to the third load phase. Recently, the FSTP inverter has attracted features like its performance, control, and applications [2- 4] etc.

Compared to the out-dated SSTP inverter, the FSTP inverter has various benefits such as reduction in cost and reliability increased due to the reduction in the number of switches, conduction and switching losses is reduced by 1/3, where one complete leg is omitted, and compact number of interface circuits to supply PWM signals for the switches. The FSTP inverter can also be operated in fault tolerant control to solve the open/short circuit fault of the SSTP inverter [2]. On the other hand, there are some drawbacks of the conventional FSTP inverter which should be taken into consideration. Similar to the traditional SSTP inverter, the FSTP inverter achieves only buck DC-AC conversion.

However, this adds major difficulty and hardware to the power conversion system and waste the merits of the reduced switch count. Also, the FSTP inverter topology is not symmetrical; while the two inverter legs are directly connected to the two load-phases, the center tap of split DC-link capacitors is connected to the third load-phases. This forces the current of the third phase to flow through the DC-link capacitors, hence a fluctuation will predictably seem in the two capacitors' voltages, which correspondingly changes the output voltage [4]. Additionally, if the DC-link split-capacitors have not equal values, there is a

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opportunity of over-modulation of the pulse-width modulation process in order to compensate this difficulty [5].

This paper proposes a novel design of the FSTP inverter topology based on the single-ended primary inductance DC-DC converter (SEPIC). The SEPIC converter is a fourth-order nonlinear system that is widely used in step-down or step-up DC-DC switching circuits, photovoltaic maximum power point tracking [6], and power factor correction circuits [7,8, 9] due to its encouraging features as the non-inverting output voltage buck-boost capability and lower input current ripple content. Based on the above-mentioned advantages, SEPIC converter has been recently researched by scholars in various topologies in many diversified studies [10, 11].

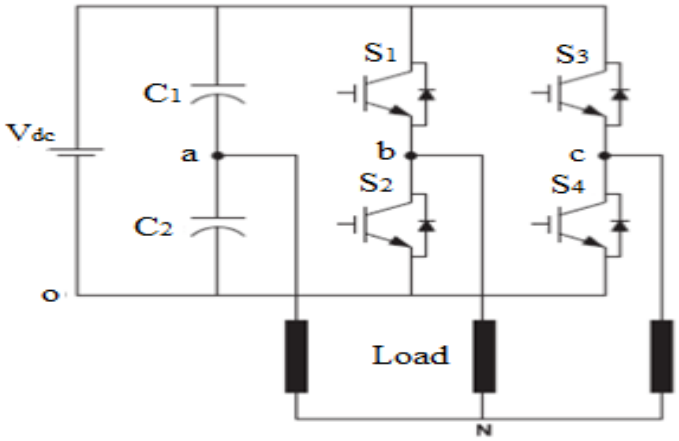

Figure 1. Conventional FSTP voltage source inverter

Although the proposed FSTP SEPIC inverter has not a voltage boost competency, it can produce an output voltage higher than that of the conventional FSTP voltage source inverter by two factors. i) The voltage utilization factor of the input DC supply will increase. ii) Another attractive feature is that the output voltage of the proposed SEPIC inverter is a pure sine wave, therefore the filtering requirements is reducing at the output side. Also, there is no dynamic need to insert a dead-band between the same-leg switches, which expressively reduces the output waveform distortion and gain non-linearity.

2. The Principle of Operation of Proposed FSTP SEPIC Inverter

Two SEPIC converters are present in the proposed FSTP SEPIC inverter, and it can attain DC–AC conversion as shown in Figure 2a and b respectively. Where the two phases of the three-phase load is connected to the output of a two DC–DC SEPIC converters which are sinusoidally modulate. While the input DC source third phase is directly connected to the input DC source. Both SEPIC DC-DC converters produce a DC-biased sine wave output, so that each converter produces a unipolar voltage. The sinusoidal modulation of each converter is 120° shifted to generate three-phase balanced load voltage and the DC-bias is exactly equal to the input DC voltage. Since the DC input supply and load is connected differentially across the two converters and thus whereas a DC bias appears at each end of the load with respect to ground, the differential DC voltage across the load is zero and the bipolar voltage is generate across the load, which requires the DC–DC SEPIC converters to be current bi-directional. The bi-directional SEPIC DC–DC converter is shown in Figure 3, while the configuration of the proposed FSTP SEPIC DC-AC inverter is shown in Figure 4.

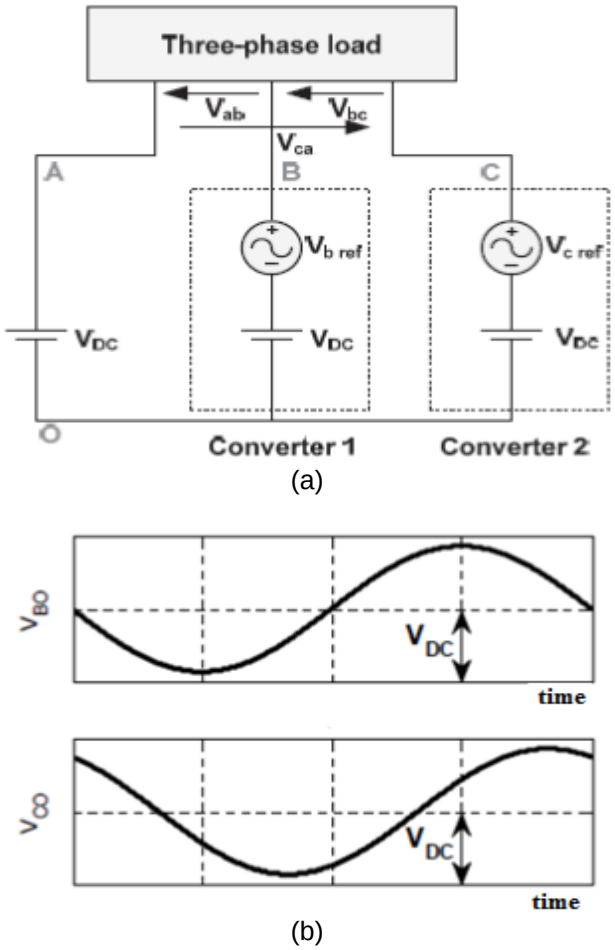

Figure 2. A basic approach to achieve DC-AC conversion with four switches using two SEPIC DC-DC converters (a) reference output voltage of the first converter, (b) reference output voltage of the second converter

As shown in Figure 3, the bi-directional SEPIC converter includes DC input voltage V_{dc}, input inductor L_1, two complementary power switches $S_1^{'}, S_1$, transfer capacitor $S_1^{'}, S_1 L_1 C_1 C_2 R_0$, output inductor L_2 and output capacitor C_2 feeding a load resistance R_0.

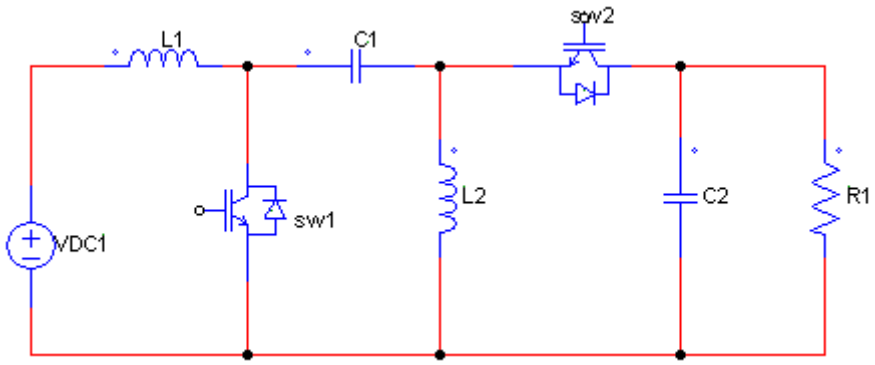

Figure 3. Bi-directional SEPIC converter

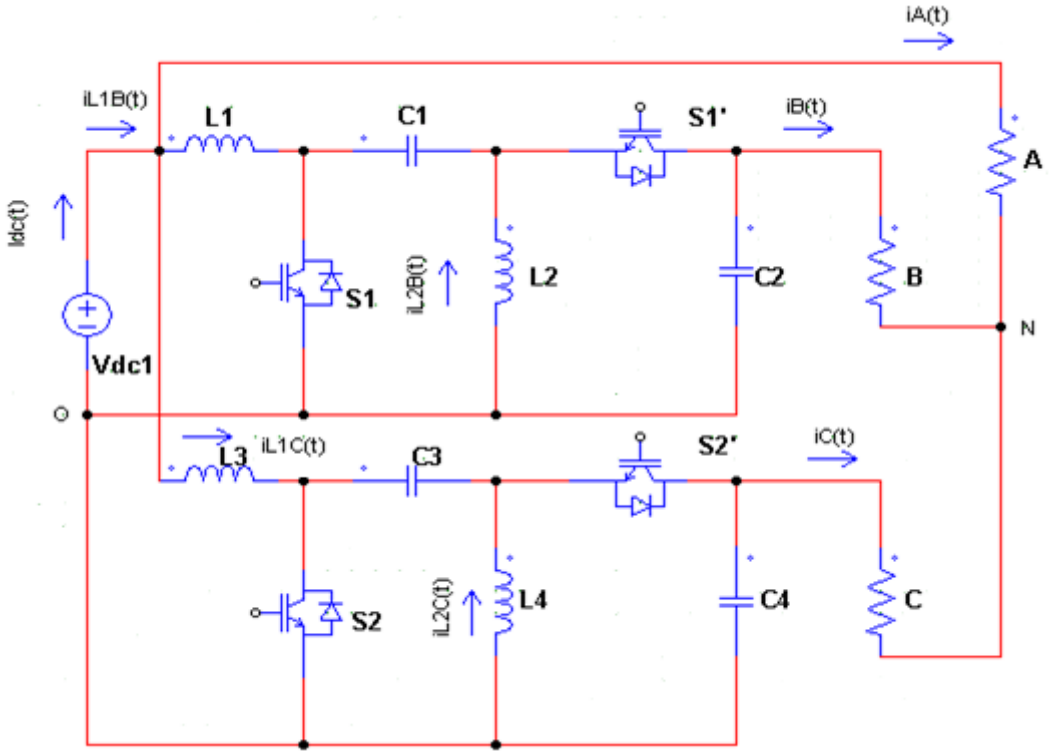

Figure 4. Proposed FSTP SEPIC inverter

SEPIC operation core implies charging the inductors L_1 and L_2 during the ON state of the switching period taking the energy respectively from the input source and from the transfer capacitor $S_1^{'}, S_1 L_1 C_1 C_2 R_0$, and discharging them simultaneously into the load through the switch $S_1^{'}$ during the OFF state of the switching period. Depend upon the duty cycle the output voltage of the SEPIC DC-DC converter may be less or more than the input voltage. Output and input voltage relation is explained in the equation as follows.

$$V_0 = \frac{D}{1-D} V_{in} \tag{1}$$

Where D is the duty cycle, while V_0 and V_{in} are the output and input voltage of the converter respectively. The reference voltage of each converter with respect to the ground implies that the sinusoidal modulation of each SEPIC converter. The reference voltage of each converter with respect to the ground is given by

$$\begin{aligned} V_{B0}(t) &= V_{DC} + V_{bref} = V_{DC} - V_{mL-L} \sin(\omega t) \\ V_{C0}(t) &= V_{DC} + V_{cref} \\ &= V_{DC} + V_{mL-L} \sin(\omega t + 2\pi/3) \end{aligned} \tag{2}$$

Where ω is the desired radian frequency, while V_{mL-L} peak of the desired line to line output voltage. Thus, established on Kirchhoff's voltage law in Figure 4, the output line voltages across the load are given by:

$$
\begin{aligned}
V_{AB}(t) &= V_{DC} - [V_{DC} - V_{mL-L}\sin(\omega t)] = V_{mL-L}\sin(\omega t) \\
V_{BC}(t) &= V_{DC} - V_{mL-L}\sin(\omega t) = V_{mL-L}\sin(\omega t - 2\pi/3) \\
V_{CA}(t) &= V_{DC} + V_{mL-L}\sin(\omega t + 2\pi/3) - V_{DC} \\
&= V_{mL-L}\sin(\omega t + 2\pi/3)
\end{aligned} \tag{3}
$$

Although the FSTP SEPIC inverter can give an output line voltage up to a value equals the voltage of the input source (V_{DC}) as indicated by equation (2). To avoid operating at zero duty it is recommended to define V_{mL-L} lower than the value of the input DC (i.e. minimum duty cycle is selected to be slightly higher than zero).

Accurate selection of passive elements of SEPIC converter is necessary for successful DC-AC conversion and requires information of the instantaneous capacitors voltages and inductors currents. The voltage across the output capacitors has been given by equation (2). Based on the basics concept of DC-DC SEPIC converter, input DC voltage is equal to the average voltage across the coupling capacitor, while the current through the output inductor and output load current is to be equal.

The load phase currents are given by equation (4),

$$
\begin{aligned}
i_A(t) &= I_m \sin(\omega t - \phi - \pi/6) \\
i_B(t) &= I_m \sin(\omega t - \phi - 5\pi/6) \\
i_C(t) &= I_m \sin(\omega t - \phi - \pi/2)
\end{aligned} \tag{4}
$$

Where I_m is the peak value of load current, and ϕ is the phase of the load impedance (Z_L). The input inductor current for both SEPIC converters can be achieved by applying energy balance rule for each SEPIC converter. Assuming ideal converters, the input inductor currents for both converters are given by,

$$
\begin{aligned}
i_{L1C}(t) &= \frac{i_C(t)V_{CO}(t)}{V_{DC}} = i_C(t)\frac{V_{DC}+V_{mL-L}\sin(\omega t+2\pi/3)}{V_{DC}} \\
i_{L1B}(t) &= \frac{i_B(t)V_{BO}(t)}{V_{DC}} = i_B(t)\frac{V_{DC}-V_{mL-L}\sin(\omega t)}{V_{DC}}
\end{aligned} \tag{5}
$$

From equation (5), it shows that the average values of both input inductor currents are equal only at a pure resistive load (unity power factor), in this event, same amount of power to the load side will be transferred by the both SEPIC converter. Otherwise, the average currents will be unequal (according to equation (5)), i.e. SEPIC converters will transfer different amount of power to the load side.

The proposed inverter topology of DC input current $(i_{DC}(t))$ is equal to the summation of the load current drawn by phase A $(i_A(t))$, and the input inductors currents of both SEPIC converters $(i_{L1B}(t))$ and $(i_{L1C}(t))$ as follows.

$$
\begin{aligned}
i_{DC}(t) &= i_A(t) + i_{L1C}(t) + i_{L1B}(t) \\
&= i_A(t) + i_B(t)\frac{V_{DC}-V_{mL-L}\sin(\omega t)}{V_{DC}} \\
&\quad + i_C(t)\frac{V_{DC}+V_{mL-L}\sin(\omega t+2\pi/3)}{V_{DC}}
\end{aligned} \tag{6}
$$

Where $i_A(t)$ is the load current of phase A as described in equation (4), which is drawn directly from the DC input source, Substituting equation (4) into (7), the DC supply current could be given in the following form:

$$i_{DC}(t) = \frac{\sqrt{3}V_{mL-L}I_m}{2V_{DC}}\sin(\phi + \pi/2) \quad (7)$$

Equation (7) shows that the DC supply current drawn by the proposed inverter topology is constant. For line-to-line voltage peak of 86.66% of the DC input voltage, the normalized load current drawn by phase A $i_A(t)/l_m$, normalized input inductor current for each SEPIC converter $i_{L1B}(t)/l_m$, and $i_{L1c}(t)/l_m$ the normalized DC input current $i_{DC}(t)/l_m$ are different load power factors.

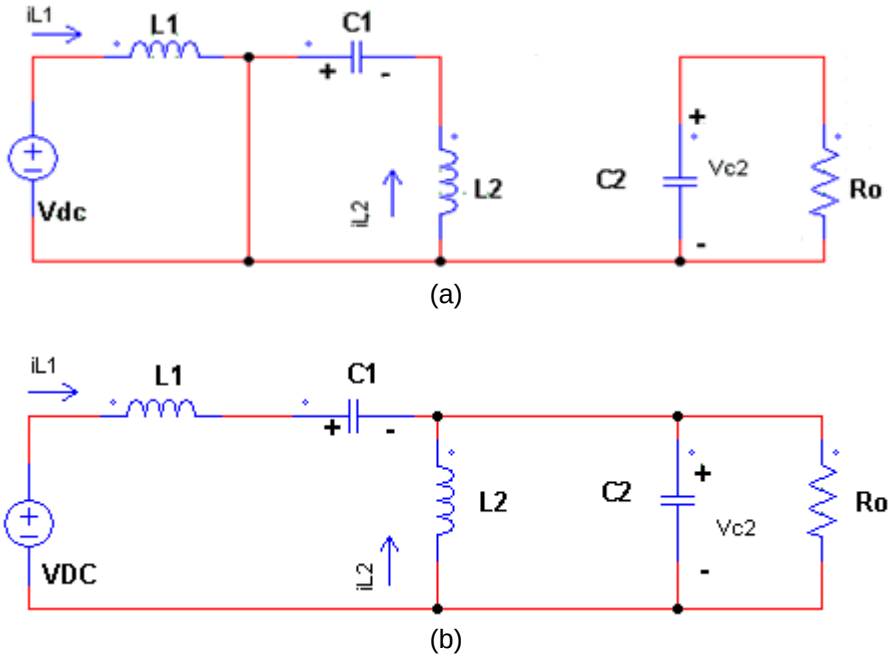

Figure 5. SEPIC equivalent circuit for (a) switch ON and (b) switch OFF

The input currents of both SEPIC converters are symmetrical in unity power factor with the same average value. At lagging/leading power factors, the input currents of both SEPIC converters have different waveforms with unequal average value for lagging/leading power factors. The converter is controlled through two complementary switches, having the control signal as its duty cycle, and is assumed to operate in continuous conduction mode (CCM). Hence, there are two state space representations during both ON and OFF state of the switch. The equivalent circuits of the SEPIC converter during ON and OFF states are shown in Figure 5a and b respectively.

3. Control Strategy

To drive the proposed FSTP SEPIC inverter a robust control strategy is required. This is due to the fact that the input DC voltage is equal to the voltage of one of the three-output phases with respect to the common point. Thus, any abnormality in the output voltage of the two SEPIC DC-DC converters from the desired DC-biased sine-wave reference leads to an important unbalance in the three-phase output line voltages.

3.1. Sliding Mode Control

Sliding-mode control (SMC) is a non-linear control theory which covers the properties of hysteresis control to multivariable environments. It is able to constrain the system status to follow trajectories which lie on a suitable surface in the state space (the sliding surface) [12, 13,

14]. The main advantages of SMC are the fast dynamic in response and the guarantee of stability and robustness for large differences of system parameters and against perturbations. Additionally, given its flexibility in terms of synthesis, SMC is relatively easy to apply when compared to other types of non-linear control. Though, its application to power converters should be considered for each converter severally. As a control method, SMC has been applied to basic DC-DC and complex converters. Although most authors discuss the generalization of their developed methods to other high-order converters, this does not imply to all converters because the difference in circuit topology totally changes the system's performance even if it is of the same order.

3.2. Sliding Surface

While the output voltage V_{C2} of each SEPIC converter is the final control target, it will be incredible for the closed loop controlled system to reach stable motion on the sliding surface if V_{C2} is only selected to be the direct control target, thus the other variables should be chosen.

Then, it is proposed to upturn the number of state variables as low as possible in the sliding surface. To avoid a large number of tuning gains, a surface containing the output voltage in addition to the input current could be chosen as given by (8).

$$S(i_{L1},V_{C2}) = \alpha_1 e_1 + \alpha_2 e_2 \tag{8}$$

Where α_1 coefficients and α_2 are gains, while e_1 and e_2 are the feedback errors of the state variables i_{L1} and V_{C2} respectively, and given by (9).

$$\begin{aligned} e_1 &= i_{L1ref} - i_{L1} \\ e_2 &= V_{C2ref} - V_{C2} \end{aligned} \tag{9}$$

The reason for choosing i_{L1} instead of i_{L2} is to allow the sliding surface to directly control the input of each converter in addition to its output, which is steadier than the other cases. At an extremely high switching frequency, the sliding-mode controller will ensure that both input inductor current and output capacitor voltage are controlled to follow exactly their sudden references i_{L1ref} and V_{C2ref} respectively. However, in the case of fixed frequency or finite frequency sliding-mode controllers, the control is unsatisfactory, where steady-state errors occur at both inductor current and output capacitor voltage. To introduce an additional integral term of the state variables is the good method for conquering these errors into the sliding surface. Therefore, an integral term of these errors is introduced into the sliding-mode controller as an additional controlled state-variable to reduce these steady-state errors. This is commonly known as integral sliding-mode control (ISMC) shown in figure 6 and the sliding surface is selected as specified by equation (10):

$$s = \alpha_1 e_1 + \alpha_2 e_2 + \alpha_3 e_3 \tag{10}$$

Where α_1, α_2 and α_3 represent the desired control parameters denoted sliding coefficients, while e_1, e_2 are given in above sliding surface and e_3 are expressed as:

$$e_3 = \int (e_1 + e_2) dt \tag{11}$$

To obtain the dynamic model substituting the SEPIC state-space models under CCM into the time derivative.
Where the three-state errors time derivative given by:

$$\frac{de_1}{dt} = \frac{d\left(i_{L1ref} - i_{L1}\right)}{dt}$$
$$\frac{de_2}{dt} = \frac{d\left(V_{C2ref} - V_{C2}\right)}{dt}$$

$$\frac{de_3}{dt} = e_1 + e_2 \quad (12)$$

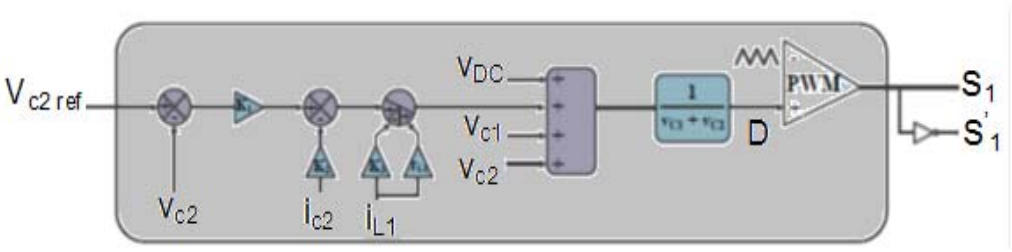

Figure 6. Integral sliding-mode controller for SEPIC converter

3.3. Double-Integral Sliding-Mode Control

To upturn the effectiveness of the integral sliding-mode control, an additional double-integral term of the state variables error could be presented in the sliding surface. This is the so-called double-integral sliding-mode (DISM) controller as shown in figure 7. Thus, the DISM controller has the following sliding surface:

$$s = \alpha_1 e_1 + \alpha_2 e_2 + \alpha_3 e_3 + \alpha_4 e_4 \quad (13)$$

While e_1, e_2 , e_3 are given in the above sliding surface and e_4 are expressed as: Where the stator error is defined as:

$$e_4 = \int\int (e_1 + e_2)dt \quad (14)$$

$\frac{de_1}{dt}, \frac{de_2}{dt}, \frac{de_3}{dt}$ is derived in above equation Substituting the SEPIC state-space models under CCM into the time derivative of (14) gives the dynamical model of the system as:

$$\frac{de_4}{dt} = \int (e_1 + e_2)dt \quad (15)$$

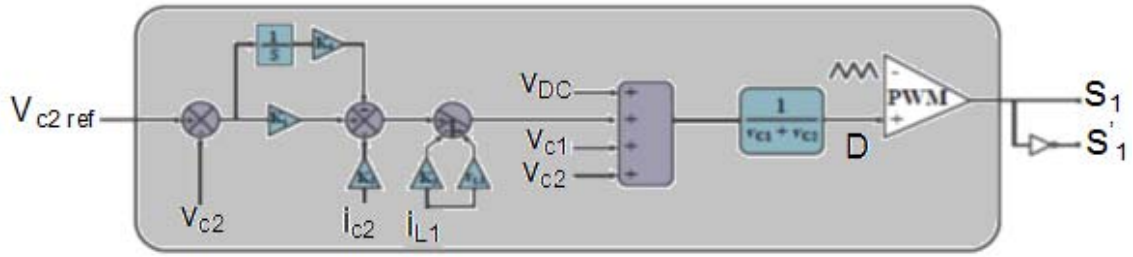

Figure 7. Double-integral sliding-mode controller for SEPIC converter

4. Simulation Results

During different conditions the performance of the proposed FSTP SEPIC inverter using the sliding-mode control strategy has been investigated. The simulation results are shown in Figure 8 and 9.

Figure 8 shows that the inverter performance during normal operating conditions, where Figure 8a shows the both converters output capacitor voltage, while Figure 8b shows the three phase output line voltages of the inverter. In Figure 8c, the both SEPIC converters input inductor current is illustrated. The input current of the DC supply is shown in Figure 8d. Figure 9 shows the step response of the inverter, where Figure 9a exhibits the enactment of the inverter under a step change in the load reference voltage from 50 to 100% with doubled frequency, while Figure 9b.

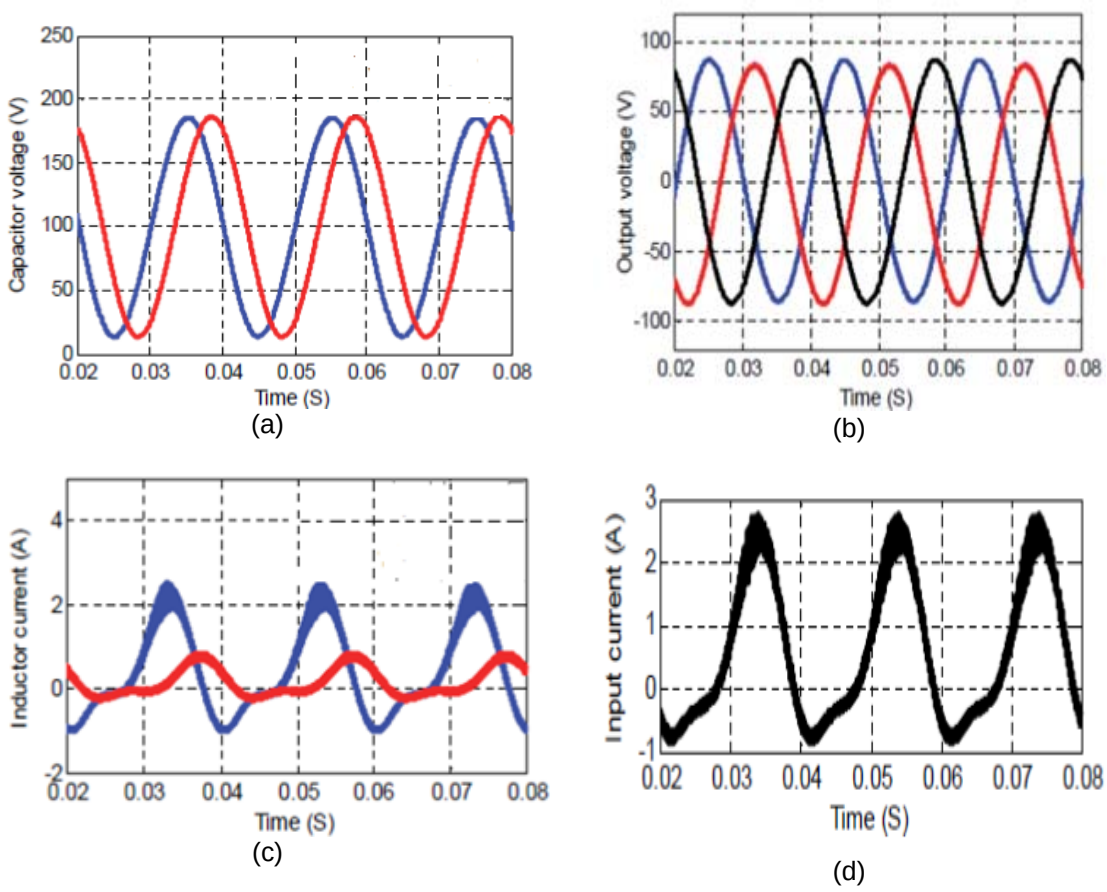

Figure 8. Performance of the FSTP SEPIC inverter under normal operating conditions, (a) Output capacitor voltage of both SEPIC converters, (b) Three phase output line voltages, (c) Input inductor current of both SEPIC converters, (d) DC supply current

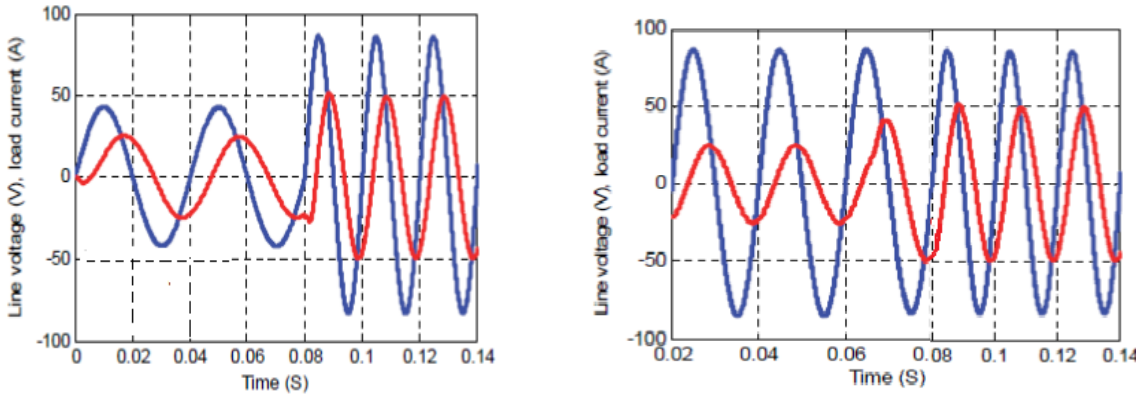

Figure 9. Step response of the FSTP SEPIC inverter, (a) Load voltage and load current for a step change of the reference load voltage from 50 to 100% with doubled frequency, (b) Load voltage and load current for a load step change from 50 to 100%

5. Conclusions

A DC-AC four-switch three-phase SEPIC-based inverter is proposed in this paper. The proposed inverter improves the operation of the DC bus by a two factor when it compared to the conventional four-switch three-phase voltage source inverter. Then, without need for an output filter, it can produce a pure sinusoidal three-phase output voltage. Unlike conventional four-switch three-phase inverter, the proposed inverter does not suffer from the problems of voltage fluctuation across the DC link split-capacitors and without circulation in any passive component the third phase load current is directly drawn from the DC source. A sliding-mode controller was designed and applied to the reduced second- order model of the SEPIC DC-DC converter. Simulation results verified the performance of the proposed inverter.

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