

Single Phase Variable Sampling Phase Locked Loop using Composite Observer

K Arun, K Selvajothi*

Department of Electronics Engineering, Indian Institute of Information Technology Design & Manufacturing, Kancheepuram, Chennai – 127, India

*Corresponding author, e-mail: ksjoythi@iiitdm.ac.in

Abstract

An observer based variable sampling period phase locked loop is introduced for grid connected systems. The composite observer acts as an efficient estimator of the fundamental components from a periodic input signal rich in DC and harmonics. The observer gains are designed using pole placement technique, which inherently ensures the stability of this estimator. Even under drift frequency, a constant number of samples (512) per cycle are maintained with the help of the numerically controlled oscillator. This makes the oscillator gain elements in the observer a constant and eliminates the trigonometric computation. This phase locked loop is found to be working in a wide range of frequency 40- 70Hz. The performance of the proposed scheme is studied with a synthetic harmonic rich signal as well as validated by implementing the PLL in Cyclone IV FPGA with a real time grid voltage.

Keywords: composite observer, harmonics, numerically controlled oscillator, phase locked loop, variable sampling

Copyright © 2016 Institute of Advanced Engineering and Science. All rights reserved.

1. Introduction

Accurate estimation of magnitude, phase and frequency play a key-role in interfacing grid connected systems such as renewable energy integration, active power filter, uninterrupted power supply, dynamic voltage restorer, power quality studies etc [1-3]. Phase Locked Loop (PLL) is widely used to estimate the phase information. Several PLL schemes have been discussed in literature for single phase systems. Three main components of PLL are phase detector, loop filter and voltage controlled oscillator [4]. The classification of PLL is mainly based on the type of phase detector used, such as stationary (product) type and synchronous (Park transformation) type. In stationary type phase detector the phase error is calculated as the product of input and the estimated quadrature component from the PLL. Here, the double frequency components will be retained in the phase error even after steady state is reached. The low pass filter introduced to remove the double frequency component, increases the estimation time of the PLL. A modified phase detector [5] designed using state variable feedback is discussed to remove the double frequency content without using the low pass filter.

Synchronous reference frame PLLs using Park transformation type phase detector are existing in literature for single phase systems. The Park transformation helps in removing the double frequency content. Several schemes can be used to generate the orthogonal components. Delay by quarter cycle, Hilbert transformation, all pass filter, second order generalised integrator (SOGI), inverse Park, sliding discrete fourier transform (SDFT) and Kalman based PLLs are some methods discussed in literature. Delay by quarter cycle [6] fails when there is a drift in input signal frequency. Modified delay based methods reduce the errors in the estimated parameters of the PLL [7] even in presence of harmonics and drift in frequency condition. Hilbert transformation based methods show poor performance when there is a drift in frequency [6]. All pass filter [5] is adaptive to frequency drifts, but cannot be used in distorted condition of the input signal. Second order generalized integrator (SOGI) [8, 9] PLL and inverse Park PLL methods are also adaptive to frequency changes [10, 11]. The performance of these two methods are equivalent to each other [10]. In [12] SDFT act as a pre-filter for DC and harmonics of the input signal. Kalman based PLL [13] is also used to eliminate the harmonics of the input signal. Apart from the above mentioned schemes enhanced PLL (EPLL) [14] is also available in literature which is equivalent to SRF-PLL [15] and this method does not require

additional orthogonal components to be generated. When the DC offset is present in the input signal, a DC block is introduced in parallel with the fundamental block in [16]. For a harmonic rich input signal, the in-loop filter [17] and parallel arrangement of multiple EPLL [18] blocks are used. All the PLLs mentioned above work on constant sampling period.

Variable sampling period based schemes like moving average filter, SDFT and cascaded delayed signal cancellation used as filter are presented [19-21] for distorted grid condition in single phase systems. The main advantage of the variable sampling PLL is that it gives constant number of samples per cycle even under drift frequency. Thus, lends it suitable for power quality applications. In variable sampling schemes, the sampling pulses are generated by dividing the hardware clock [19-20], which limits the number of samples per cycle. In this paper, to make the PLL independent of hardware, the sampling pulses are generated through a standard coupled oscillator with automatic gain control [21-22]. Multiresonant filters [23], adaptive notch filters [24] and Kalman filter based recursive algorithm [25] are used to estimate the fundamental and harmonics. Composite observer based harmonics extraction discussed in [26] utilizes simple observer structure described using pole placement technique. These schemes use parallel structures for estimation of individual components.

In this paper, a composite observer is used to estimate DC and harmonic components along with the fundamental components to design a PLL for harmonically distorted grid environment. Study of PLL using simple observer has shown that it is suitable only when the input signal is free from harmonics. Composite observer aids in introducing any number of blocks depending on the harmonic content in the input signal. Also there is another advantage that the speed of estimation can be adjusted by choosing the closed loop pole location. Thus, there is a trade off between the estimation time and the bandwidth for the chosen pole. Simulation study has been done for various conditions such as sudden change in amplitude, frequency and phase angle in presence of harmonics. This proposed scheme has 2^N samples per cycle which enhances its suitability in any signal processing applications. This paper is organized as follows: section 2, proposes a variable sampling PLL for a harmonically distorted grid condition. In section 3, transfer function model of the scheme is deduced and validated through phase disturbance. Section 4, discusses the results of the proposed PLL through simulation and experiment.

2. Observer Based Variable Sampling SRF-PLL

The block diagram of the proposed variable sampling PLL is shown in Figure 1. The main components of this proposed PLL are the variable sampling period composite observer used as an estimator and the sampling generator. In this scheme, discrete time composite observer estimates DC, in-phase and quadrature axis components of fundamental as well as harmonics from a harmonic rich periodic input signal. The fundamental in-phase and quadrature signals are transformed to direct and quadrature axis components using the Park transformation. The quadrature axis component is processed through a PI controller. This control signal (phase error) is fed after correction in to the sampling generator to produce the enabling pulses for the observer and a counter. The sampling generator is a numerically controlled oscillator (NCO) with automatic gain control. The NCO generates a constant number of samples per cycle of the input signal independent of hardware clock frequency. The counter output is used to generate the unit sine and cosine signals for the Park transformation. The composite observer and the NCO for this PLL are discussed briefly in the following subsections.

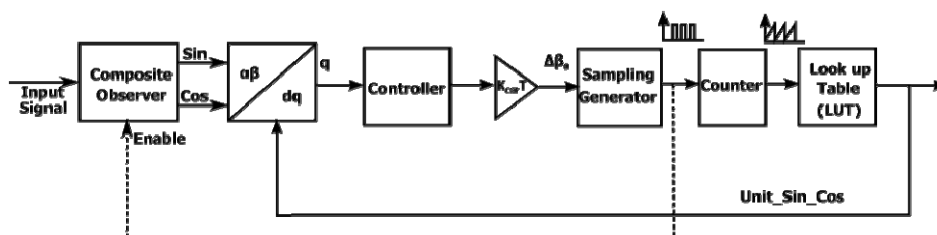


Figure 1. Structure of proposed Variable sampling SRF-PLL

2.1. Composite Observer

A variable sampling period composite observer estimates the in-phase and quadrature components of the input signal for this Park type PLL. The design of observer feedback gains is the same using pole placement technique in both constant sampling composite observer [26] and the variable sampling composite observer. Any periodic signal can be represented in Fourier series as the sum of integer multiples of the fundamental frequency of the input signal. Hence, the blocks in the composite observer are arranged in parallel to estimate the individual frequency components. The state space model of an observer is given by:

$$\begin{aligned} \hat{x}((k + 1)T) &= A\hat{x}(kT) + L(y(kT) - \hat{y}(kT)) \\ \hat{y}(kT) &= C\hat{x}(kT) \end{aligned} \tag{1}$$

where, A-system matrix, L-observer feedback gain vector, C-output vector, $\hat{x}(kT)$ – state vector and $\hat{y}(kT)$ – output of the observer. The representation of the state space model and the design requirements for simple and composite observer is tabulated in Table I.

Table 1. Representation of state space model and design requirements for simple and composite observer

	Simple observer	Composite observer
System Matrix (A)	$A = \begin{bmatrix} \alpha_1 & (\alpha_1 - 1) \\ (\alpha_1 + 1) & \alpha_1 \end{bmatrix}$ where $\alpha_1 = \cos(\omega T)$ $T = \frac{0.02}{512}$	$A = \begin{bmatrix} 1 & 0 & 0 & \dots & 0 & 0 \\ 0 & \alpha_1 & (\alpha_1 - 1) & \dots & 0 & 0 \\ 0 & (\alpha_1 + 1) & \alpha_1 & \dots & 0 & 0 \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ 0 & 0 & 0 & \dots & \alpha_m & (\alpha_m - 1) \\ 0 & 0 & 0 & \dots & (\alpha_m + 1) & \alpha_m \end{bmatrix}$ n=0,1,3...m
Observer feedback gain vector (L)	[L ₁₁ L ₁₂]	[L ₀ L ₁₁ L ₁₂ ... L _{m1} L _{m2}]
Output vector (C)	[1 0]	[1 1 0 ... 1 0]
State vector (x)	[x ₁₁ x ₁₂]	[x ₀ x ₁₁ x ₁₂ ... x _{m1} x _{m2}]
Closed loop characteristic equation of the observer	zI - A + LC = 0	zI - A + LC = 0
Desired pole location	$z = e^{-a\omega T} (a_1 \pm jb_1)$ where $b_1 = \sin(\omega T)$ w- fundamental frequency	$z = e^{-a\omega T} a_0 e^{a\omega T} (a_1 \pm jb_1),$ $\dots e^{-a\omega T} (a_m \pm jb_m)$
Desired characteristic equation	$(z - e^{-a\omega T} (\alpha_1 + j\beta_1))(z - e^{-a\omega T} (\alpha_1 - j\beta_1)) = 0$	$(z - e^{-a\omega T} \alpha_0) \cdot (z - e^{-a\omega T} (\alpha_1 + j\beta_1))(z - e^{-a\omega T} (\alpha_1 - j\beta_1)) \dots$ $\dots (z - e^{-a\omega T} (\alpha_m + j\beta_m))(z - e^{-a\omega T} (\alpha_m - j\beta_m)) = 0$

Comparing the coefficients of the observer characteristic equation with that of the desired characteristic equation, the feedback gain vector L is obtained. Here ‘a’ decides the observer pole location in the z-plane. The structure of the composite observer is shown in Figure 2. The nth block of this observer is presented in Figure 3. The equal magnitude quadrature component is obtained by multiplying the quadrature signal with a gain $g_n = \frac{(\alpha_n - 1)}{\beta_n}$.

Let G₀, G₁, G₂,.....G_m be the transfer function of individual blocks in the composite observer. Hence, the transfer function of the fundamental block in case of simple and composite observer are $\frac{G_1(z)}{1+G_1(z)}$ and $\frac{G_1(z)}{1 + \sum_{n=0,1,\dots}^m G_n(z)}$ respectively. The mapping of poles in z-plane for the

composite observer and the magnitude response of the fundamental block in the composite observer designed for 50Hz with the pole location corresponding to ‘a’ = 0.2 and 1 are shown in Figure 4 and Figure 5 respectively. Magnitude response shows that the fundamental block in the parallel structure accepts fundamental frequency and rejects all other harmonic frequencies. Also as the poles move far interior to the unit circle the band width decreases, resulting in sharper tuning.

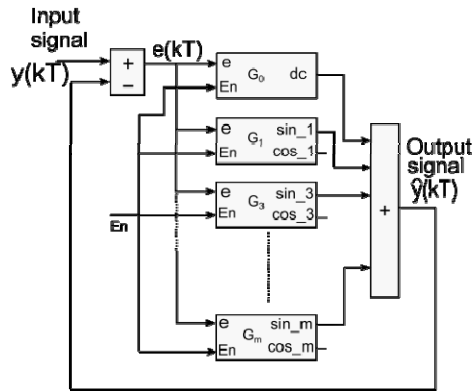


Figure 2. Structure of composite observer

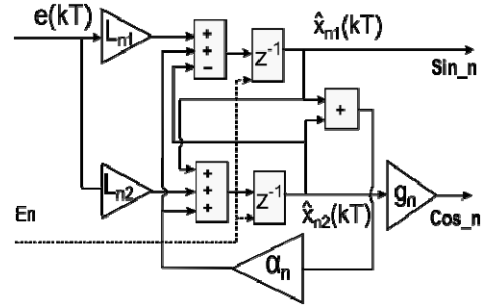


Figure 3. Structure of nth block in the composite observer

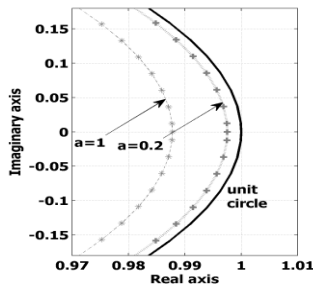


Figure 4. Poles of composite observer in z-plane corresponding to 'a' = 0.2 and 1

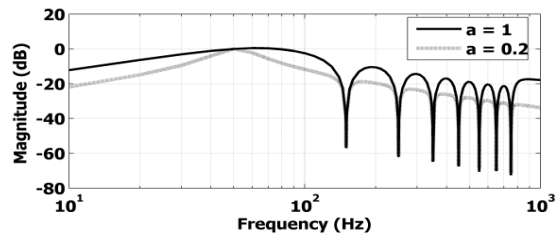


Figure 5. Magnitude plot of the fundamental block in the composite observer for the pole locations corresponding to 'a' = 0.2 and 1

2.2. Sampling Generator

The NCO is used as the sampling generator to create enabling pulses for the composite observer and to generate the address bits for the look up table to produce unit sine and cosine signals as shown in Figure 1. The frequency of the output signal generated by the NCO is an integer multiple of frequency of the input signal. This property makes it suitable for variable sampling schemes. The structure of NCO generating sample pulses is shown in Figure 6. Here, NCO is derived from a standard coupled oscillator [21-22]. The state space model of the NCO with automatic gain control is:

$$\begin{bmatrix} x_1((k+1)T_0) \\ x_2((k+1)T_0) \end{bmatrix} = G_{NCO} \begin{bmatrix} 1 - \frac{\beta_o^2}{2} & \beta_o \\ -\beta_o & 1 - \frac{\beta_o^2}{2} \end{bmatrix} \begin{bmatrix} x_1(kT_0) \\ x_2(kT_0) \end{bmatrix} \tag{2}$$

where $G_{NCO} = \frac{3}{2} - (x_1^2(kT_0) + x_2^2(kT_0))$ (3)

$$\beta_o = \sin(\omega_o T_0) \tag{4}$$

where, $\omega_o = 2\pi f_o$ and $T_0 = \frac{1}{f_{NCO}}$

f_{NCO} – the enabling frequency of the NCO (=5MHz),
 f_o , oscillator output frequency = N.f
 f, input signal frequency,
 x_1 and x_2 are the state variables.

When the input signal frequency is $\omega + \Delta\omega$, the input to the oscillator or the controller output changes to $\sin((\omega_0 + \Delta\omega_0)T_0)$ so as to generate N (512) times the input signal frequency. Hence,

$$\beta_0 + \Delta\beta_0 = \sin((\omega_0 + \Delta\omega_0)T_0) \tag{5}$$

The variation of $\Delta\beta_0$ with respect to Δf is linear. From (5), it is clear that under drift in frequency, a correction need to be provided at the output of the controller. This correction factor (K_{cor}) [21] is calculated on the assumption that as $\Delta\omega_0 \rightarrow 0$, $\cos(\Delta\omega_0 T_0) \rightarrow 0$, $\sin(\Delta\omega_0 T_0) \rightarrow \Delta\omega_0 T_0$.

Hence (5) becomes, $\Delta\beta_0 \approx \Delta\omega_0 T_0 \cdot \cos(\omega_0 T_0) \approx (\Delta\omega T) \left(\frac{N}{T}\right) (T_0) (\cos(\omega_0 T_0))$

$$\Delta\beta_0 \approx K_{cor} (\Delta\omega T) \tag{6}$$

From (6), correction factor is obtained as

$$K_{cor} = \left(\frac{NT_0}{T}\right) (\cos(\omega_0 T_0)) \tag{7}$$

where, T is the sampling period.

The PI controller output consists of both phase and frequency information. ($f + \Delta f$) is deduced from the integral part of the controller as shown in Figure 6, which contains the frequency information. As the frequency information is a sinusoidal quantity, the frequency is calculated using inverse sine function.

Here, $y = \beta_0 + \Delta\beta_0 = \sin((\omega_0 + \Delta\omega_0)T_0)$ (8)

Hence, $f + \Delta f = \frac{1}{2\pi NT_0} \left(y + \frac{y^3}{6}\right)$ (9)

The first two terms of inverse sine series is considered in (9) and this calculates the frequency with an accuracy of $\pm 0.02\text{mHz}$ for a range of 40Hz to 70Hz.

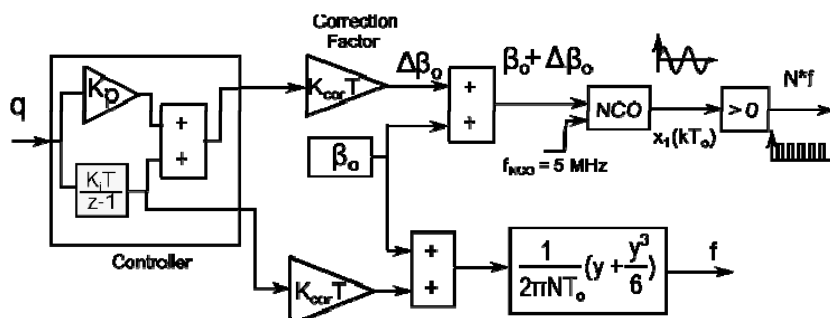


Figure 6. NCO based sample pulse generation

3. Transfer Function Model

This section deals with the analysis of the proposed PLL by deducing the transfer function model in continuous time with two different estimators-simple observer and composite observer. A step change in phase is given to these models and the time response of these PLLs is studied. Symmetrical optimum procedure [10] is used to design the controller of PLL.

3.1. Simple Observer as an Estimator

The observer is modelled as a first order system with time constant $\tau_{obs} = \frac{1}{a\omega}$. The transfer function model of the observer based variable sampling PLL is shown in Figure 7. The simulation study of this model is done for a time constant $\tau_{obs} = \frac{1}{2\pi \times 50}$. Figure 8 shows the phase error vs time for the PLL and the transfer function model for three different values of phase margins such as 30°, 45° and 60° respectively.

The transfer function model is derived based on the assumption that ω is constant. When the step change in phase angle is given to both the transfer function model and the PLL, initial transient in frequency deviates from the nominal value and it is proportional to the controller gains. The controller gains are higher with lower phase margin (PM) and hence more deviation is seen in the response of the PLL compared to the model as shown in Figure 8.

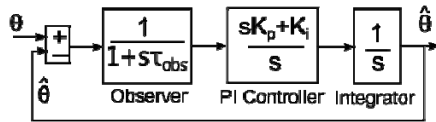


Figure 7. Transfer function model of an observer based SRF-PLL

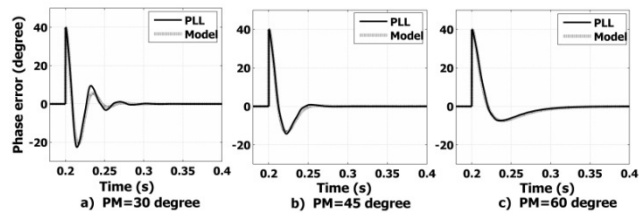


Figure 8. Simulation results when a step change in phase of 40° is applied to transfer function model and the PLL (a) PM=30° (b) PM=45° (c) PM=60°

3.2. Composite Observer as an Estimator

When DC and harmonic components are present along with the fundamental block, composite observer is approximated as a first order system having time constant given by:

$$\tau_{obs} = \frac{1 + aH}{a\omega}; \text{ where } H = H_{dc} + \sum_{m=3}^{m=N} \frac{1}{m}; H_{dc} = 0.5 \tag{10}$$

The response of the variable sampling PLL and the transfer function model are illustrated in Figure 9 for a phase change of 40°. The controller is designed using symmetrical optimum procedure. The proportional integral (PI) coefficients have been evaluated for different phase margins (30°, 45° and 60°). Here, the model closely follows the system. Composite observer based PLL gives a sluggish response compared to the simple observer because of the presence of DC and harmonics blocks along with the fundamental.

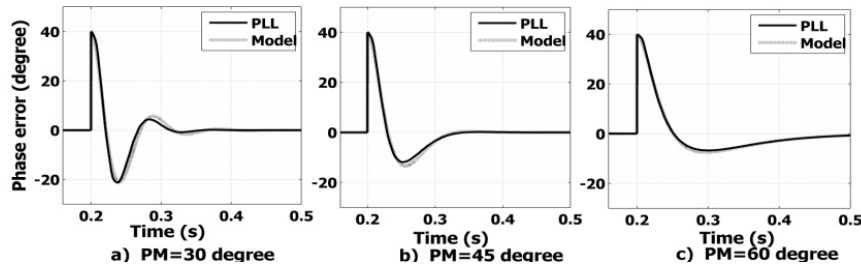


Figure 9. Simulation results when a step change in phase of 40° is applied to transfer function model and variable sampling PLL. (a) PM=30° (b) PM=45° (c) PM=60°

4. Results and Discussion

The composite observer based variable sampling PLL is simulated using MATLAB Simulink and the results are verified experimentally by implementing the same using DSP Builder tool in Altera Cyclone IV FPGA. A simple observer as well as a composite observer with closed loop poles located at $z = e^{-a\omega T}$ in z-domain with 'a'=1 are used as estimators in the PLL for a digitally synthesized harmonic rich input signal as well as for a real time grid voltage of slowly drifting frequency.

4.1. Performance of Simple Observer Based PLL

Initially a sinusoidal signal of magnitude unity at 50Hz is given to this PLL. At 0.2s, a DC offset of 10% is introduced to the sinusoidal input signal. Then at 0.3s, the input signal is switched suddenly to a harmonic rich signal of THD 45% having odd harmonics upto 15th at 50Hz. Figure 10 represents simulation result of estimated V_d, drift in frequency and phase error of this PLL. With a sinusoidal input signal, simple observer estimates parameters without any error. But for a harmonic rich input signal, ripple is seen in the estimated values, inferring that noise creeps into the system. The increase of filtering capability by moving poles closer to origin in z-plane will make the response more sluggish. Another fact is that the simple observer is estimating only fundamental orthogonal components and hence, for a harmonic rich input signal this PLL fail to estimate the parameters efficiently. This necessitates the requirement of estimating DC and individual harmonic components, which is possible through a composite observer. For the same pole location, here as the filtering capability is increased-because of the paralleling of simple observer blocks, modelled for all the harmonics in the input signal-the estimated parameters are converging to the desired value as shown in the transient responses under subsection 4.2. With the sinusoidal input the PLL estimates magnitude, frequency and phase exactly whereas with a 10% DC offset, the estimation goes oscillating about a mean value. When a harmonic rich signal is fed, the PLL gives more oscillatory response for magnitude and frequency. The DC offset has more deteriorating effect on estimation of phase than with harmonics for this simple observer based PLL. Here the controller gains are chosen as $K_p=130$ and $K_i=7014$.

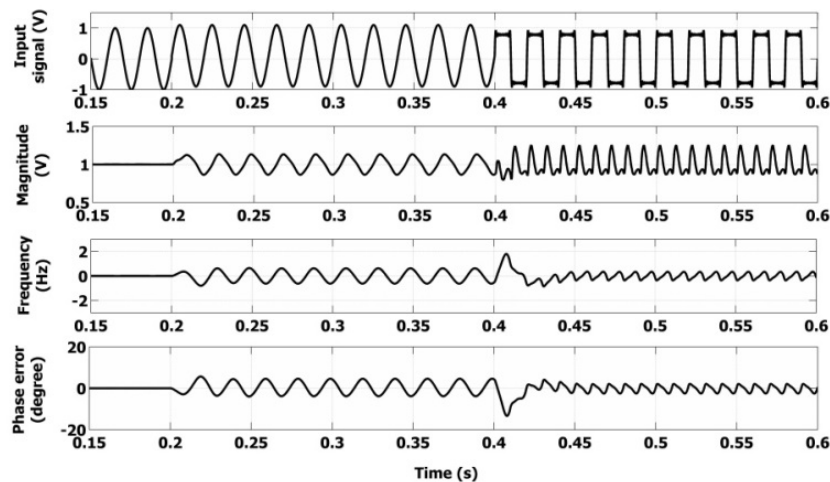


Figure 10. Simulation response of estimated V_d, drift in frequency and phase error when sinusoidal and a harmonic rich signal are applied to the simple observer based PLL

4.2. Performance of Composite Observer Based PLL

In the following subsections the performance of the PLL using the composite observer as estimator is studied by giving a step change in amplitude, frequency and phase of the input signal. The controller gains are chosen as $K_p=100$ and $K_i=3500$. The experimental results are coincident with the simulation results.

4.2.1. Step Change in Amplitude

A 40% sag in the harmonic rich input signal (odd harmonics upto 15th) is produced at 0.2s and restored after 0.4s. Figure 11 (a) and (b) illustrates the response of the variable sampling PLL through simulation and experiment respectively. When the amplitude of signal is changed the PLL estimates the magnitude of V_d within a cycle, frequency overshoot is 0.25Hz and peak phase error is about 3.5°. This estimation speed is achieved with the inclusion of DC as well as harmonics by the estimator. Under steady state all the parameters are confined to the desired value, which is clear from both the simulation and experimental results shown in Figure 11.

4.2.2. Step Change in Frequency

For the same harmonic rich input signal with frequency 47.5Hz is fed to the PLL and suddenly changed to 52.5Hz at 0.2s and restored to 47.5Hz after 0.4s. Figure 12 (a) and (b) shows the input signal, direct axis voltage, drift frequency and phase error through simulation and experiment. These results reveal that the PLL is estimating the frequency in 2.5 cycles and peak phase deviation of 19.5° for +5Hz stepchange. For a step change of -5Hz the frequency is estimated in 3.3 cycles and the maximum phase error is about 20.5°. Also a smoother transient can be seen in the results with step disturbance for simulation and experiment. Steady state values are converging to the desired values.

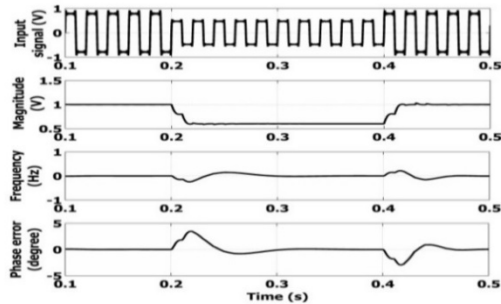


Figure 11(a). Simulation response of PLL on estimation of V_d , drift frequency and phase error with 40% sag at 0.2s and reinstated at 0.4s

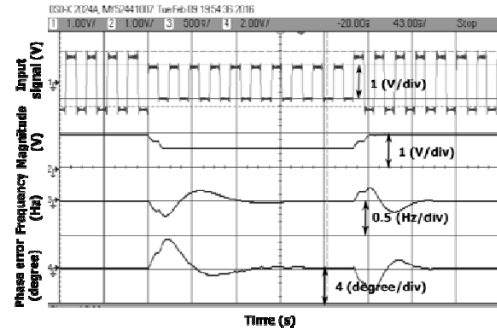


Figure 11(b). Simulation response of PLL on estimation of V_d , drift frequency and phase error with 40% sag at 0.2s and reinstated at 0.4s

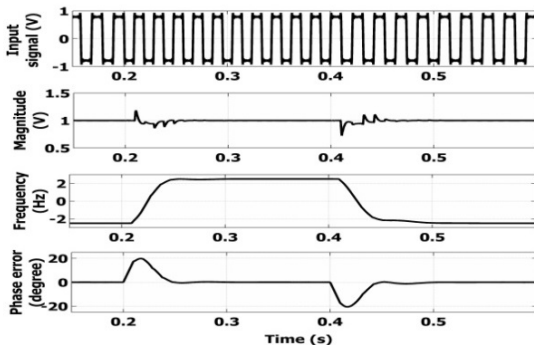


Figure 12(a). Simulation response of PLL on estimation of V_d , drift frequency and phase error for step change in frequency from 47.5Hz to 52.5Hz at 0.2s and reinstated after 0.4s

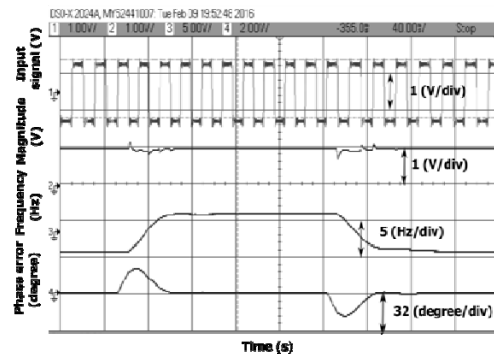


Figure 12(b). Simulation response of PLL on estimation of V_d , drift frequency and phase error for step change in frequency from 47.5Hz to 52.5Hz at 0.2s and reinstated after 0.4s

The frequency of this harmonic rich signal is varied in steps of 10Hz from 40Hz to 70Hz and the estimated parameters are observed. Figure 13 illustrates the PLL designed for 50Hz is working efficiently over a wide range of frequency. Hence, this scheme could be used for any standard grid frequency.

4.2.3. Step Change in Phase Angle

A step change in phase of 40° is given to this harmonic rich input signal at 50Hz and the PLL is evaluated through simulation and experiment. The results for estimated V_d , drift in frequency and phase error are shown in Figure 14 (a) and (b). The estimation of phase angle occurs in 2.83 cycles. The peak phase overshoot is about 18.95° and peak frequency deviation is 4.25Hz.

4.2.4. DC Offset

A DC offset of 0.5V is given to this harmonic rich input signal at 50Hz and the simulation and experimental responses of the PLL for estimated V_d , drift in frequency and phase error are shown in Figure 15 (a) and (b) respectively. There is no error in phase and frequency estimated by this PLL under steady state.

4.3. Effect of Unmodelled Harmonics

A similar harmonic rich signal containing odd harmonics upto 25^{th} with THD = 45.22% is fed to a composite observer modelled with DC and odd harmonics upto 15^{th} . The unmodelled harmonics (THD = 4.47%) present in the signal are 17^{th} , 19^{th} , 21^{st} , 23^{rd} and 25^{th} of 2% each. The estimated parameters by the PLL under steady state is shown in Table 2 for two different pole locations of the observer with 'a' = 0.5 and 1. The results show that as 'a' reduces, the accuracy of the estimated parameters increases. This occurs with a compromise on speed of estimation.

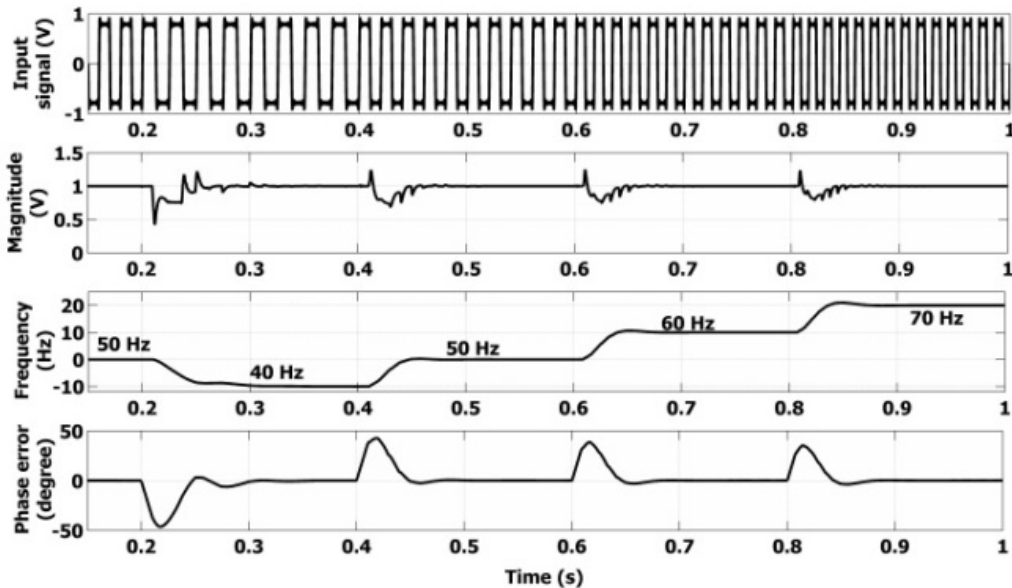


Figure 13. Simulation response of PLL on estimation of V_d , drift frequency and phase error for frequency change in steps of 10Hz from 40Hz to 70Hz

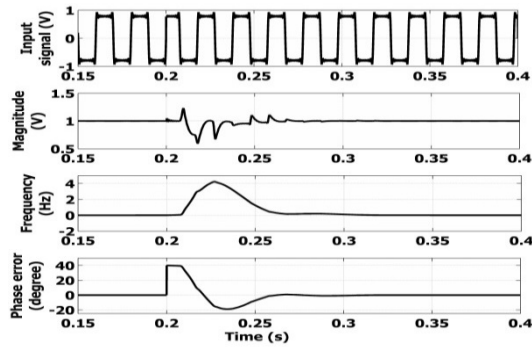


Figure 14(a). Simulation response of PLL on estimation of V_d , drift in frequency and phase error when a step change in phase angle of 40° occurs at $t=0.2s$

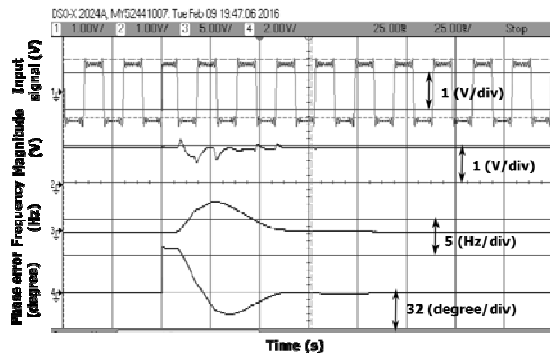


Figure 14(b). Simulation response of PLL on estimation of V_d , drift in frequency and phase error when a step change in phase angle of 40° occurs at $t=0.2s$

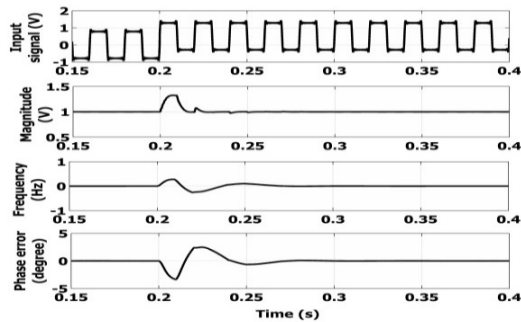


Figure 15(a). Simulation response of PLL on estimation of V_d , drift in frequency and phase error when a harmonic rich signal is applied to composite observer based PLL for DC offset of $0.5V$

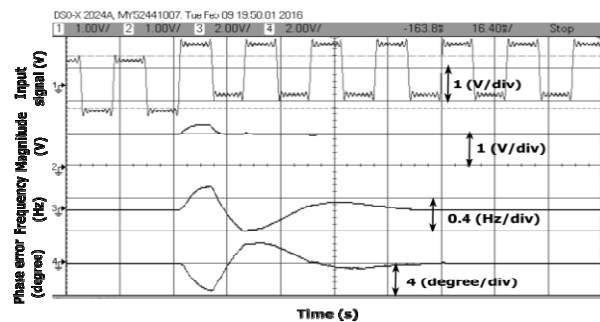


Figure 15(b). Simulation response of PLL on estimation of V_d , drift in frequency and phase error when a harmonic rich signal is applied to composite observer based PLL for DC offset of $0.5V$

Table 2. Error in Estimated Parameters of Composite Observer Based PLL in Presence of Unmodelled Harmonics

	Pole location with 'a'= 0.5	Pole location with 'a' = 1
Peak Phase Error	0.006°	0.015°
Peak Frequency Error	0.446mHz	1mHz
Magnitude Error	0.33%	1.5%

4.4. Performance of the PLL with a Slowly Drifting Frequency

The voltage across a rectifier type capacitive nonlinear load ($36\Omega \parallel 2200\mu F$) when connected to a grid of reduced voltage $90V_{p-p}$ through a $4mH$ inductor is used to validate the performance of the PLL. The third harmonic component is predominant (3.4%) along with DC (0.7%) and fundamental (100%) in this grid voltage having THD of 3.9%. The estimated magnitude, frequency and phase of the grid voltage with a simple observer and composite observer based PLL are shown in Figure 16 (a) and (b) respectively. When the actual grid frequency is drifting slowly from 50Hz, the estimated frequency from the simple observer based PLL is found to have ripples and estimated frequency by the composite observer modelled with $m=0, 1$ and 3 in the PLL is $50.04Hz$. As the PLL is used to estimate the frequency by measuring voltage from the grid, this estimator could be modelled with the required number of blocks.

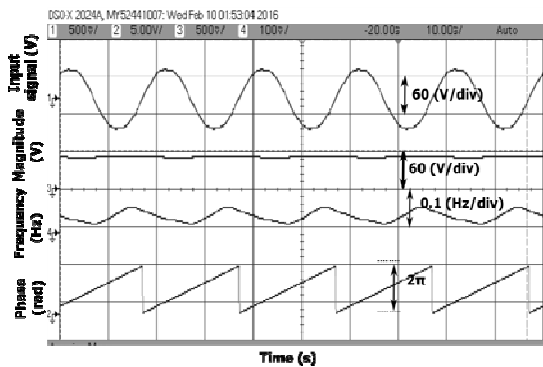


Figure 16(a). Experimental results of estimated voltage, frequency and when a real time grid voltage signal is applied to the simple observer based PLL

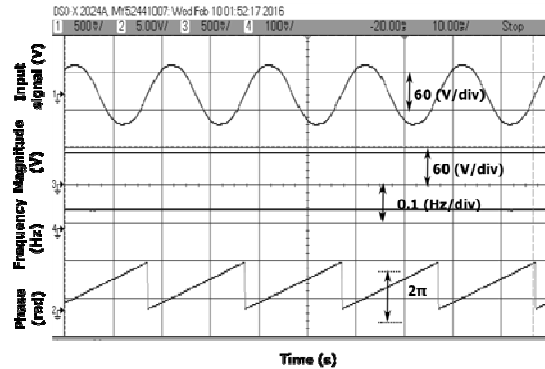


Figure 16(b). Experimental results of estimated voltage, frequency and when a real time grid voltage signal is applied to the composite observer based PLL

5. Conclusion

In this paper a variable sampling period composite observer based PLL, estimating the parameter efficiently is discussed. The composite observer helps in choosing required number of harmonic blocks depending upon the harmonics present in the input signal. On-line estimation of the individual harmonic components can be estimated by this scheme. The transfer function model of the composite observer derived helps in analysing the scheme and tuning of the controller. The performance of this PLL in estimating the parameters is proved through the simulation and experimental studies by providing step change in magnitude, frequency, phase and DC offset in presence of harmonics. This PLL is working efficiently for wide range of frequency 40-70Hz. The effect of unmodelled harmonics with respect to pole location of the estimator is studied and is found to be very minimal for a sharper tuning, with a compromise on transient time. As this PLL is used to synchronize with the grid frequency, grid voltage is used to validate the scheme and is found that only DC, fundamental and third harmonic block are required for estimation. As the scheme maintains constant number of samples per cycle for a drifting frequency, makes it suitable for power quality studies.

References

- [1] JM Carrasco et al. Power-Electronic Systems for the Grid Integration of Renewable Energy Sources: A Survey. *IEEE Transactions on Industrial Electronics*. 2006; 53(4): 1002-1016.
- [2] Rajesh Damaraju, SVN Lalitha. A Fuzzy Controller for Compensation of Voltage Sag/Swell Problems Using Reduced Rating Dynamic Voltage Restorer. *TELKOMNIKA Indonesian Journal of Electrical Engineering*. 2015; 15(3): 407-414.
- [3] C Prakash, N Suparna. Design and Simulation of Phase-Locked Loop Controller Based Unified Power Quality Conditioner Using Nonlinear Loads. *International Journal of Power Electronics and Drive System*. 2012; 2(4): 417-423.
- [4] Guan-Chyun Hsieh, Hung JC. Phase Locked Loop Techniques. A Survey. *IEEE Transactions on Industrial Electronics*. 1996; 43(6): 609-615.
- [5] Timothy Thacker, Ruxi Wang, Dong Dong, Rolando Burgos, Fred Wang, Dushan Boroyevich. *Phase-Locked Loops using state variable feedback for single-phase converter systems*. Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition, Washington, DC. 2009: 864-870.
- [6] SM Silva, BM Lopes, BJC Filho, RP Campana, and WC Boaventura. *Performance evaluation of PLL algorithms for single phase grid-connected systems*. 39th Annual Meeting IEEE IAS World Conference on Industrial Applications of Electrical Energy. 2004; 4: 2259-2263.
- [7] Golestan S, Guerrero JM, Vidal A, Yepes AG, Doval-Gandoy J, Freijedo FD. Small-Signal Modeling, Stability Analysis and Design Optimization of Single-Phase Delay-Based PLLs. *IEEE Transactions on Power Electronics*. 2016; 31(5): 3517-3527.
- [8] Ciobotaru M, Teodorescu R, Blaabjerg F. *A new single phase PLL structure based on second order generalized integrator*. 37th IEEE Power Electronics Specialists Conference. 2006: Jeju, 1-6.

- [9] Teodorescu R, Blaabjerg F, Liserre M, Loh PC. Proportional-resonant Controllers and Filters for Grid-connected Voltage-source Converters. *IEE Proceedings Electric Power Applications*. 2006; 153(5): 750-762.
- [10] Saeed Golestan, Mohammad Monared, Francisco D Freijedo, Josep M Guerrero. Dynamics Assessment of Advanced Single -Phase PLL Structures. *IEEE Transactions on Industrial Electronics*. 2013; 60(6): 321-330.
- [11] Santos Filho RM, Seixas PF, Cortizo PC, Torres LAB, Souza AF. Comparison of Three Single-Phase PLL Algorithms for UPS Applications. *IEEE Transactions on Industrial Electronics*. 2008; 55(8): 2923-2932.
- [12] Subramanian C, Kanagaraj R. Single-Phase Grid Voltage Attributes Tracking for the Control of Grid Power Converters. *IEEE Journal of Emerging and Selected Topics in Power Electronics*. 2014; 2(4): 1041-1048.
- [13] De Brabandere K, Loix T, Engelen K, Bolsens B, Van den Keybus J, Driesen J, Belmans R. *Design and operation of a phase-locked loop with Kalman estimator-based filter for single-phase applications*. 32nd IEEE Annual Conference on Industrial Electronics, Paris. 2006: 525-530.
- [14] M Karimi-Ghartemani and MR Iravani. A Method for Synchronization of Power Electronic Converters in Polluted and Variable-frequency Environments. *IEEE Transactions on Power Systems*. 2004; 19(3): 1263-1270.
- [15] Karimi-Ghartemani M. A Unifying Approach to Single-Phase Synchronous Reference Frame PLLs. *IEEE Transactions on Power Electronics*. 2013; 28(10): 4550-4556.
- [16] Karimi-Ghartemani M, Khajehoddin SA, Jain PK, Bakhshai A, Mojiri M. Addressing DC Component in PLL and Notch Filter Algorithms. *IEEE Transactions on Power Electronics*. 2012; 27(1): 78-86.
- [17] Karimi-Ghartemani M, Khajehoddin SA, Jain PK, Bakhshai A. Derivation and Design of In-Loop Filters in Phase-Locked Loop Systems. *IEEE Transactions on Instrumentation and Measurement*. 2012; 61(4): 930-940.
- [18] Karimi-Ghartemani M. A Distortion-free Phase-locked Loop System for FACTS and Power Electronic Controllers. *Electric Power Research*. 2007; 77(8): 1095-1100.
- [19] Carugati I, Maestri S, Donato PG, Carrica D, Benedetti M. Frequency Adaptive PLL for Polluted Single-Phase Grids. *IEEE Transactions on Power Electronics*. 2012; 27(5): 2396-2404.
- [20] Orallo CM, Carugati I, Maestri S, Donato PG, Carrica D, Benedetti M. Harmonics Measurement With a Modulated Sliding Discrete Fourier Transform Algorithm. *IEEE Transactions on Instrumentation and Measurement*. 2014; 63(4): 781-793.
- [21] K Arun, K Selvajothi. Cascaded Delayed Signal Cancellation Based Variable Sampling SRF PLL. *Mediterranean Journal of Measurement and Control*. 2016; 12(1): 511-520.
- [22] C Turner. Recursive Discrete Time Sinusoidal Oscillators. *IEEE Signal Processing Magazine*. 2003; 20: 103-111.
- [23] Rodriguez P, Luna A, Candela I, Mujal R, Teodorescu R, Blaabjerg F. Multiresonant Frequency-Locked Loop for Grid Synchronization of Power Converters Under Distorted Grid Conditions". *IEEE Transactions on Industrial Electronics*. 2011; 58(1): 127-138.
- [24] Mojiri M, Karimi-Ghartemani M, Bakhshai A. Time-Domain Signal Analysis Using Adaptive Notch Filter. *IEEE Transactions on Signal Processing*. 2007; 55(1): 85-93.
- [25] Girgis AA, Chang WB, Makram EB. A Digital Recursive Measurement Scheme for Online Tracking of Power System Harmonics. *IEEE Transactions on Power Delivery*. 1991; 6(3): 1153-1160.
- [26] K Selvajothi and PA Janakiraman. Extraction of Harmonics using Composite Observer. *IEEE Transactions on Power Delivery*. 2008; 23(1): 31-40.