TELKOMNIKA Indonesian Journal of Electrical Engineering
Vol.12, No.2, February 2014, pp. 1333 ~ 1342
DOI: http://dx.doi.org/10.11591/telkomnika.v12i2.3210

Self-adapting Radar Video Echo Acquisition System based on LZW Algorithm

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Abstract

This paper presents a high-speed low-complexity Field Program Gate Array (FPGA) design and implementation of the lossless Lempel-Ziv-Welch (LZW) algorithm on Xilinx Virtex-E device family for self-adapting Radar video echo data acquisition Applications. A multi-channel self-adaptive variable sampling rate data acquisition system based on FPGA and I2C bus is introduced. By writing the frame data into E2PROM and design the interface between FPGA and E2PROM, multi-channel data programmable sampling ratio is realized. Because the radar echo samples contain abundant phase information and details of the image data, phase relation of the original image must be maintained. So it will not affect the reconstruction image information in data compression process. In order to ensure the accuracy of imaging data of radar echo data, acquisition system adapts lossless compression algorithm LZW based on FPGA. The algorithm principle of LZW and the coding flow are introduced. By comparing with the compression ratio in different encoding unit, 12bit encoding width is appropriate. Simulation results show that the LZW algorithm has better compression ratio for echo text data.

Keywords: *LZW, self-adapting data acquisition, FPGA, data compression*

1. Introduction

Radar video echo data acquisition system has already been widely used in such fields such as communication, radar tracking technology used in missile guidance and remote sensing. In order to obtain the target distance and velocity etc, serial receiving target echo signal is needed [1-3]. With the increasing resolution of radar images, it is becoming more and more important to find an efficient way to store the high volume of sampling data at real-time or to compress data with higher compression performances for limited bandwidth of communication channel [4].

In order to improve the precision of measurement and real-time tracking target, multi-channel echo signals of radar target echo data and multi-operation of FFT are needed in a relatively long measuring period (such as100ms) for the real radar system. FFT frequency and FFT counts are required to be altered in one measuring period.

For the sake of avoiding spectrum aliasing after sampling, the acquisition frequency of radar system will be larger than twice as the highest possible signal frequency. As the echo signal frequency of the target changed, it is required more memory to store large redundancy data according to fixed originally high-frequency acquisition. On the contrary, low-frequency acquisition will lead to data waveform distortion [5]. Usually, there are two methods to change the acquisition frequency: one is adjusting sampling interval directly, the other is to adopting self-adapting sampling mode [6]. The former is to adopt variable cutoff frequency analog filter in the front of sampling circuit, the latter is to determine sampling rate of each channel based on the highest frequency of each channel sampling parameters and change sampling frame data by program.

In order to acquire valid data as much as possible, solving the conflict between the high-speed data acquisition and large volume storage is necessary in radar video echo data acquisition circuit design. So the data compression is an effective way to solving the above problem. A data acquisition (DAQ) system is proposed to deal with issues inherent in arctangent

Received May 16, 2013; Revised August 26, 2013; Accepted September 16, 2013

demodulation of a quadrature radar signal, but the data storage strategies of sampling data is not introduced in [7]. In [8] an efficient data acquisition and SAR processing system based on a modified discrete Fourier Transform algorithm is proposed, which requires lesser system's computational load. Owing to the sensitive radar video echo signal, we usually records data firstly and then do data forensics, analysis, so we can only adopt real-time lossless compression algorithm. So, it is required that radar video echo data acquisition and processing system has good real-time performance. While pursuing the measurement accuracy of target, we must reduce the complexity of signal processing algorithms at the same time.

At present there are many compression and decompression methods based on the software, which are post processing of the data. Not only this method reduces the execution speed, but consumes a large amount of CPU resources. Using hardware design to achieve real-time data lossless compression can change high speed signal into slowly varying signals. It can decrease the channel capacity of communication and improve the reliability of data. So in radar video echo signal acquisition system, aiming to achieve the effective data transmission, increase the system bus data transmission rate and expand the system data storage capacity, the hardware implementation of real-time data lossless compression can only be used.

2. Data Compression Algorithm Comparision

In order to improve the accuracy and real-time data transmission speed within the limited data transportation bandwidth, it is important to study the lossless real-time data compression technique. According to whether the data can be absolutely reproduced, data compression is divided into lossy compression and lossless data compression technology [9]. Lossy compression method is appropriate for the information which is less sensitive to some certain frequency signal components such as voice, image. And it is allowed some information losing during compression. Lossy compression algorithm mainly includes the predictive encoding, multi-solution encoding and graphics encoding. Lossless compression algorithm mainly includes Huffman encoding, arithmetic encoding, run-length encoding [10], LZ encoding and so on [11]. Among them, Huffman encoding and arithmetic encoding methods which based on the probability of occurrence of source data are encoded. There are two treating processes in coding, which are statistical processing and data encoding, so the speed of data processing and real-time performance is not good. Better compression result of run-length encoding can be achieved if more than 4 times the characters appear continuously, so this method is not suitable for radar echo signal compression. The LZ encoding method based on the dictionary model, in which no requirement for data block break it is using a single word instead of string, inputting signal by data stream format. This method has good real-time performance and complete reversible decompression. LZ coding Algorithm includes LZ77, LZ78 and LZW [12-13]. According to the compression design request of radar echo data, this paper adapts LZW lossless compression algorithm.

3. Hardware Principle Design

The radar video echo data acquisition system introduced in this paper can collect 16 channels analog signals simultaneously, which are processed by 16 channels electromagnetism interference isolation circuits, amplifications, 16 channels following circuits, active low-pass filters and a high-speed analog switches. At last, analog signals flow into the high-speed ADC, and output signal are 16-bits digital codes. Sampling control logic (FPGA) of sampling processing module is utilized to implement the buffering and processing function. The control logic writes compressed data into the storage array of data store module through high-speed system bus [14]. Block diagram is shown in Figure 1.

3.1. Self-adapting Acquisition Design

In this design, multi-channel programmable acquisition system is realized based on the design of interface circuit between I2C bus and FPGA. I2C bus which is a kind of serial transmission bus among chips composed of serial clock signal SCL and serial data signal can realize full duplex data transmission.

The storage circuit is composed of I2C bus and AT24C64 accord with I2C bus specification which belongs to E2PROM. This method's merits are simple design, long term

data storage and stable operation. Configure the hardware circuit to realize programmable sampling rate, as the schematic diagram Figure 2.

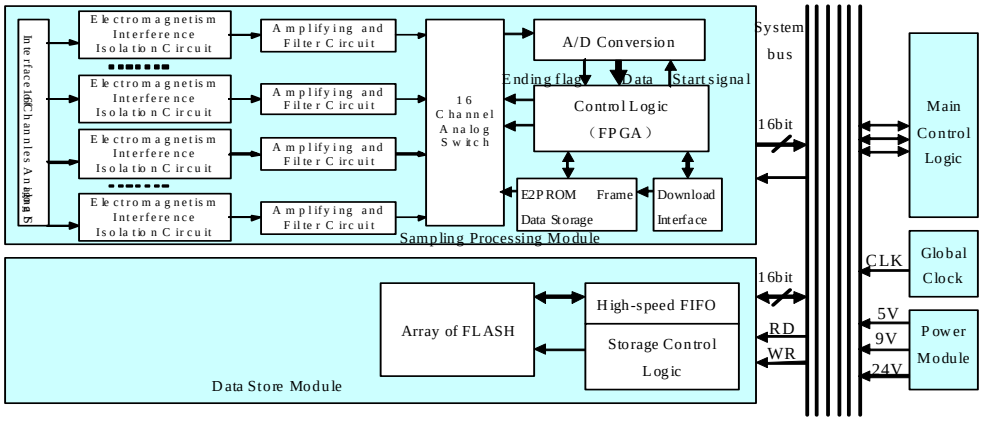

Figure 1. Hardware Principle Block Diagram of Hardware

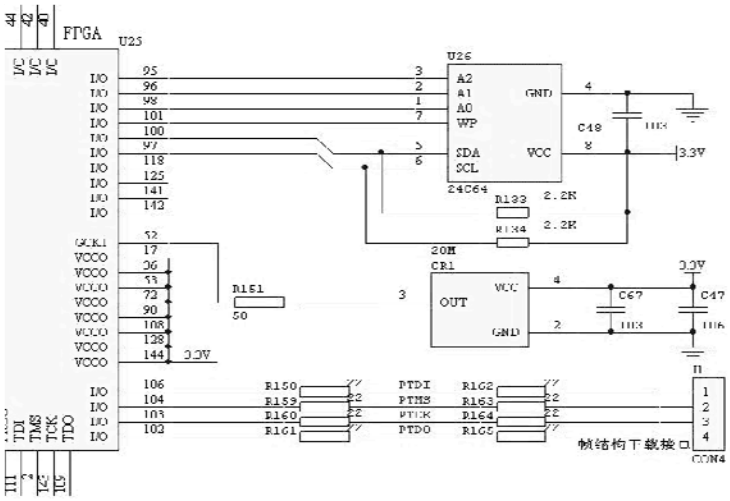

Figure 2. Schematic Diagram of Configuration Hardware

SDA and SCL are all bidirectional transmission signals which are joined by positive polarity of power supply. The chip address signal is produced by address input signal A0, A1, A2 which are connected to FPGA. The clock signal is transmitted to SCL, and control signal such as addressing, start and stop are transmitted on SDA time-sharing.

3.2. Working Mode of Programmable Sampling

The implementation procedure of programmable sampling rate: when the system powered on, judge the current state firstly. The state flag S_PROM='0' shows programming state, otherwise is sampling state. Secondly, according to the demand the user takes turns in downloading the sampling channel data to E2PROM through frame data interface. Then center control logic reads channel configuration data off the frame data storage into frame format FIFO integrated in FPGA. Set the sampling channel and then start ADC. After conversation, write the data to high-speed buffer integrated in FPGA and then read out the next sampling channel data from frame format FIFO, and so on. After finishing 64 channel analog signal conversation once insert frame flag"EB90", and then do the next loop operation until complement all the data conversation, and insert ending flag at last. Thus foundation of programmable sampling rate is completed. The control flow chat is shown as Figure 3.

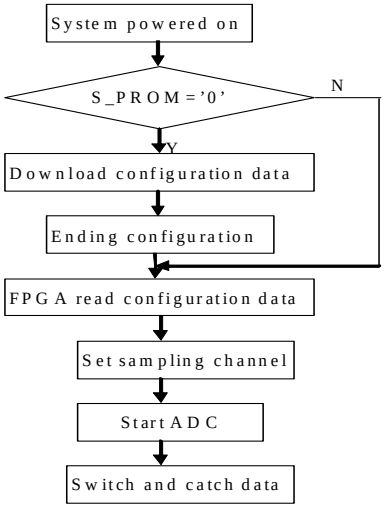

Figure 3. Programmable Sampling Rate Control Flow Chart

3.3. The Timing Design of Programmable Sampling

When connect the parallel port cable with the interface of frame format, the state flag signal S_PROM will ground (S_PROM='0'). Then the system is in program state. As programming, the computer sends synchronization frame signal PZTB, coding synchronization signal ZTB, clock signal PCLK and frame data PDATA[7..0]. After receiving program order from the PC, the controller reads the configuration data into E2PROM frame storage. Part of timing is shown in Figure 4.

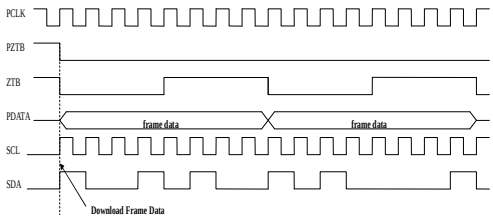

Figure 4. Program Timing Diagram of Frame Structure

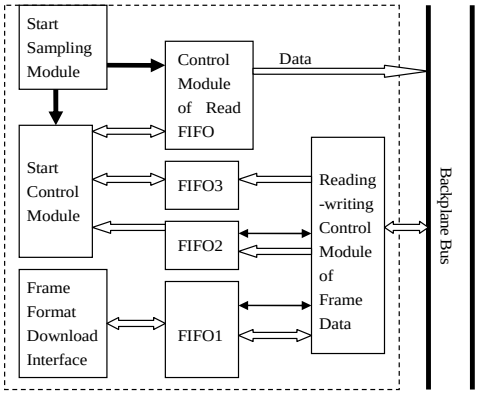

Figure 5. Self-adapting acquisition schematic diagram of programmable sampling and FIFO

As shown in Figure 5, frame format data D[7..0] is written to frame format download module beforehand through data signal PTDI, clock signal PTCLK, state signal PTMS and feedback signal PTDO. Then FIFO1 reads out the information and stores them to frame data read-write control module. After system powered on, FPGA writes all information into FIFO2 actively and then sampling module controls channel switching of analog switching group by above information. So, the sampling rate can be programmable. In consideration of limitation of the E2PROM reading and writing rate and improve the switching speed, every time the system powered on, firstly read out frame data from E2PROM and store to high-speed FIFO integrated in FPGA, then after starting sampling, system directly readout the configuration data to control the channel switch.

Frame format data is based on the unit of byte. 4 bits channel address decode signal A3-A0 expressed by low 4 bit of frame data D[7..0], the fifth and sixth bits of frame data is to select 4 analog switches, and the high two bits is flag bits. D7D6=”10” expresses the last byte of configuration, that is to say, the current sampling channel is the last one in this circle sampling and clear the channel switch counter. If D7D6=”00” expresses sampling operation is continuing.

According to different application environment, users can adopt more high-speed AD converter and confirm sampling rate of each channel according to total sampling rate and frame data user-defined. If the total sampling rate is 400Mbps for 16 channel signal, sampling rate is 25Mbps for each channel. If for 4 channel signal, each channel sampling rate can reach 100Mbps. So, the system achieves programmable sampling rate for each channel on the basis of total sampling rate fixed.

4. LZW Algorithm Design Based on FPGA

4.1. LZW Data Compression Algorithm

Because compression ratio of real-time LZW data compression algorithm is high, it can be used to achieve adaptive compression of different data streams. Especially for some data stream which changes slowly and comes up repeatedly. With the increases of the volume of data, the compression efficiency can be better. LZW algorithm has three important objects: the input data stream, output stream and a string table used to encode [15]. Where the input data stream represents compressed data; output coding stream represents compressed output stream; after compression the string table stores the index number. Only the index number of the first data block can be output for the same data block.

The principle of LZW compression algorithm is to build a string table. The input string is mapped to a constant output code. Usually code length is set to 12bit, 15bit or 18bit. String table has "prefix ". It is assumed that a new string of PS consists of any string P and a character S. If the PS has existed in the string table, S is the extension P, and P is the prefix of S [16]. The string table is dynamically generated, which must be initialized before encoding to make it contain all of the single character string. In the process of compression, a new character string of compression information can be created continuously. The prefix of PS and the opposite words should be stored in saving the new character string at the same time. In the process of decompression, the decoder can recover the same string table in accordance with the encoding.

4.2. FPGA Modularization Design

FPGA has the advantage of fast running speed, strong logic function, abundant on-chip RAM resources and good universality. Implementation of LZW algorithm with FPGA must solve the following problems [17]: the first problem is a dictionary generation. Generally, the dictionary is completed by using limited on-chip RAM resources integrated in FPGA. The second problem is the dictionary maintenance which is realized by the on-chip logic resource integrated in FPGA. In the compression algorithm, it is important to decide whether the existing dictionary which is need to update or not according to the current character string after lookup the dictionary. Complicated dictionary costs much time and more logic resource in management. The last one is output recoding problem after compression. The native format change of stored data leads to the change of quondam packet information. In the process of data decompression to recover, it is necessary to carry out processing because the boundary of data packet cannot be defined clearly. The compressed output data is 12 bit code, which is needed to be recoded according to the memory device or width of system data bus.

In the acquisition system of radar signal, the timing control of signal acquisition and processing is the key point to ensure the accuracy of data transmission [18]. In most cases, signal processing adopts pipeline data processing mode, as shown in Figure 6.

It can be easily seen from the figure that, firstly, radar data acquisition module must send interrupt signals to the main control device when the digital code is written to the store module through sampling channel. Analyzes and compresses sampling data are realized after data is written to the storage device. Because of the limit of the acquisition data cycle, this pipeline acquisition mode based on sending interrupt signal is not conducive to achieve real-time data compression. Since the decline of real-time transmission rate, the pipeline technique cannot meet the increasing demand of signal acquisition.

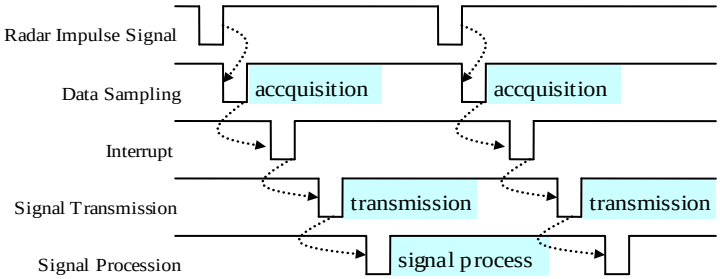

Figure 6. Pipeline Sequence Diagram of Radar Data Acquisition

In order to save FPGA I/O pins and minimize the system size, acquisition system introduced in this paper firstly divides 16 bit data into high 8 bit and low 8 bits. The two groups of data are respectively written to addresses corresponding to the data buffer module in FPGA. The timing control module sends the cached data sequentially into the LZW algorithm module and receives the state signal from other module. Then the compressed data is written to the system bus width through the data width conversion module.

Because the system needs a lot of on-chip Block RAM resource to generate FIFO and dictionary, we adopt the Xilinx company's Virtex-E series XCV400E. This device has abundant RAM resources, a total of 40 Block RAMs, and the capacity of each Block RAM is 4096 bits. Block RAM can be used as the on-chip and off-chip buffer of FPGA, high-speed parallel accessed buffer memory and bus width converter. The control signals of each port in dual-port RAM are separated in our design, and the data bus width of each port can be independently configured. The Data Cache and data width conversion module use dual-port RAM in the acquisition system, and the dictionary storage module selects single-port RAM [19]. The FPGA on-chip integrated function module as compression control module is shown in Figure 7.

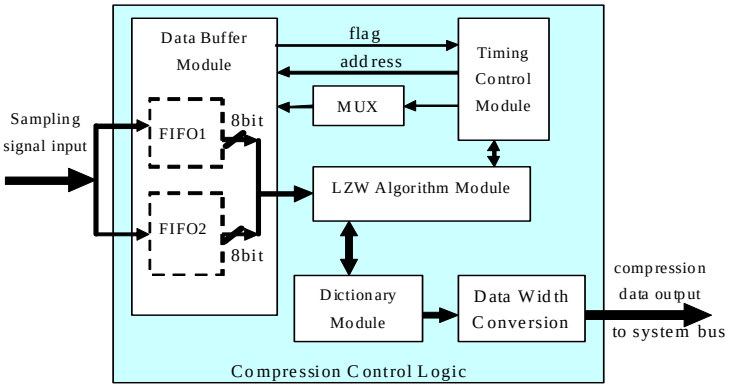

Figure 7. Compression Module Composition of FPGA

From Figure 7, the main control device consists of four modules:

a. Timing Control Module.

This module realizes read and write operations of data buffer by judging the flag of FIFO, and it also provides control signals for the other modules.

b. Data Buffer Module.

Two independent on-chip high-speed FIFOs are integrated in FPGA. In order to maximize its real-time processing speed, sampling data is written to buffer in parallel by judging the flag state of FIFO.

c. LZW algorithm module.

The key functions of dictionary initialization, lookup, judgment, upgrade, input code

compression and output code generation are realized in this module.

d. Dictionary Module.

It is used to storing compressed data information. A dictionary of 20 bit data width and 4K depth is generated by 20 RAM Blocks in parallel. Each area stores 20bit width character string, which consists of two parts. The head is 12 bit prefix character P, the tail is 8 bit current character S. The output is 12 bit characters.

e. Data Width Conversion Module.

12 bit output codes after compression are transformed to 16 bit width corresponding to the system bus. In this paper, four dual-port RAM blocks (RAMB4_S4_S4) constitute a 16bits 1K length high-speed FIFO in parallel. The compressed 12 bit output characters steam is transformed to 16 bit data through data width conversion module integrated in FPGA. Then the 16 bit output data is written into system bus.

4.3. Programme Flow of LZW Algorithm

Acquisition system in this paper leans from advantage of simple implementation in finite-state machine based on pipeline acquisition mode. Compression algorithm uses VHDL language to finish finite state machine. The algorithm flow is shown in Figure 8.

Table 1. Process of Compression Agorithm

Process	Dictionary Finger	Dictionary Character	Character Matching whether or not	Currently Character	Output Code stream
Initialization	000	0	-	-	-
	001	1	-	-	
	……	……	-	-	-
	0FF	255	-	-	-
1	-	-	23matching	23	
2	100	(23,76)	Not matching	76	017
3	101	(76,1)	Not matching	1	04C
4	102	(1,5)	Not matching	5	001
5	103	(5,23)	Not matching	23	005
6	-	(23,76)	(23,76）matching	76	-
7	104	(23,76,200)	Not matching	200	100
8	105	(200,255)	Not matching	255	0C8
9	106	(255,23)	Not matching	23	0FF
10	-	(23,76)	(23,76）matching	76	-
11	-	(23,76,200)	(23,76，200）matching	200	-
12	107	(23,76,200,48)	Not matching	48	104
13		……		……	……

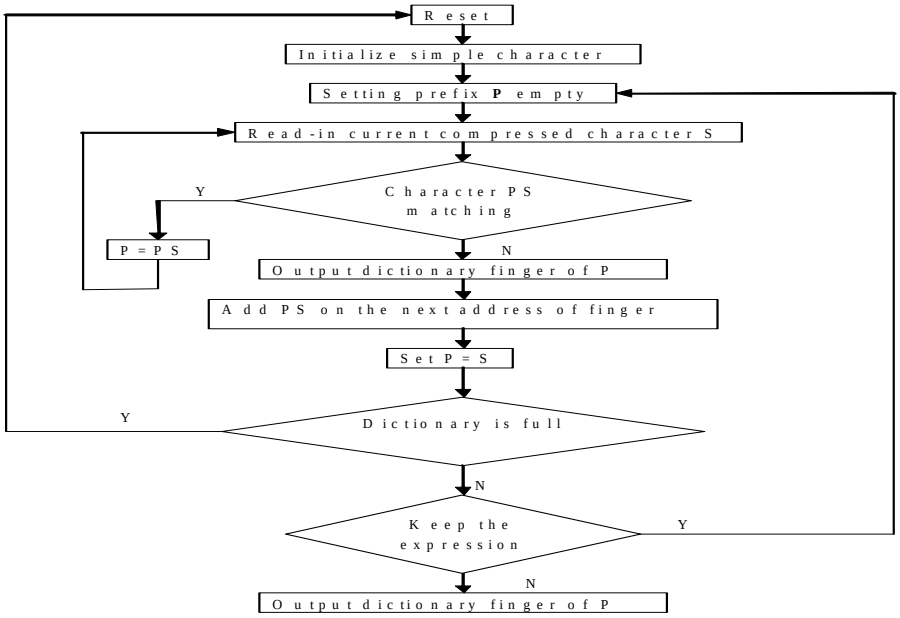

Figure 8. Expression Algorithm Flow Chart of Finite State Machine

State machine firstly complete the initialization process. The corresponding data 0~255 are stored in physical address 000H to 0FFH. Then state machine enters into the cyclic process of compression encoding. While reading current character, if it is consistent with some character in the dictionary, read the next character; else add this character to the end of current string. At the same time, state machine outputs dictionary pointer of prefix. Repeat the above process, until the end of the coding.

By using the string stream "23,76,1,5,23,76,200,255,23,76, 200, 48……" as an example, Table 1 describes the LZW compression process. The output stream is "017, 04C, 001, 005, 100, 0C8, 0FF, 104". The dictionary pointer and output stream are indicated by hexadecimal data. Table 1 shows the process of compression algorithm.

4.4. Test Conclusions Analysis

Because of the high- frequency radar pulse signal scanning, there should be more correlation of the same position and adjacent position in radar echo signal. It is the spatial relationship. In addition, the most great majority echo data of radar image is invariable. It is composed of static objects echo. The shift of moving objects is small in a few adjacent scanning cycles and the most data is overlapped. Besides that, displacement of moving object could be seen as translational motion to radar high-frequency signal scanners. It is the temporal relationship of the radar echo data.

When lossless compression algorithm is realized in data acquisition system, dictionary bit width and encoding unit are the main factors to be taken into account at the same time. We use MATLAB to simulate dictionary width of 10bit, 12bit, 14bit and 16bit. The unit length of data encoding is respectively 5K, 10K, 100K, 500K, 1M, 2M and 5M. The compression ratios of the different encoding data length (The ratio of the original data length to the data length of output compressed bit stream) under the condition of the different dictionary bit-width are simulated. 30 times simulations are done for each condition. Figure 9 is shown as the mean value of LZW algorithm compression ratio under different condition.

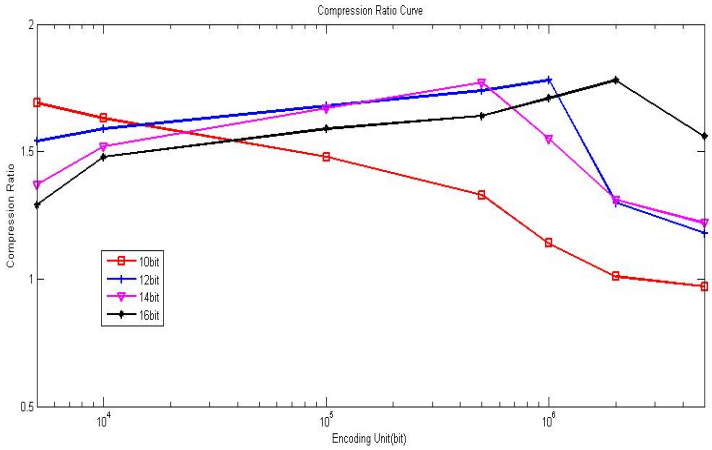

Figure 9. Compression Ratio Curve

We can see that higher compression ratio can be achieved for a short dictionary bit-width. But as the data length has increased, the compression ratio decreased. Although good compression ratio can be achieved in large dictionary bit-width under the condition of increasing encoding unit length, the running time of compression algorithmic could be long. Considering the dictionary storage space, the compression efficiency and running time of algorithm, the dictionary with 12bit was adopted.

In this paper, global clock frequency of radar data acquisition system is 100MHz. We choose two kinds of radar data frame to verify validity and feasibility of compression algorithms, as shown in Table 2. The compression ratio formula is the total number of bit in a block before compression to the total number of bits in the same block after compression. Among them, the

data frame 1 represents radar video echo text file whose capacity is 1M bits. But there is more clutter signal in this frame. The data frame 2 represents radar video echo text file whose capacity is 1M bits. This frame contains less clutter signal.

Table 2. Test of Compression Algorithm

Data Frame	File Type	Size (bit)	Output Steam（bit）	Compression Ratio
Frame 1	Text file	1M	713317	147%
Frame 2	Text file	1M	577822	181.5%

From the test results, the compression performance of slow change radar echo data with less clutter signal is better. However we can improve LZW algorithm to increase the compression ratio in the future. For example, solidifying the initialization process to saving compression time and simplify the control flow, or trying to memorize the position of dictionary pointer aiming at the high-frequency characters. It needn't to lookup the characters from the beginning of the dictionary, so the complexity of the algorithm is decreased.

5. Conclusion

This paper introduces the LZW algorithm applied in self-adapting radar video echo acquisition system based on FPGA. Because the sampling mode can be controlled by program, the system can acquire echo signal in different mode on the condition of not change the hardware design. By using the abundant on-chip Block RAM resource of FPGA, we realize the real-time acquisition and compression processing of massive radar data. The compression algorithm can be achieved by finite-state machine using VHDL. This method has strong portability and is easier to upgrade online.

Acknowledgements

The author thanks the anonymous reviewers for their valuable remarks and comments. This work is supported by 2013 National Natural Science Fund of China (Grant No. 51275492), 2012 Innovation and Entrepreneurship training program of the undergraduate of Shanxi Province (Grant No. 2012248).

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