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Low leakage decoder using dual-threshold technique for static random-access memory applications

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ABSTRACT

Decoders are one of the significant peripheral components of static random-access memory (SRAM). As the CMOS technology moves towards nano scale regime, the leakage power starts dominating dynamic power. In this paper, we propose decoders using NAND logic in 32 nm CMOS technology. Leakage power is reduced by employing dual-threshold technique. Dual thresholding is a technique that uses transistors of two different threshold voltages. The technique is implemented in simulation by two methods; first method uses transistors with different threshold voltage and the second method uses substrate biasing to vary the threshold voltage. Row and column decoders are designed and simulated in H-Spice. The leakage power is calculated and compared for both the methods. The NAND gate implemented by Method-1 and Method-2 provides a maximum leakage power savings of 87.67% and 90.81% respectively. The maximum leakage power savings of 96.76% and 98.74% is reported for the row decoder implemented by Method-1 and Method-2 respectively. Similarly, Method-1 gives maximum leakage power savings of 97.09% and Method-2 gives a savings of 99.11% for column decoder. The difference in leakage power savings of Method-1 and Method- at same threshold voltage is 3.14%, 1.98%, and 2.02% for NAND gate, row decoder and column decoder respectively.

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1. INTRODUCTION

CMOS technology scaling provides faster and high-performance devices, however, the power efficiency starts degrading due to the domination of leakage power in lower technology nodes [1]–[15]. Leakage or static power is a power consumed when the circuit is not functional. Nanoscale designs often employ optimization techniques to reduce power, area and improve circuit performance. Leakage power, data stability and speed of the circuit are the major requirements in today's static random-asccess memory (SRAM) design. However, maintaining the desired stability and reducing the leakage power is a challenging task. At lower technology nodes, read static noise margin (read stability) and write static noise margin (write ability) and functional failures of SRAM cell can be minimized by applying read and write enhancement techniques. Leakage power can be reduced by circuit design techniques [13]. In SRAM, one of the essential components are address decoders. The decoder design plays a significant role in determining the power consumption and access time of the memory [2]–[6]. There are solutions available in literature for reducing the leakage power of circuits [7]–[19]. Conventisonal decoders are implemented using AND gate. The problem with conventional design is AND gate cannot be directly derived in CMOS technology [6]. Moreover, when fan-in more than 4,

it slows down circuit functionality. Also, it occupies more area leading to increased delay and power consumption. Hence, decoders are realized using NAND, NOR, and NOT gates [5]. In NAND logic, all transistors need equal size thereby reducing the manufacturing cost. When considering gates with more inputs, NOR logic requires transistors of different sizes whose sizes are more compared to NAND logic leading to more area and manufacturing cost.

Akashe *et al.* [3] have proposed 2:4 decoder using Mutli thresholding technique with 2 inputs and 4 outputs in 45 nm technology. The decoder is designed by using CMOS NAND gates. Yavits *et al.* [4] dual mode logic (DML) address decoders are proposed, and results are compared with static CMOS decoders. The decoders are implemented using NAND and NOR gates from a commercial 16 nm low power library. In static mode, the proposed decoder consumes less energy and has lower delay as compared to the static CMOS address decoder. The design is recursive and can be extended to support any address width n.

In this paper, we propose 1:2 row and column decoders based on NAND logic in 32 nm CMOS technology. we use dual-thresholding technique simulated in two different ways to reduce the leakage power of decoders designed using NAND logic. The dual-thresholding technique employed is more effective in reducing the leakage power of decoders without affecting the performance.

2. METHOD

First, conventional NAND gate shown in Figure 1 is simulated in H-Spice. Then dual thresholding technique is applied to reduce the leakage power of NAND gate [20]. The dual-threshold voltage technique employs low and high threshold transistors where the performance and leakage power are critical respectively. High performance and low power are achieved using this technique. Alternativcely, substrate biasing can also be used to obtain dual-threshold voltages. A source to well reverse bias is applied to NMOS sleep transistors to achieve high thresholds [21]–[26]. In the simulation environment, dual thresholding technique can be simulated in two ways. First method is to use transistor with different threshold voltages. This can be done by changing the threshold voltage of transistors in model file. Second method is to use substrate biasing (body terminal) and vary the threshold voltage of the transistor. Here, we design and simulate NAND logic-based decoders for SRAM applications using H-Spice. The CMOS process technology used is 32 nm. The supply voltage and the temperature used are 1 V and 100 ℃ respectively. Predictive technology (PTM) transistor models are used to perform simulation.

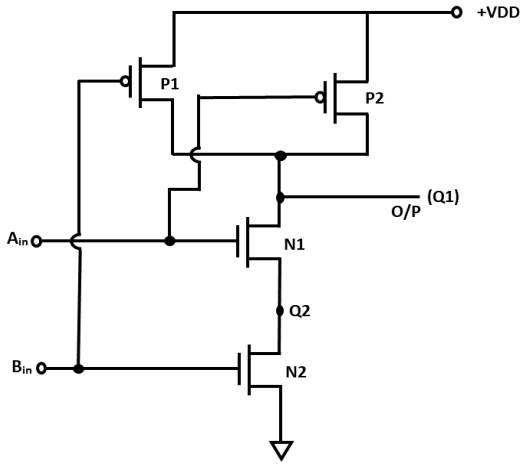

Figure 1. Two input CMOS NAND gate

3. METHOD

3.1. Method-1

The schematic of NAND implemented with transistors having two different threshold voltages (varied in model file) is shown in Figure 2. It consists of low threshold CMOS NAND gate connected in series NMOS sleep transistor of high threshold. Low threshold CMOS NAND logic has been implemented by employing high performance (HP) model. High threshold NMOS sleep transistor has been implemented by using of low power (LP) model. The threshold voltage of the transistor used for NAND gate design is 0.49396 V. The threshold voltage of NMOS sleep transistor is kept more than NAND gate transistors and is varied from 0.50396 V to 0.52396 V in model file. The leakage power is determined by making the input signal zero to the

sleep transistor and the results are tabulated in Table 1. The results shows that the maximum leakage power saving is 87.67% obtained at a threshold voltage of 0.52396 V. Also, increase in threshold voltage of the sleep transistor decreases the leakage power.

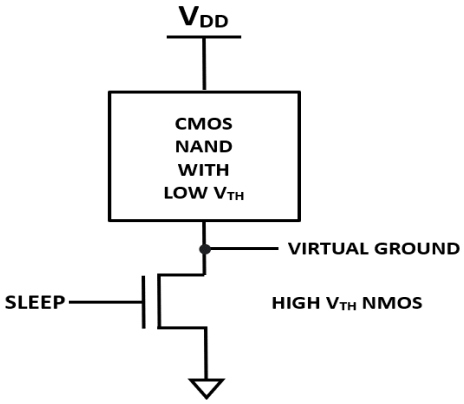

Figure 2. Dual threshold NAND gate implemented using low and high V_{th} transistors

Table 1. Leakage power comparison of conventional NAND and Dual thresholding technique (Method-1)

Circuit	Threshold voltage (V)	Leakage power (nW)	Saving compared to conventional design (%)
Conventiona NAND	0.50396	0.0.04892	
Dual threshold NAND	0.50396	0.007725	84.20
	0.51396	0.006798	86.10
	0.52396	0.006030	87.67

3.2. Method-2

The schematic of NAND implemented using substrate biasing is shown in Figure 3. In the schematic, low threshold CMOS NAND is connected in series with high threshold NMOS sleep transistor. Low threshold CMOS NAND logic and high threshold NMOS sleep transistor has been implemented by employing HP model only. The threshold voltage of NAND gate in the HP model is 0.49396 V. The substrate (body) terminal of NMOS sleep transistor is connected to negative voltage to vary the threshold voltage. The increase in reverse bias voltage increases the threshold voltage. The bias voltage for the circuit to fix or vary the threshold voltage is determined by plotting the transfer characteristics of the NMOS sleep transistor which is shown in Figure 4. The input signal to sleep transistor is made zero to determine the leakage power and the circuit is simulated and the results are tabulated in Table 2. The results shows that the maximum leakage power saving is 90.81% at threshold of 0.52447 V.

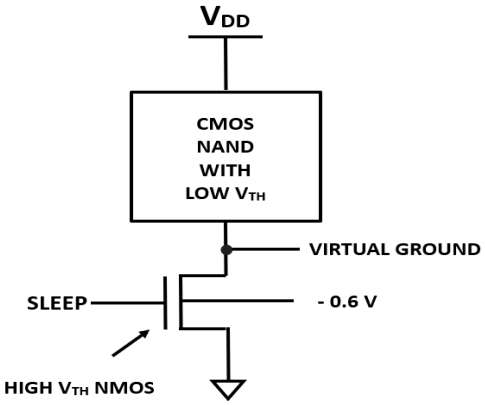

Figure 3. Dual thresholding technique implemented using substrate biasing

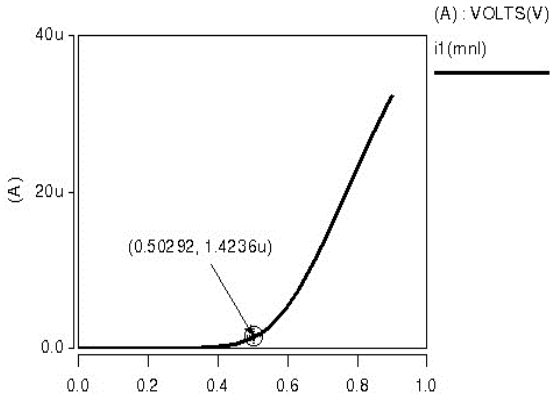

Figure 4. Transfer characteristics of the NMOS sleep transistor at bias voltage of-0.6 V

Table 2. Leakage power comparison of conventional NAND and Method-2 (substrate biasing)

Circuit	Threshold voltage (V)	Leakage power (nW)	Saving compared to conventional design (%)
Conventional NAND	0.49396	0.4031	
Dual threshold NAND	0.50292 (Bias voltage -0.6 V)	0.04712	88.31
	0.51432 (Bias voltage -0.7 V)	0.04104	89.81
	0.52477 (Bias voltage -0.8 V)	0.03702	90.81

3.3. Decoder design

A decoder is a logic circuit with n inputs 2^n outputs. It also has an enable input, when En = 1, which produces output. Address decoder is one of the critical components of the memory. In this work, 1:2 row and column decoders are designed using NAND logic and dual thresholding technique is applied to reduce the leakage power of the decoders. The decoders design is carried out using NAND gates, as it occupies less silicon area, cost effective and has lesser delay compared to NOR gates. Also, the dual threshold voltage technique applied for the design and simulation of NAND gate in two different methods are effective in calculating the leakage power.

3.3.1. Row decoder

Row decoder is essential element in all random-access memories which enable the word line by the address input. Row decoder produces 2^n outputs for n-bit address data. Among 2^n, one of the outputs activates SRAM cell. Address applied to the memory depends on the cell which is activated. The circuit and timing diagram of the row decoder using NAND in Figure 5 and Figure 6 respectively. From the timing diagram, the decoder outputs are zero when WLEN is zero. This shows that the proposed decoder can even support the retention mode of memory operation in addition to the read mode. NAND gate designed using Method-1 and Method-2 are used to design row decoder. Simulations are carried out and the leakage power is calculated. The leakage power consumption of low threshold row decoder depends on the threshold voltage of sleep transistor as they are connected in series. Leakage power can be varied by varying the sleep transistor threshold voltage.

To implement the row decoder in method-1, low threshold CMOS 1:2 decoder connected in series with NMOS sleep transistor of high threshold. High power models are used for decoder design and low power model is used for sleep transistor. The sleep transistor threshold voltage is varied from 0.50396 V to 0.52396 V by changing it in model file. The leakage power is determined simulation by making the input signal zero to the sleep transistor and the results are tabulated in Table 3. As expected, the leakage power decreases with increase in threshold voltage and the maximum leakage power saving is 96.76% at threshold of 0.52396 V.

For Method-2, model HP is used for both decoder design and sleep transistor. The threshold voltage of MOSFET transistor depends upon the bias voltage applied between the substrate (body) and source. The threshold voltage can be adjusted by varying the bias voltage applied between substrate (body) and source. By keeping the input signal of the sleep transistor zero, leakage power has been determined from simulation and results are tabulated in Table 4. The results shown in Table 4 reveal that as the bias voltage increases, threshold voltage also increases and decreases the leakage power. The maximum leakage power saving is 98.74% at threshold of 0.52477 V.

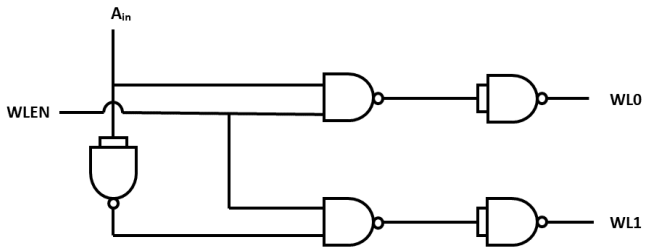

Figure 5. 1:2 Row decoder using CMOS NAND gates

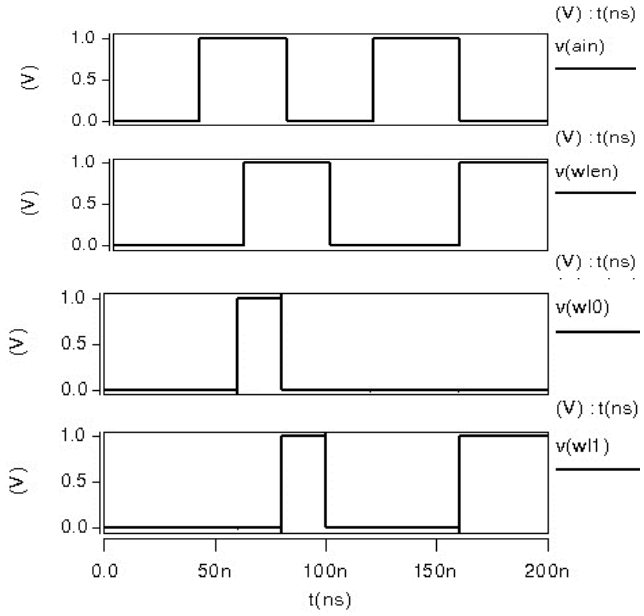

Figure 6. Timing diagram of 1:2 row decoder

Table 3. Leakage power comparison of conventional row decoder and dual-thresholding technique (Method-1)

Circuit	Threshold voltage (V)	Leakage power (nW)	Saving compared to conventional design (%)
Conventional row decoder	0.50396	7.149	
Dual threshold row decoder	0.50396	0.2717	96.19
	0.51396	0.2492	96.51
	0.52396	0.2316	96.76

Table 4. Leakage power comparison of conventional row decoder and Method-2 (substrate biasing)

Circuit	Threshold voltage (V)	Leakage power (nW)	Saving compared to conventional design (%)
Conventional row decoder	0.49396	17.71	
Dual threshold row decoder	0.50292	0.2782	98.42
	0.51432	0.2445	98.61
	0.52477	0.2219	98.74

3.3.2. Column decoder

The column decoder is a logic circuit and is used in memory array for selecting a particular column for modifying or reading the contents of the selected memory cell [5]. The column decoder circuit select one out of 2^M bit lines of the SRAM array according to column address of M-bit. The number of bit-lines to be decoded corresponds outputs of the last decoding stage. Power consumption and data access time in memories also depends on the column decoder design [6]. Conventional column decoder using NAND gate and simulated timing diagram is shown in Figure 7 and Figure 8 respectively.

Similar to row decoder both Method-1 and Method-2 is used to simulate the column decoder and the results are shown in in Table 5 and Table 6. The simulation results shown in Table 5 shows that the maximum leakage power savings of column decoder implemented using Method-1 is 97.09% at threshold of 0.52396 V. The results shown in Table 6 indicates that the maximum leakage power savings of column decoder implemented using Method-2 is 99.11% at threshold of 0.52477 V. The leakage power consumption of column decoder without applying the dual thresholding technique is lesser than that of the row decoder, as it has few transistors.

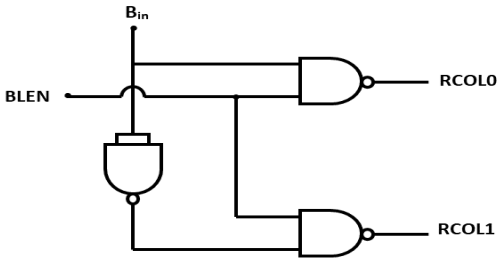

Figure 7. 1:2 Column decoder using CMOS NAND gates

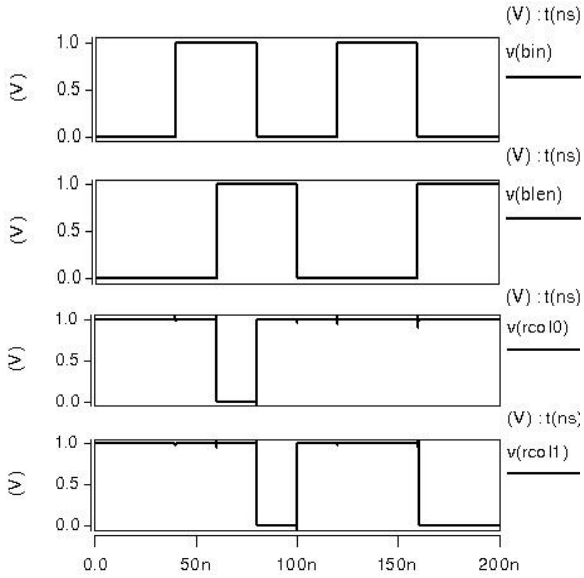

Figure 8. Timing diagram of 1:2 column decoder

Table 5. Leakage power comparison of conventional column decoder and dual-thresholding technique (Method-1)

Circuit	Threshold voltage (V)	Leakage power (nW)	Saving compared to conventional design (%)
Conventional column decoder	0.50396	4.268	
Dual threshold column decoder	0.50396	0.1469	96.55
	0.51396	0.1342	96.85
	0.52396	0.1238	97.09

Table 6. Leakage power comparison of conventional column decoder and Method-2 (substrate biasing)

Circuit	Threshold voltage (V)	Leakage power (nW)	Saving compared to conventional design (%)
Conventional column decoder	0.49396	10.88	
Dual threshold column decoder	0.50292	0.1130	98.96
	0.51432	0.1031	99.05
	0.52477	0.09669	99.11

4. RESULTS AND DISCUSSION

Address decoders are proposed using CMOS NAND gates. Dual-thresholding technique is applied to reduce the leakage power of NAND gate as well as address decoders in deep sub-micron technologies. The simulations are carried out on H-spice with CMOS process technology of 32 nm. The supply voltage and the temperature used are 1 V and 100 ℃ respectively. PTM transistor models are used to perform simulation. Two methods are proposed to vary the threshold voltage of the circuit designed. In Method-1, threshold voltage is varied in model file and in Method-2, substrate voltage is used to vary the threshold voltage. The maximum leakage power savings obtained from the NAND gate is 87.67% and 90.81% implemented by Method-1 and Method-2 respectively. Similarly, Method-1 gives maximum leakage power savings of 96.76% and Method-2 gives a savings of 98.74% for row decoder. The maximum leakage power savings of 97.09% and 99.11% is reported for the column decoder implemented by Method-1 and Method-2 respectively. The leakage power savings difference reported for Method-1 and Method-2 at same threshold voltage is 3.14%, 1.98%, and 2.02% for NAND gate, row decoder and column decoder respectively.

5. CONCLUSION

Row and column decoders have been proposed for the SRAM application in deep sub-micron technologies. Decoders havebeen designed by employing CMOS NAND gates, as this gate has many advantages compared to NOR gate in terms of area, manufacturing cost and delay. The leakage power consumption of conventional NAND, row and column decoders have been determined by performing simulation in 32 nm technology. The leakage power consumption of the proposed address decoders and NAND gate is reduced by applying dual-thresholding circuit level technique. In Method-1, threshold voltage is varied in model file and in Method-2, substrate voltage is used to vary the threshold voltage. The maximum leakage power savings obtained from the NAND gate is 87.67% and 90.81% implemented by Method-1 and Method-2 respectively. Similarly, Method-1 gives maximum leakage power savings of 96.76% and Method-2 gives a savings of 98.74% for row decoder. The column decoder provides a maximum leakage power savings of 97.09% implemented by Method-1 and 99.11% in Method-2 respectively. The Method-1 and Method-2 provides **t**he difference in leakage power savings at same threshold voltage of 3.14%, 1.98%, and 2.02% for NAND gate, row decoder and column decoder respectively. The dual-threshold technique is well suited for SRAM memory, as it reduces the leakage power without affecting the performance.

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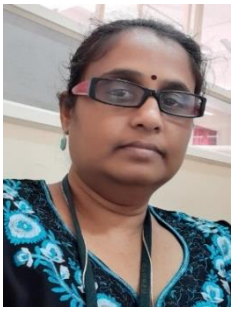

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