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A Small-sized High-performance Storage Module for High-g Measurement

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Abstract

The storage capacity, speed and the dimension of the storage device is restricted in the impact test environment. In order to meet high speed data transmission, data logging high reliability requirements in high-g environment measurement, the paper presents the design of a miniature high-performance memory module. The module uses a high-speed serial transceiver as the input interface, and through the FPGA to achieve real-time processing the high-speed data store into the large capacity memory chip. The dimension of the circuit module is merely 33mm×33mm but the storage rate can be up to 60Mbyte/s, and the capacity is 8Gbyte. Ensuring continuous and reliable operation requires a dedicated buffer for the data transmission. The paper proposes a multilevel high-speed buffer structure based on the field programmable gate array technology for speeding up data access. Then, the paper presents a protection shell for the circuit module, which introduces a steel shell filled with two-component epoxy resin for the protection in the high-g harsh environment. At the test of projectile penetrate the concrete; the impact acceleration peak is up to 1.42×10^{5}g. But the data storage module is stable and the inner circuit is well work under the impact, which validates the anti-impact protective structure designed by the method has the higher reliability.

Keywords*: high-g measurement, storage module, NAND flash, high-speed buffer, protection shell*

1. Introduction

The need for real time acquisition and storage is vital to measurement field. The structures of the storage system in the market are variety in different applications [1-5]. But in some harsh measurement environment, the instrumentations are always to be minimized. It's possible to accomplish the test in narrowness space and the data protection in harsh environment. The miniature data storage deceives can be used for the testing data in a wide field of high-g shock applications. The paper [6] developed a micro storage measurement unit, ϕ35×80mm^3, to acquire the acceleration and other sensors' signals in aircraft test. The system uses SRAM as the storage medium. Paper [7] provided a ultra high-g deceleration time measurement for the penetration into steel target and the paper [8] illuminated a ultra-high impact resistant digital data recorder for missile flight testing. The characteristics of those devices are low power consumption, small size and high reliability in high impact resistant environment, but thus is limited the capacity and the speed of the storage. The storage capacity of the proposed devices are not more than 20Mbyte, and the data use parallel transmission mode.

The performance of the data storage systems are usually limited the bottlenecks of storage capacity and the data streaming rate. The high-speed and large capacity storage devices which can up to several hundred gigabytes of non-removable memory, even to several terabytes, and the average sustained data storage rates are up to several hundred megabytes per second in the market are always big sizes, and they are either expensive or cumbersome or both [9-10]. They are not suitable to use in some special environment such as high-g deceleration measurement for the penetration into steel target or concrete are limited. In order to meet the demand for the high speed data storage in the high-g shock measurement environment, we should select the optimal dimensions and the rates of the storage due to the different of the using conditions. Except to ensure high speed data storage required by the

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system, miniaturized design is needed yet. In this paper, a high-performance storage module is expressed in terms of not only high storage rates, large capacity but also small dimension and low power. Miniaturization and high speed, high reliability and agility are key techniques for the storage module.

This paper introduced a high speed data communication interface based on LVDS and a high speed and large capacity data storage module of flash memory. It takes programmable logic device as the control core and achieves complex sequential and logical control through the hardware description languages (VHDLs). The high-speed data recording module has the advantages of high storage speed, large storage capacity, small volume, high flexibility and high reliability etc. The dimension of the circuit is merely 33mm×33mm, and the storage rate can be up to 60MByte/s and the storage capacity reach 8GByte in each storage module. It can realize higher memory bandwidth and storage capacity through extending the storage module. The paper also presents a protection shell for the circuit module in high-g shock measurement.

2. The Proposed Method

In order to overcome the challenges of high-speed data streaming, not only a high speed LVDS interface circuit, but also an effective way to continuously stream data into the flash memories by using FPGA technology. The circuits of the data storage module can be divided into several main functional blocks as depicted in the Figure 1: FPGA and PROM circuits, LVDS deserializer and cable equalizer, interface protection circuits, flash memories, power supply circuits and standby connector. All control processing algorithms and interface part are implemented in the FPGA. The LVDS signals first through the cable equalizer recovery into the LVDS deserializer to complete the serial-to-parallel conversion, then the data is temporarily stored into the buffer in the internal of the FPGA by using the recovered clock, and finally streamed in the flash memories.

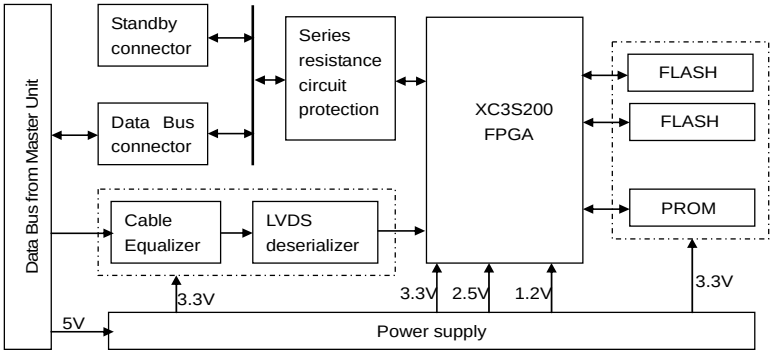


Figure 1. Functional Block Diagram of the Storage Circuit Module

The DS92LV1023A serializer and DS92LV1224B deserializer comprise a 10-bit serdes chipset designed to transmit and receive serial data over LVDS differential backplanes at equivalent parallel word rates from 40MHz to 66MHz. The LVDS signals are injected in a coaxial-cable, and received by the LVDS receiver. LVDS interface's transmission is always at the speed of the 60MByte/s, but some are invalid data and not required to record. Therefore, at the transmitting and the receiving of the data convention, the lower two bits are used as a determination flag for whether the data is valid data. The data communication protocol is shown in Table 1. Figure 2 shows the LVDS transmitting serial data format. Serial data are contained within frames of 10 bits, as well as coded information bits. A transmission is initialized by a leading low start bit. Next to the leading low start bit comes 10 bits of data information. The first two bits of 10 bits are used as the flag to identify whether it is the valid data. Finally, a trailing high stop bit is indicating the end of a data frame.

Table 1. Data Communication Protocol

Flag	d1d0	d9d8d7d6d5d4d3d2
Valid data	00	Valid data bits
Invalid data	01/10/11	Invalid data bits

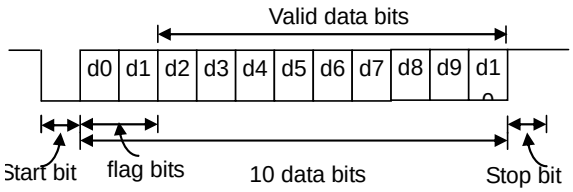


Figure 2. LVDS Transmitting Format

3. Research Method

All data processing algorithms are implemented in the FPGA. The chosen FPGA device is the Xilinx Spartan-3 XC3S200. It presents programmable a flexible architecture of Configurable Logic Blocks (CLBs), abundant block or distributed RAM resources and abundant programmable Input/Output Blocks, etc. The block diagram of the data transfer interface is shown in Figure 3. Several fundamental blocks designing entry through the hardware description languages (VHDLs) have been designed and implemented in the FPGA: LVDS controller, the RAM for data buffering and flash controller. It makes the complex logic design become legible hierarchy schema to facilitate the system debug, modify and transplant. A multi-level high-speed buffer structure is designed to match the high-speed data cache in FPGA. The primary buffer is an 8KByte dual-port block RAM, and the primary function is data buffering for the high speed LVDS signals. The subordinate buffer is composing of two 4KByte dual-port block RAM. It's an intermediate buffer being between high speed buffer and the flash memory devices, using two levels of buffer to speed up the access of memory system.

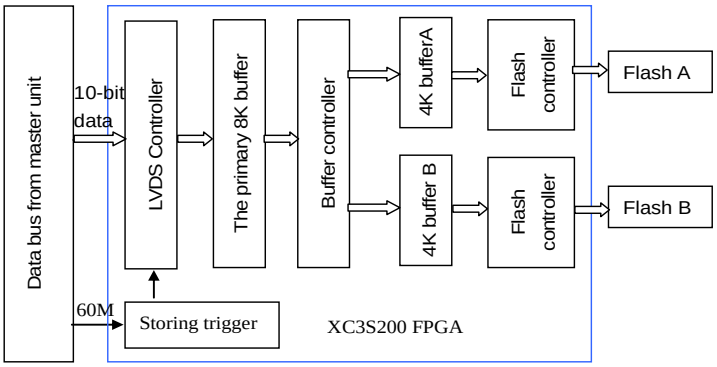


Figure 3. Block Diagram of the Transfer Interface Controlled

The on-chip real-time archiving is designed to store the continuous data that are temporarily stored in the FPGA internal buffers which is configured by the block RAM resource to nonvolatile memory. There are two stages to write data into the flash memory devices. The first one is to use the internal memory for buffering the high speed and continuous data stream. Figure 4 shows the basic steps of data reception. As a first step, the FPGA is programmed to incept the 10-bit binary data (d9~d0) from the LVDS deserializer and choose the high 8-bit binary data (d9~d2) to write into the primary buffer, and then check the low 2-bit binary data (d1 and d0) to identify whether it is the valid data. If d0 bit and d1 bit are all zero, the data is valid and then the buffer's write address plus 1, else come back the first step.

Figure 5 illustrates how the high-speed interface module works. As shown in the figure, 'LVDS_rclk' is 60MHz clock which is the recovered clock of the DS92LV1224 deserializer, and

the low 2-bit data are checked at the rising edge of recovered clock, at the same time, the high 8-bit binary data (d9~d2) is written to the primary buffer. ‘Fifo_wr’ is not ‘LVDS_rclk’. ‘Fifo_addra’ is the address control signal. When the low two bits of 10-bit data are "00" indicates that the data is valid data, the invalid flag ‘Inv_flag’ is set to high at the rising edge of recovered clock, else the invalid flag ‘Inv_flag’ is set to low. When ‘Inv_flag’ is high, the write address of the buffer will be plus one on the rising edge of clock ‘Fifo_wr’. In this way, the high speed and continuous data stream is written to the cache.

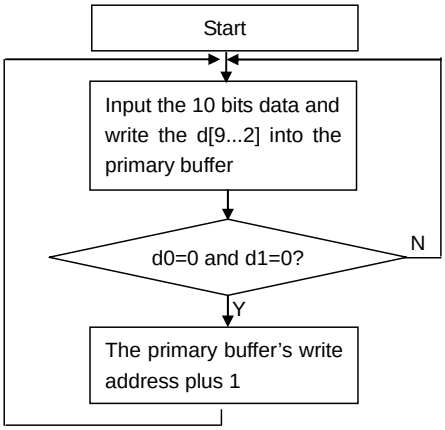


Figure 4. Data Reception Approach Flowchart

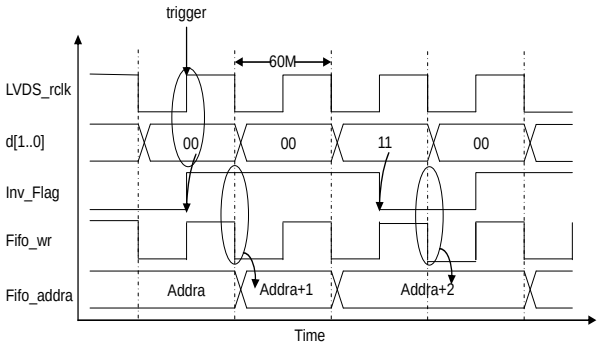


Figure 5. Time Diagrams Illustrate for Data Buffering

The second stage is processing the data in the specified source buffer and writing the data to the flash memory devices. Figure 6 illustrates buffer controller approach flowchart. The buffer controller continuously checks with the number of the data in the primary buffer, and if the total of the data is more than the maximum of 4160 bytes, and the data is read out 4096 bytes to the secondary buffer A at the rate of 120MByte/s. When the flash controller checks with the number of the secondary buffer A is more than 10 bytes, the secondary buffer A is read out by the flash controller at the rate of 30MByte/s and then written to the external flash memory chip A to perform page program. Then the buffer controller continuously checks again with the number of the data in the primary buffer. If the total of the data is more than the maximum of 4160 bytes, the data is read out 4096 bytes to the secondary buffer B at the rate of 120MByte/s. The same way is used to read the data from the secondary buffer B and written to Flash B. It continues to perform the time diagrams alternately until the record stopped.

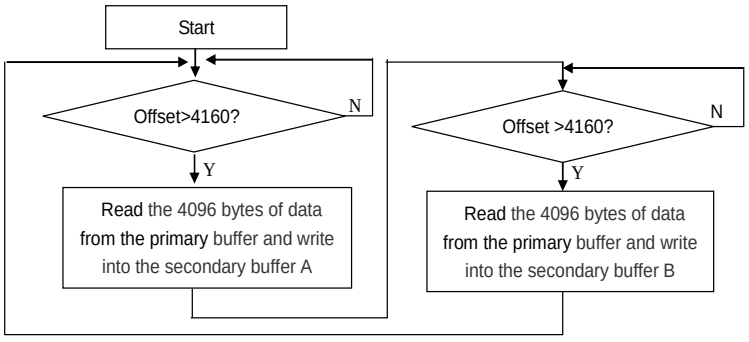
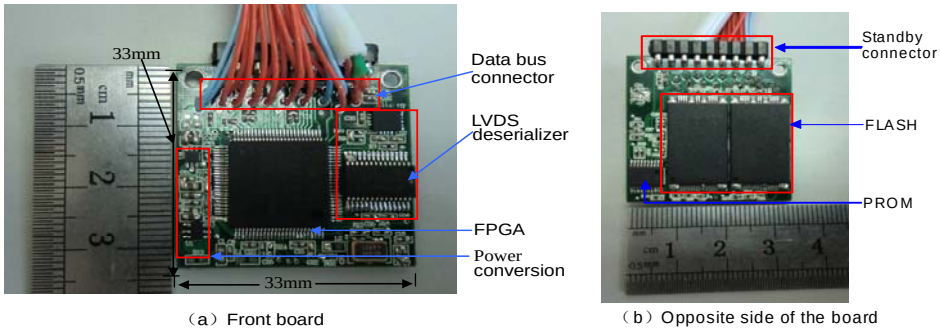


Figure 6. Buffer Controller Approach Flowchart

When the flash controller checks with the number of the secondary buffer are more than 10 bytes, it begins to enter the FLASH page program processing. The flash controller read 4096 bytes out of the secondary buffer and writes into the page registers at the rate of 30MByte/s. The max time for the page program is 700us and the typical time is 200us. The multiple measurements of the actual programming time are generally maintained between 150us to 250us. The Flash chip will not respond to other operation in this time. The two K9WBG08U1M chips are used to storing the high speed data by the interleave Two-Plane Page program. 4096×4bytes of data will be written for each programming cycle and the time for writing the data at 30MB/s is t= 4096 bytes×4/30MB/s=546us>250us. It can meet the requirements for the parallel operation.

4. Results and Analysis

In order to accord with the design requirements of miniaturization, the smaller package of the device is choosing, and the storage module is realized on four printed circuit boards (PCB). The prototype board of the system is shown in Figure 7. The size of the circuit board sizes are measuring at 33mm×33mm. The protection of the storage module is the focus of the design in high-g environment. Figure 8 illustrates a protection shell for the circuit module, which introduces a steel shell filled with two-component epoxy resin for the protection in the high-g harsh environment. The memory circuit module and metal shell is solidified as a whole can improve the impact resistance.



（a）Front board （b）Opposite side of the board

Figure 7. Circuit Board (33mm×33mm)

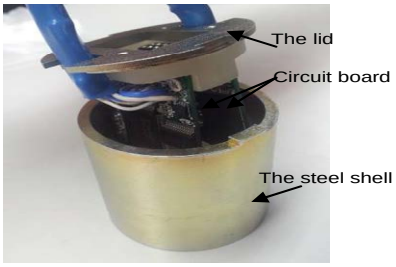


Figure 8. The Protective Structure

An experimentation for penetration into the concrete was used to test the reliability of the protective structure. As shown in Figure 9, the storage structure is stabile under the impact test and the inner circuit working properly, which proves the anti-impact protective structure designed by the method has the higher reliability. In Figure 10, the sensor actually measured the actual penetration of concrete targets acceleration peak value of -1.42×10^5g (the accelerometer is reverse placement).

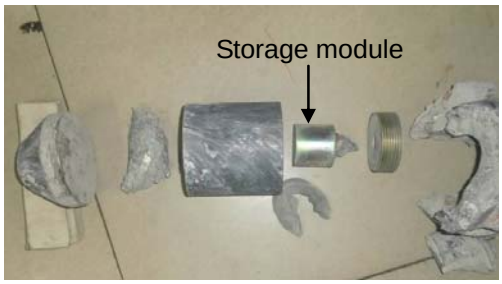


Figure 9. The Test of Recorder Penetration

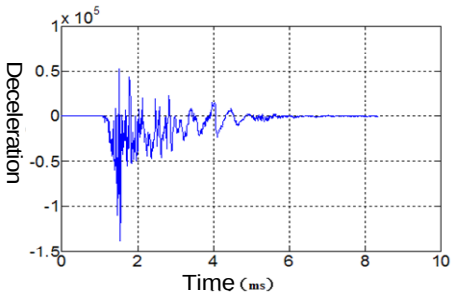


Figure 10. The Overload Curve of Penetrate Concrete

5. Conclusion

The paper dedicates to design a high-speed large-capacity storage module with a small size (33mm×33mm) which is based on NAND flash memory for the high-speed data storage in real-time. In order to store the high-speed real-time data, the paper studies the high-speed data communication interface module using LVDS and high-speed large-capacity storage module using flash memory chips. The whole processings are then implemented into FPGA hardware logic. The two-plane page program operation and pipeline technique is proposed to improve the average input and output speed of the recorder module. We design a set of data cache which makes full use of RAM resource inside the FPGA to resolve the matching problems of realizing high-speed input data and flash memories storage. In order to adapt the high-g test environment, a protection shell for the circuit module. The concrete penetration experiment shows that the module has high reliability. It can adapt to achieve the real-time high speed storage in harsh environment, and it can be used in other applications.

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