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An Improved Charge Pump with Suppressed Charge Sharing Effect

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Abstract

A differential charge pump with reduced charge sharing effect is presented. The current-steering topology is adopted for fast switching. A replica charge pump is added to provide a current path for the complementary branch of the master charge pump in the current switching. Through the replica charge pump, the voltage at the complementary node of the master charge pump keeps stable during switching, and the dynamic charge sharing effect is avoided. Apply the charge pump to a 4.8GHz band integer-N PLL, the measured reference spur is -49.7dBc with a 4-MHz reference frequency.

Keywords*: CMOS, charge pump, charge sharing, PLL*

1. Introduction

The phase-locked loop (PLL) is extensively used in modern communication systems such as LO signals generation in RF transceiver [1-3]. In the charge pump based PLL, the charge pump is adopted to transform the timing difference between the reference and the divider frequency into the control voltage to tune the VCO [1].

The non-idealities of the charge pump can induce spurious tones in the output of the PLL. Especially in the ∆-Σ frequency synthesizer, the quantization noise of the ∆-Σ modulator would be folded back into the in-band phase noise due to the mismatch of the charge pump [4]. As a mixed signal block, the dynamics of the charge pump should be carefully considered. The leakage current, the current mismatch, the charge sharing effect and the timing mismatch between the switching signals are the main problems associated with the charge pump [5]. Several charge pump structures were proposed to compensate these non-idealities in the literature [6-8]. A full differential charge pump is proposed in [6, 7], which the low-speed glitches are eliminated by adding capacitors at the common source nodes of the differential pair, and the high-speed glitches induced by capacitive coupling are cancelled by the source floating dummy transistors. A unity gain amplifier is used to hold the voltage at the complementary node stable. However, the charge sharing still exists due to the limited bandwidth of the unity gain amplifier. The source-switching charge pump in [8] is slow to turn off the output current.

This paper presents the design of a current steering differential charge pump. The charge pump employs a replica charge pump to keep the voltage stable at the complementary node of the master charge pump, which suppresses charge sharing effect. The charge pump is integrated in an integer-N PLL, and fabricated in the 0.18μm CMOS process.

2. Proposed Charge Pump

To avoid the dead zone, in every period of the reference signal, there is a duration when both UP and DOWN switches are both turned on. In that duration, the charge pump would inject the current noise into the loop filter, thus increase the in-band phase noise. The reference spur also would be increased if there is any current mismatch. The faster the switching speed of the charge pump, the smaller pulse width of the dead-zone avoidance pulses required. The

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differential current steering topology is preferred for its current mode operation, which switches faster than the gate-switched or the source-switched charge pump.

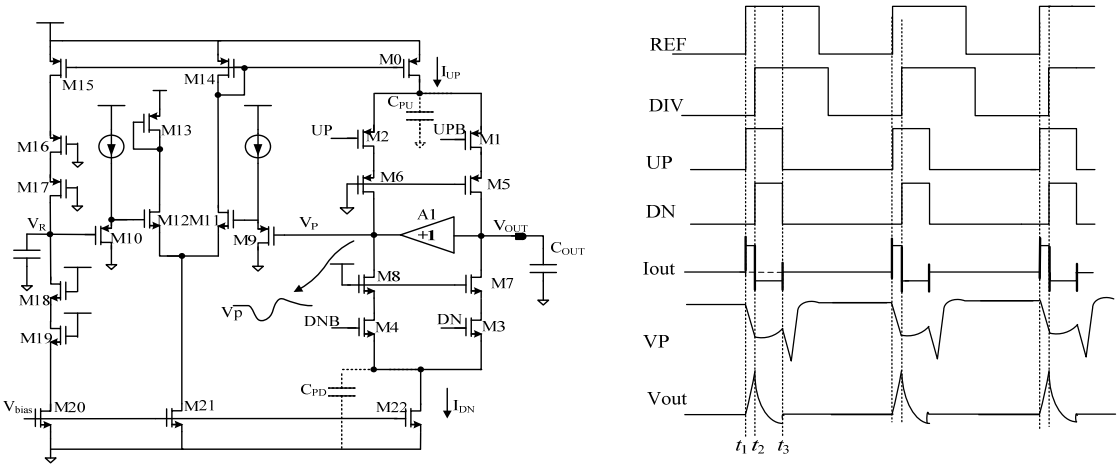


Figure 1. (a) The charge pump proposed in [4] and Schematic of the proposed Colpitts VCO, (b) Timing chart of the charge pump PLL

Figure 1(a) shows a high performance charge pump proposed by [8]. A self bias technique is used to reduce the sensitivity of the pump current mismatch to the common-mode output voltage. A simple op-amp by M9-M14 senses the output voltage, and compares it with its replica voltage VR, to adjust the charging current IUP until equal with the discharging current IDN. A unity gain buffer A1 was connected between the CP output VOUT and its dummy node VP, which keeps their voltage equal to reduce the charge sharing effect.

Although the charge sharing effect is reduced by the buffer A1, it is still not eliminated. When implemented in a chip, the current mismatch can only be reduced to about 1% due to the process deviations of the current mirrors. So when the PLL enters the locked state, there is still some phase offset between the REF and DIV due to the non-idealities.

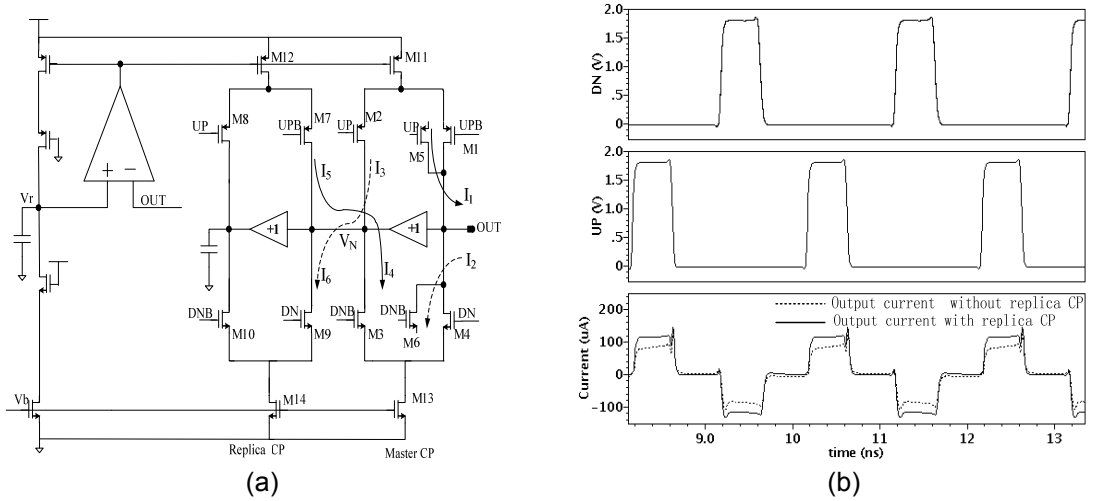


Figure 2. (a) The proposed charge pump with replica charge pump to eliminate charge sharing effect, (b) Transiant simulation of the charge pump with and without the replica charge pump

As shown in Figure 1(b), the voltage ripple in the charge pump output is observed when the PLL in the locked state. For example, assume the discharging IDN is slightly larger than the charging current IUP, to compensate the current mismatch, the signal UP goes high before DN. When the charging current IUP is switched from left branch to the output, the current IDN in the left branch still exists, so the voltage of the unity gain buffer's output VP suddenly drops R0IDN due to the limited response speed of the unity gain buffer A1, where R0 is the open-loop output impedance of A1. When the DN signal goes high, the voltage in the parasitic capacitor CPD differs from the output voltage VOUT, and the charge sharing occurs between the output capacitor COUT and the parasitic capacitor CPD [9]. According to the total amount of the charge injected to the loop filter keeps constant when the PLL locked, there is:

$$I_{CP}(t_2 - t_1) = \Delta i(t_3 - t_2) + Q_{CS} \tag{1}$$

Where QCS is the charge injection provided by CPD and CPU. The phase error is given by:

$$\phi_e = 2\pi \frac{\Delta i(t_3 - t_2) + Q_{CS}}{I_{CP} T_{ref}} \tag{2}$$

Where ICP is charge pump current, Tref is the reference clock period, and Δi is the current mismatch of the charge pump [5]. The spur can be calculated from Equation (2).

The amount of the reference spur in the 3rd-order PLL is approximately given by:

$$\mathrm{P_r} = 20\log\left(\frac{1}{\sqrt{2}}\frac{f_{BW}}{f_{ref}} N\phi_e\right) - 20\log\left(\frac{f_{ref}}{f_{p1}}\right) \tag{3}$$

For example, if we assume that fref =4MHz, fBW =80kHz, fout=5GHz (i.e. N=1250), fpl =300kHz, ICP = 120μA and t3-t2 =l ns, QCS=CPΔV, then Pr is calculated by:

$$\begin{aligned}\mathrm{P_r} &= 20\log\left(\frac{80kHz}{4MHz}\frac{1250}{\sqrt{2}} 2\pi \frac{10uA\times 1ns + 30\,fF\times 50mV}{80\mu A\times 0.25\mu s}\right) - 20\log\left(\frac{4MHz}{300kHz}\right) \\ &\approx -35dBc\end{aligned} \tag{4}$$

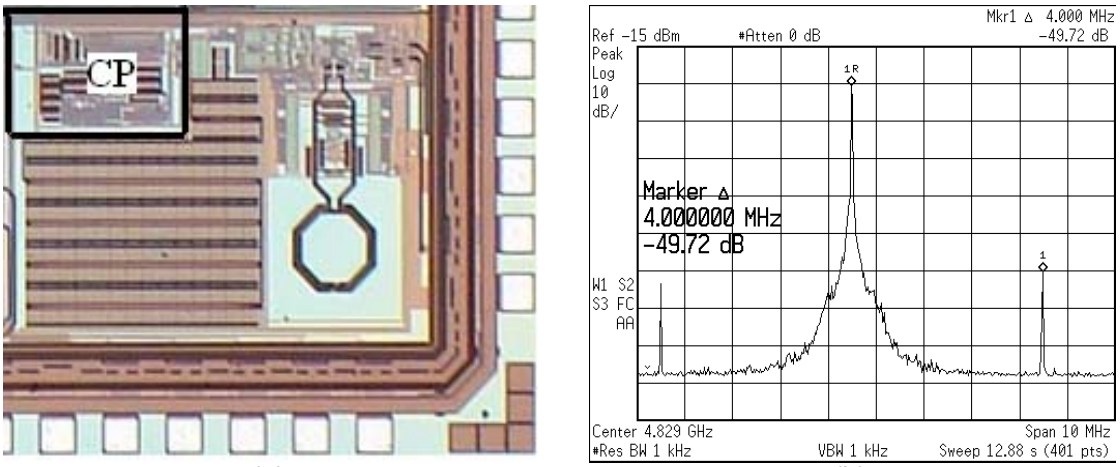
In addition, the voltage ripple at the node VP also disturbs the charging current through the bias feedback network.

To minimize the charge sharing from CPU and CPD, a charge pump is proposed, as shown in Figure 2(a). The charge pump circuit employs two identical charge pumps. The right one is the master charge pump to provide the current to the loop filter, the left one is a replica of the right charge pump. Either DN and UP signal goes high, the current flows in the middle branch has I2 = I6 = I3, I1 = I5 = I4. The current flowing into the node VN keeps nearly constant during the current switching, so the voltage at the node VN is stabilized, and the dynamic charge sharing can be substantially mitigated.

The dynamics of the charge pump was simulated with and without replica charge pump as shown in Figure 2(b), respectively. The charge pump output current level is designed to be 120uA. The signals UP and DN have a pulse width of 0.5ns with a transition time of 0.05ns. Without the replica charge pump, the charge sharing occurs when the switches turn on. The output current could not reach the designed value, which degrades the gain of the charge pump.

The process mismatches between the charging current source M11 and M12, the discharging current source M13 and M14 may impair the compensation effect. They cause the compensation current I5≠I4, I3≠I6. Even the replica charge pump would inject excess current into node VN in this case, the voltage ripple at the node VN can still be reduced by the replica charge pump and the unity gain buffer A2.

The process mismatch of the MOS transistors can be mitigated through the layout matching techniques, such as common centriod layout of current mirrors, adding dummy transistors and increasing overdrive voltage etc.



(a) (b)

Figure 3. (a) The chip microphotograph of the charge pump, (b) Measured reference spur at 4-MHz offset.

3. Measured Results

An integer-N PLL with the proposed charge pump is fabricated in a 0.18μm CMOS process. The supply voltage is 1.8V. The chip microphotograph is shown in Figure 3(a). The digital and the analog sections are separated by deep substrate trenches to avoid substrate cross-talk. The reference signal is 4MHz from a XTAL oscillator. The frequency synthesizer is designed to have a loop bandwidth of 80kHz with a 53° phase margin. The loop filter is a fully integrated passive third-order loop filter. The charge pump output current is set to be 120μA. The measured reference spur is -49.7dBc at 4MHz offset from a center frequency 4.829GHz as shown in Figure 3(b).

4. Conclusion

An improved charge pump of current steering topology with suppressed charge sharing effect is proposed. A replica charge pump is added to charge and discharge current to the complementary node of the master charge pump simultaneously. The charge sharing between the parasitic capacitors at the current source node and the loop filter is reduced. Apply the charge pump to a 4.GHz band integer-N PLL, the measured reference spur is -49.7dBc with a 4-MHz reference frequency.

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