Indonesian Journal of Electrical Engineering and Computer Science
Vol. 32, No. 1, October 2023, pp. 134~142
ISSN: 2502-4752, DOI: 10.11591/ijeecs.v32.i1.pp134-142

Ternary arithmetic and logic unit with carbon nanotube-based field-effect transistors for ultra-low power and high-speed applications

Murali Krishna Peddachowdappa, Vishnu Vardhan
Department of Electronics and Communication Engineering, Anantapur College of Engineering,
Jawaharlal Nehru Technological University, Anantapuram, India

Article Info

Article history:

Received Oct 14, 2022
Revised Jun 13, 2023
Accepted Jun 17, 2023

Keywords:

Arithmetic and logic unit
Carbon nanotube field effect transistors
Consumer electronics
Low power devices
Multi-value logic
Power delay product
Ternary logic

ABSTRACT

The number of consumers for different applications has expanded tremendously as a result of the growth of consumer electronics-related applications in numerous sectors. Customers often need high-speed applications that use a minimal amount of power for a variety of applications like signal processing, picture processing, and communication systems. The speed of a ternary logic-based design might be greater than that of a binary logic-based one. In this study, a novel architecture for arithmetic and logic units (ALUs) is proposed. The design makes use of ternary logic. In order to accomplish both low power consumption and high performance, methodologies for designing carbon nanotube-based field-effect transistors (CNTFETs) are employed. The method that has been suggested is able to carry out operations such as addition, subtraction, multiplication, reasoning, and comparison. After developing the recommended model, it is compared to earlier designs for power delay product (PDP), average power consumption, and maximum delay duration. The simulation findings show that the carbon nanotube field effect transistors (CNTFET) based ternary ALU circuits outperformed conventional ternary full adder circuits. The suggested design had a delay time of 13.94 ps and a PDP of 5.32 aJ, while the old design had a delay time of 17.67 ps and a PDP of 51.38 aJ.

Corresponding Author:

Murali Krishna Peddachowdappa
Department of Electronics and Communication Engineering, Anantapur College of Engineering
Jawaharlal Nehru Technological University
Anantapuram 515 002, Andhra Pradesh, India
Email: murali.43@gmail.com

1. INTRODUCTION

The traditional Bolano-like characterization of variables with a finite or infinite number of values, such as a ternary logic or a furious logic, replaces multi-valued logic because it lessens the number and complexity of the interconnections and a chip area [1], and as a result, increases the information content of the variables. For example, a ternary logic or a furious logic. A scale technology that increases chip density as well as the amount of broad use of portable communication and calculating systems is quickly becoming an essential component of the industry. Variables in the design of digital circuits and systems that are crucial to consider include power density, manufacturing costs, and resilience. The planning and execution of digital schemes have garnered a significant amount of attention, and as a result, binary logic is now an extremely important component in these areas [2]. This is due to the powerful mathematical and logical foundations as well as their inherent behaviour, which makes them suited for the implementation of integrated binary circuits [3].

According to Moore's Law, the total number of transistors on chipsets will double every 18 to 24 months; thus, the amount of space that is occupied and the amount of power that is wasted in the chipsets are crucial factors. One of the strategies that has been suggested for reducing the amount of space that is being used, speeding up the process of multi-valued logic (MVL) in circuit strategy. However decreased energy loss, or more specifically, the lowest energy loss in very large-scale integration (VLSI) circuits, generates an excessive amount of heat and therefore has an effect on the longevity and performance of circuits [4].

The logical circuit's ternary architecture is superior to the binary design, which was used before. In addition, the implementation of ternary logic may make use of serial and serial-parallel mathematics. All of this can be done in a more expedient manner. Compressed natural gas (CNG) is a carbon allotrope that may be conceptualised as a petal sheet folded into a cylindrical nanostructure, which is a two-dimensional carbon dioxide lattice. This structure is known as CNG. Multi-walled carbon nanotubes (MWCNTs), single-cylinder carbon nanotubes (CNTs), and single-wall CNTs comprising more than one cylinder are the three types of CNTs that may be considered secret [5]. In a carbon nanotube field effect transistors (CNTFET), a field-effect transistor, carbon nanotubes are used as the channel material for one or a range of semi-conducting carbon nanotubes, as opposed to bulk silicon, which is used in the creation of a normal metal oxide semiconductor field effect transistor (MOSFET).

When it comes to the performance of low-energy logic circuit design, CNTFET transistors are a feasible option to metal oxide semiconductor (MOS) transistors. CNFETs make use of a single wall CNT as a guiding channel, which is also known as the chiral vector. Depending on the tube angle of atom arrangement, CNFETs may either conduct or behave as a semiconductor. The voltage at the CNFETs' threshold fluctuates on the width of the CNT based on the chirality vector. Other types of CNFET are being researched in addition to normal CNFET. This is done in order to create conditions that allow the technology to be scaled down to 10 nm and beyond. Researchers at Stanford have recently presented evidence of a CNFET-based processor or computer [6], despite the fact that there has been a decline in interest in CNFET-based logic circuits owing to complex manufacturing processes and reliability concerns. CNTFETs are deserving of praise due to the unique mechanical and electrical characteristics that they possess [7].

This study involves the implementation and testing of a CNTFET-based arithmetic and logic units (ALU). CNTFET has the potential to cut power usage while simultaneously boosting operational speed. When compared to traditional fin field-effect transistor (FinFET), CNTFET is capable of reducing both the chip size and the amount of power used by leakage. In order to develop the ALU for high-speed signal processing and other communication-related applications, this study makes use of ternary logic. In the next part, section 3, you will find a detailed description of the planned planning.

The following outline has been prewritten for this paper: In section 2, specific information is defined on already-existing methods, along with the benefits and drawbacks of such methods. In section 3, the suggested design is broken down into its component parts and the internal architecture of the ternary ALU is clarified. In the section 4, find extensive information on the outcomes of several performance measures. This study comes to a close with a discussion of potential future work in section 5.

2. LITERATURE SURVEY

Various authors have proposed several techniques to increase the capability of ternary ALU by increasing the speed and reducing power consumption. In this section, a comprehensive analysis is performed based on some of the recent techniques used to optimize the design performance. Sharma and Kumre have proposed the low-power ternary ALU in the CNFET technology. In a multi-valuation logic system, the distinctive feature of CNTFET is its geometry-dependent threshold voltage. Depending on the status of input selection traits, the projected enterprise is depend on multiplexing arithmetic, logical, or diverse operations. The Hewlett Simulation Program with Integrated Circuit Emphasi (HSPICE) simulator synopsis with Stanford 32 nm CNFET shows the handling modules outperform complements regarding energy use, energy consumption, and device counting [8].

The innovative design for the ternary arithmetic and logic unit (TALU) employing CNTFet in this study was proposed by Gadgil and Vudadha. The TALU architecture includes a select block, transmitter gate block, and function modules. The functional components are designed with a 2:1 multiplexer-based concept. Compared with existing designs, this reduces the need for input decoders, resulting in fewer transits. Simulations on the existing and proposed TALU designs on the HSPICE-based circuit were carried out [9]. Bastani *et al*. [10] have developed a new rough ternary adder based on the CNTFET logic to lower the size and energy consumption. A new complete adder has been proposed. The designs wished for are expressively lower than that for other conventional, CNTFET-based trip circuits. The results achieved with Stanford 32 nm CNTFET simulator from Synopsys HSPICE have shown. This full ternary adder is also used to minimize the

steps of a ternary multiplier construction and to measure the efficiency of the cycles by calculating certain significant metrics. The design layout is also designed to measure area consumption.

Using CNTFET technology based on a novel decoder and multiplexer, Shalamzari *et al*. [11] have suggested developing fresh quaternary half-added and single-digit multipliers. A 32 nm Stanford compact model is used in the simulations that Synopsys HSPICE runs on the suggested designs. The outcomes from the functional analysis demonstrate that every design performs appropriately and flawlessly. In addition, the development in power delay product (PDP) for the half-adder and the anticipated multiplier was 81.34 percent and 74.07 percent, respectively, as compared to certain contemporary designs found in the literature. According to the findings of the simulation carried out using a variety of load condensers, process modifications, supply voltage, frequency, and temperature, the designs that were offered are functioning in a stable manner.

A novel voltage division structure was invented by Ebrahimi *et al.* [12], and it has the potential to be used in the production of four-valued logic. A voltage divider is used in the construction of the essential doors, which include a half-added adder and a full-adder, to guarantee that the design functionality is as promising as possible. In addition, a decoder has to enhance metrics for a half addition, such as the amount of power it consumes, the latency, and the number of transistors it uses. HSPICE, a software package designed specifically for simulation, is used to model the ideas. This semi-additional architecture has been improved in comparison to earlier attempts, and the results show a reduction in power consumption of 75%, a decrease in latency of 7.8%, and an increase in PDP parameters of 77%.

The innovative CNFET-based technique that Mehrabi *et al*. [13] developed for three-input exclusive-OR circuits and full-adder cell applications was published in The Journal Applied Physics Letters. These designs have several advantages, including high levels of performance, low levels of power consumption, and simple construction. Extensive testing is carried out in order to evaluate, under a variety of circumstances, how well the proposed designs would function. The simulation is done using synopsys HSPICE with complementary metal-oxide semiconductor (CMOS) 32 nm and CNFET 32 nm. The findings of the simulation indicate that the structures are superior to other recently developed CMOS and CNFET-based full adder cells.

Based on CNTFET carbon, Moaiyeri *et al*. [14] proposes the lowest, most energy-efficient logic circuits possible. The unique characteristics of CNTFETs, such as the abstraction that can be achieved by amassing sufficient diameters of carbon nanotubes, make it possible to design effective circuits that can accommodate a variety of threshold voltages. The suggested minimum and extreme circuits are used to calculate the threshold voltages. The Stanford 32 nm CNTFET knowledge provides a summary of the experiments that used Synopsys HSPICE and extensive simulations to examine the presentation and sensitivity for different process and temperature factors.

As a result of what has been said so far, it should come as no surprise that several efforts have been suggested to carry out high-speed ALU implementation. The bulk of current efforts are focused on reducing the amount of power that is consumed as well as the overall number of transistors. Additionally, a greater number of implementations are carried out based on CMOS and FINFET technologies. The following is an explanation of the primary purpose of this work:

- Implementing the suggested design for high-speed operations may help minimise the amount of electricity used as well as the complexity of the work.
- To use CNTFET to increase the unit's operating frequency to the maximum extent for high-speed digital applications.

3. PROPOSED DESIGN

A new CNTFET-based, low delay, and power consumption ternary-arithmetic logic cell are described. This architecture is appropriate for logical circuits, notably data transmission lines [15], with a wide range of load drives. This proposed architecture enters A third value into the binary logic function. This ternary logic can be used for simplifying circuits, reducing the difficulty of connections and chip space and, in turn, the power delay. This reduces energy efficiency in digital architecture. Due to the larger information content of each line, better use of transmission channels can be obtained. Serial and parallel processes may be accomplished more quickly by applying ternary logic. Allow 0, 1, and 2 to signify the ternary values of false, indeterminate, or true circumstances. The implementation of the ternary arithmetic circuit and logic design is explained in the following sections.

3.1. Carbon nanotube FET

Carbon nanotubes are formed by a thin sheet of cylindrical graphic carbon plates thicker than one atom. They have two useful cylinders, MWCNTs and single-wall carbon nanotubes. The CNTFET diameter (DCNT) is computed based on (1).

$$D_{CNT} = \frac{q}{\pi}\sqrt{n_1^2 + n_1 n_2 + n_2^2} \quad (1)$$

Where q is the distance of approximately 0.144 nm between neighboring atoms. CNTFET threshold voltage is determined as (2).

$$V_{TH} \approx \frac{0.43}{D_{CNT}/nm}\ eV \quad (2)$$

Where n,m are chiral vectors, the transistors are based on CNTFETs, because of their unique qualities, including compact size, fast speed, low power ingestion, and a similar feature to MOSFETs.

3.2. Ternary logic

In ternary logic, the smallest unit of memory is called a qutrit, and it has the capacity to store the values 0, 1, and 2. This capacity is represented by 31 vectors, which are written as follows: |0> = [1 0 0] T, |1> = [0 1 0]T, and |2 > =[0 0 1]T. T is given in [16]. |0 0.... 0>, |0 0.... 1>, and... |2 2... 2> are the discrete states that make up a ternary n-qutrit memory unit's three distinct states. Tensor multiplication is another method that may be used to determine all of the states that are feasible for a ternary n-qutrit system. The results of performing operations such as adding and multiplying using ternary numbers are shown in Table 1.

Table 1. Addition and multiplication of two ternary numbers

Addition (a)	0	1	2
0	0	1	2
1	1	2	1
2	2	0	0
Multiplication (b)			
0	0	0	0
1	0	1	2
2	0	2	1

3.3. Ternary logic representation

In the binary logic, the values {0, 1} mean Vdd = 1 and GND = 0. In the ternary case, use the values {0, 1, 2}, which means ½ Vdd = 1, Vdd = 2, and GND = 0. The binary logic, the values {0, 1}, which revenues Vdd = 1 and GND = 0. The basic actions of the ternary logic can be distinguished as follows, where $Xi, Xj = \{0, 1, 2\}$.

$$Xi + Xj = max[Xi, Xj] \quad (3)$$

$$Xi.Xj = min[Xi, Xj] \quad (4)$$

$$\bar{X}i = 2 - Xi \quad (5)$$

The symbols "+." and "−" are, respectively, for OR, AND, and NOT operations. Table 2 shows the logic table.

Table 2. Logic table

Voltage level	Logic value
0	0
½ Vdd	1
Vdd	2

Thus three inverters, one standard ternary (STI), one negative ternary (NTI) inverter, and positive ternary inverter (PTI) are shown in Table 3, are necessary for the construction of the ternary inverter. The combined interconnections and chip areas can be reduced by using ternary logic, as it reduces electric power delays. The higher information content of each line [17] may lead to better use of transmission channels. Serial and parallel processes may be accomplished more quickly by applying ternary logic. Let's assume the ternary values for false, undefined, and true instances are 0, 1, and 2, respectively.

Table 3. Truth table

Value	PTI	STI	NTI
0	2	2	2
1	2	1	0
2	0	0	0

3.4. Universal ternary logic gates

Ternary NAND and NOR gates can be used to appliance any logic, like binary NAND and NOR gates. Connecting to a transmission door at output [18], [19] creates the simplest ternary NAND and NOR gates. A dot in the gate symbol is displayed as standard or simple ternary gates. Table 4 shows the functionality of ternary logic gates.

Table 4. The truth table for ternary NAND, NOR, and EX-OR gates

A	B	NAND	NOR	EX-OR
0	0	2	2	0
0	1	2	1	1
0	2	2	0	2
1	0	2	1	1
1	1	1	1	1
1	2	1	0	1
2	0	2	0	2
2	1	1	0	1
2	2	0	0	0

3.5. Proposed design of inverter circuit

Figure 1 represents the circuit diagram for the ternary inverter, which includes a gate input connected to an input voltage Vdd and ground voltage 0. Vout gives the output value for this inverter circuit. A total 6 number of CNTFET transistors are used to design the inverter circuit. Through the gate, the input value is connected to the transistor. Output is produced based on the input voltage. Every transistors have a threshold voltage level based on the diameter of the transistors.

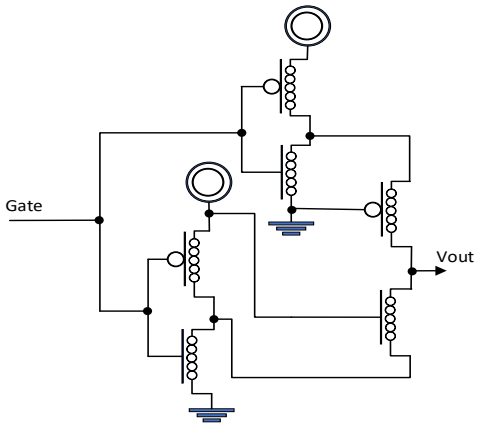

Figure 1. Circuit diagram of ternary inverter using CNTFET

3.6. Proposed design of NAND gate using CNTFET

The circuit diagram for the NAND gate is exposed in Figure 2. Input A and input B are connected to the transistors. Input voltage Vdd is connected to the top of the p-type transistors, and ground voltage 0 is associated with the n-type transistors' bottom. 6 CNTFET transistors are connected for this NAND gate.

3.7. Proposed design of NOR gate using CNTFET

The NOR circuit may contain 12 transistors connected. Similarly, Vdd and GND are used in different parts of transistors to construct this gate. Figure 3 shows the schematic diagram for the NOR gate. The fundamental gates in the digital schemes enterprise are the NOR gate, the inverter, and the NAND gate.

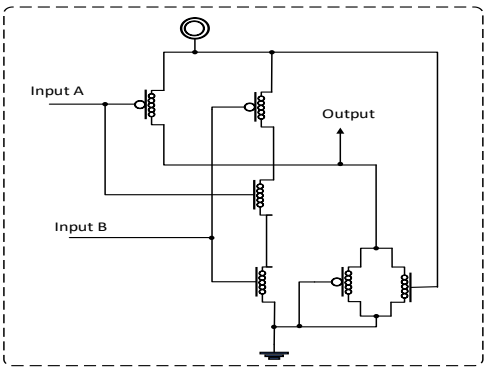

Figure 2. Circuit diagram for NAND gate using CNTFET

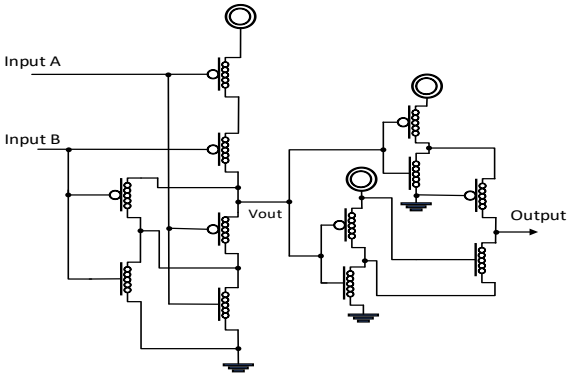

Figure 3. Circuit diagram for the NOR gate using CNTFET

3.8. Adder subtractor module

The suggested adder-subtractor module provides 2-bit ternary numbers with addition and subtraction [20]–[23]. The module accomplishes operations using the symmetry idea in a ternary adder and the structure of a subtractor from a popular ternary adder module [24], [25]. This cell's logical execution level can be found in Figure 4. All inputs are produced as a pulse for the terminal logic of inputs A and B. The outputs are S/D and carry/borrow.

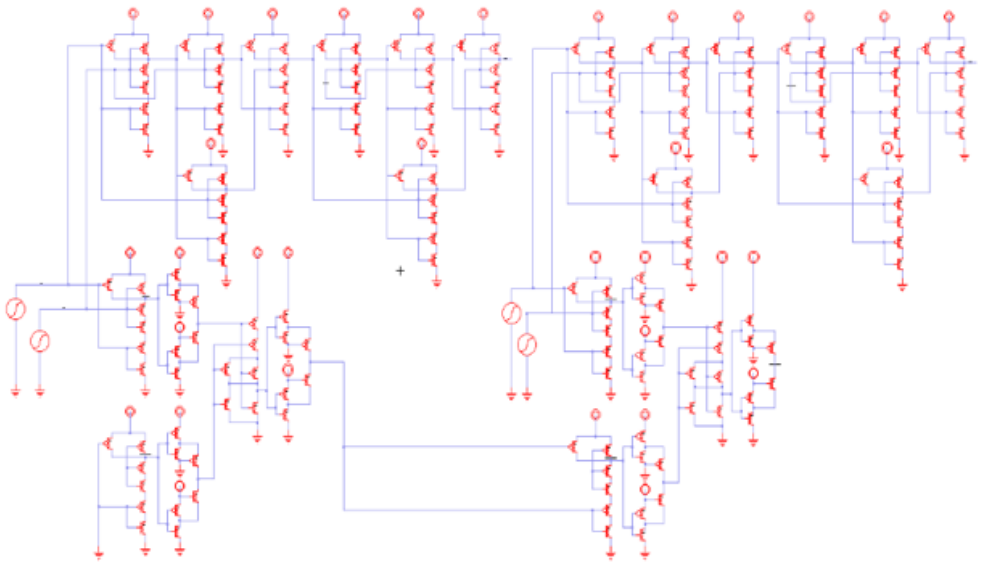

Figure 4. Adder/subtracter circuit using CNTFET designed in electronic design automation (EDA) tool

3.9. Comparator module

The combinational circuit is a module for comparing 2-bit ternary values A and B and determining their relative scales. Three binary variables indicating A>B, A<B, or A=B specify a comparison answer. Because the output variables cannot be logic 1, the available comparator can be based on binary gates, thus improving performance. The schematic circuit of the comparator is shown in Figure 5. Implementing gateways for the output variables (A=B), (A<B), and (A>B), indicating A=B, A<B, and A>B.

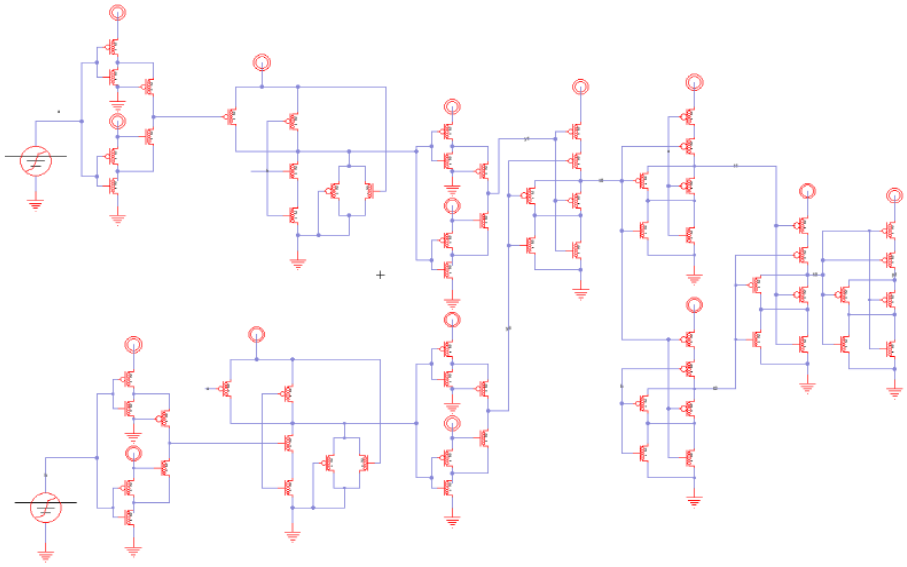

Figure 5. Comparator circuit using CNTFET designed in electric EDA tool

3.10. Proposed ternary arithmetic and logic unit

In this section, get a conceptual approach for implementing various blocks of ternary ALU architecture. This block has two input lines, A and B, as illustrated in a block diagram, and outputs that are depicted as Y out. Arithmetical modules such as the adder-subtractor, the multiplier, and the comparator module are designed as depicted in the block diagram. The design of multiplexer arithmetic circuits requires several uniform operators to be implemented.

Figure 6 shows that 4-bit input A and 4-bit input B are sent as input to the different modules, such as arithmetic, comparison, and logic modules, and the output of these lines is selected through a 2-bit MUX where the modes of operations are controlled. If the sel-1 is set as 00, an addition operation is performed. If it is set to 01, a subtraction operation is performed. If 02 is set, then the multiplication operation is performed. By combining the values of the sel-1 and sel-2, specific arithmetic operations are performed, and output is obtained at Y out.

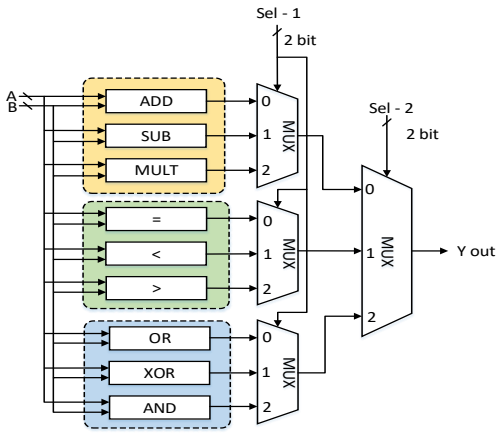

Figure 6. Block diagram of the proposed design

4. RESULT AND DISCUSSION

HSPICE software was used to conduct circuit modeling at the transistor level. The following points were considered for all transistors: channel length 32-nanometer, transistor 5-nanotubes, room temperature 0.9 power supply tension. Since fewer transistors have been utilized in NAND and NOR gates than in AND and OR, this delivers the optimum time and reduces energy usage. The standard type is designed for upgrade modes such as CNTFETs, where every transistor has one or more CNTs. The proposed design is simulated to assess the efficiency comparison of the proposed and existing ternary circuits. The results show improved power consumption and delayed products compared to other designs.

Table 5 displays the simulation outcomes of the science, technology, and innovation (STIs). The proposed design has less delay than the other methods of 13.94 ps and less power consumption of 1.095 µW. The capacitor used in the proposed design is also less than the other methods. The input voltage may range up to 0.9 from the wave. The inverted signals are obtained as results when compared to the input voltages. All possible combinations of input are applied to generate the output wave.

Table 5. Simulation of results of STIs

Simulated design	Maximum delay time (in ps)	Average power consumption (µW)	PDP (in aJ)	Maximum equivalent input capacitors
[1]	20.00	10.3	20.6	-
[3]	17.67	2.9	51.38	4
[7]	85.9	7.67	-	200
[9]	-	1.14	37.78	-
[14]	31.137	2.036	6.746	-
Proposed design	13.94	1.095	5.32	4

5. CONCLUSION

This study outlines the new design of ternary 4-bit ALU logic circuits utilizing a CNTFET. Binary logic today leads to future technology. Binary logic is necessary to create a complex circuit to increase the chip sizes and high-power dissipation in CMOS technology. In CNTFET-based ternary logic circuits, less power dissipation and reduced latency are obtained. Depending on the nanotube's diameter, the threshold voltage is adjustable for adjusting the threshold voltage for ALU circuits as for CMOS. The simulation results show that the existing design used nearly 200 input capacitors, whereas the proposed design used only 4. The proposed design minimizes the average power consumption by nearly 2% compared to conventional CNTFET designs. The above results illustrate the best possible future potential in ALU logic circuits with CNTFET-based Ternary circuits.

REFERENCES

[1] S. L. Murotiya and A. Gupta, "A novel design of ternary full adder using CNTFETs," *Arabian Journal for Science and Engineering*, vol. 39, no. 11, pp. 7839–7846, Nov. 2014, doi: 10.1007/s13369-014-1350-x.

[2] T. Chattopadhyay, "Design of optical reconfigurable balanced ternary arithmetic logic unit using MEMS based design," *Optics Communications*, vol. 356, pp. 123–135, Dec. 2015, doi: 10.1016/j.optcom.2015.07.035.

[3] A. Doostaregan and A. Abrishamifar, "Evaluating a methodology for designing CNFET-based ternary circuits," *Circuits, Systems, and Signal Processing*, vol. 39, no. 10, pp. 5039–5058, Oct. 2020, doi: 10.1007/s00034-020-01400-2.

[4] P. Keshavarzian and R. Sarikhani, "A novel CNTFET-based ternary full adder," *Circuits, Systems, and Signal Processing*, vol. 33, no. 3, pp. 665–679, Mar. 2014, doi: 10.1007/s00034-013-9672-6.

[5] M. H. Moaiyeri, K. Navi, and O. Hashemipour, "Design and evaluation of CNFET-based quaternary circuits," *Circuits, Systems, and Signal Processing*, vol. 31, no. 5, pp. 1631–1652, Oct. 2012, doi: 10.1007/s00034-012-9413-2.

[6] M.-A. Asadi, M. Mosleh, and M. Haghparast, "An efficient design of reversible ternary full-adder/full-subtractor with low quantum cost," *Quantum Information Processing*, vol. 19, no. 7, p. 204, Jul. 2020, doi: 10.1007/s11128-020-02707-4.

[7] M. H. Moaiyeri, S. Sedighiani, F. Sharifi, and K. Navi, "Design and analysis of carbon nanotube FET based quaternary full adders," *Frontiers of Information Technology & Electronic Engineering*, vol. 17, no. 10, pp. 1056–1066, Oct. 2016, doi: 10.1631/FITEE.1500214.

[8] T. Sharma and L. Kumre, "CNTFET-based design of ternary arithmetic modules," *Circuits, Systems, and Signal Processing*, vol. 38, no. 10, pp. 4640–4666, Oct. 2019, doi: 10.1007/s00034-019-01070-9.

[9] S. Gadgil and C. Vudadha, "Design of CNTFET-based ternary ALU using 2:1 multiplexer based approach," *IEEE Transactions on Nanotechnology*, vol. 19, pp. 661–671, 2020, doi: 10.1109/TNANO.2020.3018867.

[10] N. H. Bastani, M. H. Moaiyeri, and K. Navi, "An energy- and area-efficient approximate ternary adder based on CNTFET switching logic," *Circuits, Systems, and Signal Processing*, vol. 37, no. 5, pp. 1863–1883, May 2018, doi: 10.1007/s00034-017-0627-1.

[11] Z. D. Shalamzari, A. D. Zarandi, and M. R. Reshadinezhad, "Newly multiplexer-based quaternary half-adder and multiplier using CNTFETs," *AEU - International Journal of Electronics and Communications*, vol. 117, p. 153128, Apr. 2020, doi: 10.1016/j.aeue.2020.153128.

[12] S. A. Ebrahimi, M. R. Reshadinezhad, A. Bohlooli, and M. Shahsavari, "Efficient CNTFET-based design of quaternary logic gates and arithmetic circuits," *Microelectronics Journal*, vol. 53, pp. 156–166, Jul. 2016, doi: 10.1016/j.mejo.2016.04.016.

[13] S. Mehrabi, R. F. Mirzaee, M. H. Moaiyeri, K. Navi, and O. Hashemipour, "CNFET-based design of energy-efficient symmetric three-input XOR and full adder circuits," *Arabian Journal for Science and Engineering*, vol. 38, no. 12, pp. 3367–3382, Dec. 2013, doi: 10.1007/s13369-013-0627-9.
[14] M. H. Moaiyeri, A. Rahi, F. Sharifi, and K. Navi, "Design and evaluation of energy-efficient carbon nanotube FET-based quaternary minimum and maximum circuits," *Journal of Applied Research and Technology*, vol. 15, no. 3, pp. 233–241, Jun. 2017, doi: 10.1016/j.jart.2016.12.006.
[15] S. Vidhyadharan and S. S. Dan, "An efficient ultra-low-power and superior performance design of ternary half adder using CNFET and gate-overlap TFET devices," *IEEE Transactions on Nanotechnology*, vol. 20, pp. 365–376, 2021, doi: 10.1109/TNANO.2020.3049087.
[16] C. Vudadha, S. P. Parlapalli, and M. B. Srinivas, "Energy efficient design of CNFET-based multi-digit ternary adders," *Microelectronics Journal*, vol. 75, pp. 75–86, May 2018, doi: 10.1016/j.mejo.2018.02.004.
[17] S. Tabrizchi, N. Azimi, and K. Navi, "A novel ternary half adder and multiplier based on carbon nanotube field effect transistors," *Frontiers of Information Technology & Electronic Engineering*, vol. 18, no. 3, pp. 423–433, Mar. 2017, doi: 10.1631/FITEE.1500366.
[18] H. Samadi, A. Shahhoseini, and F. Aghaei-liavali, "A new method on designing and simulating CNTFET_based ternary gates and arithmetic circuits," *Microelectronics Journal*, vol. 63, pp. 41–48, May 2017, doi: 10.1016/j.mejo.2017.02.018.
[19] K. Navi, M. H. Moaiyeri, R. F. Mirzaee, O. Hashemipour, and B. M. Nezhad, "Two new low-power full adders based on majority-not gates," *Microelectronics Journal*, vol. 40, no. 1, pp. 126–130, Jan. 2009, doi: 10.1016/j.mejo.2008.08.020.
[20] M. Toulabinejad, M. Taheri, K. Navi, and N. Bagherzadeh, "Toward efficient implementation of basic balanced ternary arithmetic operations in CNFET technology," *Microelectronics Journal*, vol. 90, pp. 267–277, Aug. 2019, doi: 10.1016/j.mejo.2019.05.010.
[21] A. Kumar, S. K. Gupta, and P. Kota, "4-trit CNFET-based arithmetic logic unit," in *2023 International Conference on Device Intelligence, Computing and Communication Technologies, (DICCT)*, Mar. 2023, pp. 34–38, doi: 10.1109/DICCT56244.2023.10110209.
[22] B. Jeevan, K. Bikshalu, E. H. krishna, and K. Sivani, "Design of 2-1 multiplexer based high-speed, two-stage 90 nm carry select adder for fast arithmetic units," *Microprocessors and Microsystems*, vol. 99, p. 104846, Jun. 2023, doi: 10.1016/j.micpro.2023.104846.
[23] D. R. Florance and B. Prabhakar, "Design of joint reconfigurable hybrid adder and subtractor using FinFET and GnrFET technologies," *Integration*, vol. 88, pp. 32–42, Jan. 2023, doi: 10.1016/j.vlsi.2022.09.002.
[24] C.-C. Wang, O. L. J. A. Jose, W.-S. Yang, R. G. B. Sangalang, L. K. S. Tolentino, and T.-J. Lee, "A 16-nm FinFET 28.8-mW 800-MHz 8-bit all-N-transistor logic carry look-ahead adder," *Circuits, Systems, and Signal Processing*, vol. 42, no. 4, pp. 2283–2304, Apr. 2023, doi: 10.1007/s00034-022-02212-2.
[25] N. Ahmad, A. Kumar, S. K. Gupta, and P. Kota, "In-memory half adder computation using CNTFET transistors in 8T SRAM," in *2023 International Conference on Device Intelligence, Computing and Communication Technologies, (DICCT)*, Mar. 2023, pp. 44–49, doi: 10.1109/DICCT56244.2023.10110189.

BIOGRAPHIES OF AUTHORS

Murali Krishna Peddachowdappa received B.Tech. degree in electronics and communication engineering from JNTUH College of Engineering and Technology, Hyderabad M.Tech. degree in digital systems and computer electronics from JNTUA College of Engineering and Technology, Ananthapuram. He is presently doing his research in JNTUA College of Engineering in low power VLSI under guidance of Dr. D. Vishnu Vardhan. His areas of interest are low power, VLSI, and embedded systems. He can be contacted at email: murali.43@gmail.com.

Dr. Vishnu Vardhan an experienced professional with 20 years of teaching experience and 6 years of research experience, is currently serving as the Head of the Department of ECE at Jawaharlal Nehru Technological University Anantapur College of Engineering. Holding a qualification of M.Tech. and Ph.D., Dr. Vishnu Vardhan has made significant contributions to the field. His research interests primarily focus on embedded systems, image processing, and VLSI. With a total of 43 journal publications and 15 conference papers, Dr. Vishnu Vardhan has actively disseminated his findings to the academic community. In addition to his academic pursuits, he has been actively involved in various administrative roles, including serving as the NSS programme officer, officer in charge of the academic section, TEQIP-III coordinator, and placement officer at JNTUACE Ananthapuramu. As an associate professor and HOD, Dr. Vishnu Vardhan continues to demonstrate his expertise, leadership, and commitment to the field of ECE. His extensive experience and scholarly contributions make him a valuable asset to the institution and the academic community as a whole. He can be contacted at email: vishnu.ece@jntua.ac.in.