

## Research of High-voltage Impulse Track Circuit Receiver Based on Software-Algorithms

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### Abstract

*This paper aims to design a type of track receiver that relies on software algorithms and to optimize the whole structure of the track receiver. A voltage sensor is placed between the sender and receiver in a track circuit to collect high-voltage pulse signals generated by the sender. These signals are then sent to the CPU of the receiver for software operation. At the same time, the receiver also collects the high-voltage pulse signals from the track circuit. First, the Butterworth Low-Pass filters out 50Hz traction current of the pulse signals. These signals are the outputs from two different types of operating CPUs. Consequently, the main goal of this paper is to successfully design two sets of CPUs that respectively adopt two types of software algorithms, FFT and Mallat. It will be proven that this improved scheme has possibly reached the qualities of high speed and accuracy of CPU operation, and obviously improves instantaneity and reliability. It has been shown that this scheme, which is more feasible, has a higher degree of automation and is easier to maintain than the original equipments practically used. Hence, the scheme has the possibility of owning a much brighter application prospect in the future.*

**Keywords:** High-voltage impulse track circuit, receiver, FFT, Mallat

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### 1. Introduction

Track circuits, used in telegraphed code segments, mainly check the shunt and adjust the state of the track sections which effectively ensure the safety of trains` operation. Because of the movements towards high speed, modernized, intelligent and networked railway-signaling, the track circuit will play a very important role in the evolution of railway-signaling. The circuit can be applied in various fields such as: the interval of the railway, the station interlocking system and even both electrified and un-electrified rail tracks. High voltage pulse track circuit also known as high-voltage asymmetric track circuit was invented in 1953. This type of high-voltage asymmetric pulse signal was chosen as the track circuit signal source to reveal the status of the track segment, free or occupied, simply due to its remarkable ability to breakdown rusts, sand and greasy sediments on the surface of the track. It was originally used to solve the problem of bad shunting due to its gradual self-improvement and was successfully applied in the DC, AC electrochemical section of interval and station. Thanks to its excellent performance on solving various complex problems related to the practical function of track circuits and its extremely tenacious vitality, it will be used continuously in railway signaling systems [1].

### 2. The Improvements of the Internal Structure of the High Voltage Pulse Track Circuit Receiver

- 1) Firstly, the receiver adopts two sets of CPUs which rely on disparate software algorithms and is used for identifying and computing the high voltage pulse signal [2].
- 2) Secondly, the comparator, which replaces mechanized relay, displays the computed-results after being compared. Thus, it increases reliability and safety of the system.
- 3) Finally, the sensor receives the high-voltage pulse signal from the sender and sends it directly to the receiver, where the signal is computed by the CPU of the receiver. The entire system is designed as a closed-loop system, so the reliability of the system is greatly improved by this [3].

After successfully carrying out the improvements of the receiver, on the high-voltage impulse track, as mentioned before, its internal structure principle will be changed as Figure.1 shows below. On one hand, the high-voltage pulse signal is filtered out by a Butterworth low-pass filter. However, on the other hand, the signal, after optoelectronically isolated and A/D converted, is arithmetically operated by the CPU decoder. Here, two sets of CPUs are adopted as decoders which output the final results after comparison. The sensor receives directly the high-voltage pulse signal from the sender on the track circuit and re-sends the signal to the receiver for decoding-operation [4].

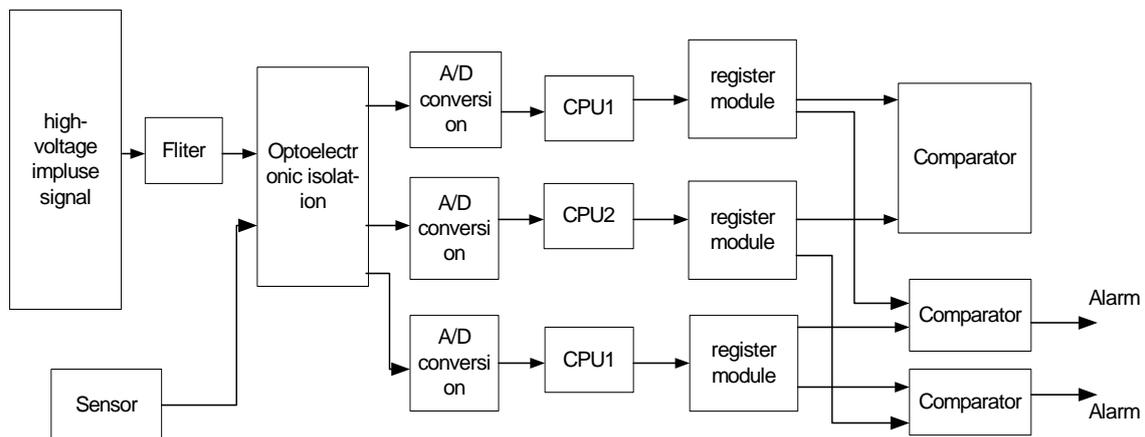


Figure 1. The diagram of high-voltage pulse track circuit receiver

### 3. High-Voltage Impulse Signal

The so-called "high-voltage" impulse signal, named after its higher pulse amplitude and the receiver, based on high-voltage impulse, is notably good at preventing some accidents from occurring such as: insulation damage and AC interference. The appearance of the signal is shown in Figure 2.

#### 3.1. The Simulation of High-Voltage Impulse Signal

The followings are the traits of the signal:

- 1) The cycle of pulse wave is  $1/3S$ . The spectrum of pulse is distributed from 0 HZ to 3KHZ continuously. The pulse peak's tail is mainly comprised of 100Hz low frequency components (or DC components).
- 2) The pulse's generator generates the high-voltage pulse signal with wave amplitude ranging from 50V to 100V and a frequency of 50HZ.
- 3) The head and tail of the high-voltage impulse are at an approximate ratio of 4:1 to 8:1.

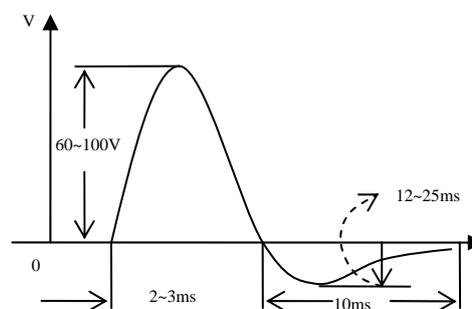


Figure 2. The wave of high-voltage impulse

High-voltage impulse signal is stimulated under the circumstance of MATLAB and its shape is shown in Figure 3.

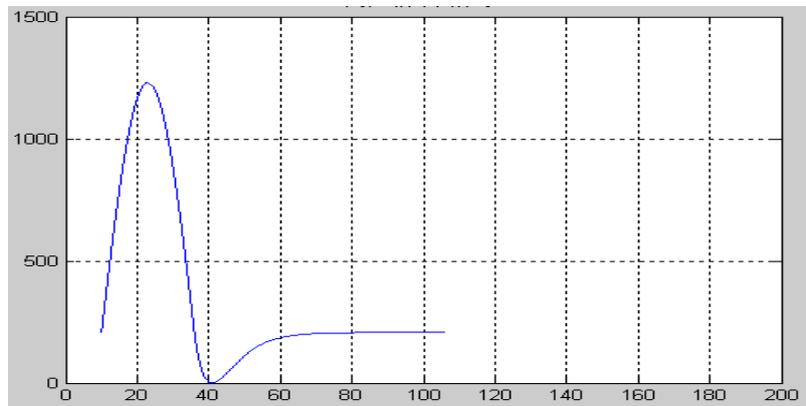


Figure 3. High-voltage impulse signal

### 3.2. Filtering the Propulsion Current

The filter module is designed to filter some clutter waves like the 50 Hz traction current from the high-voltage pulse signals. We would like to devise the Butterworth filter as the band-stop filter since its performance of simulation is vividly better than that of the designed band-pass filter. So, band-stop filter is adopted in the simulation process.

Simulation of high-voltage impulse signal interfered by propulsion current and the signal after 50Hz traction current being filtered out are separately shown in Figure 4 and Figure 5 [5].

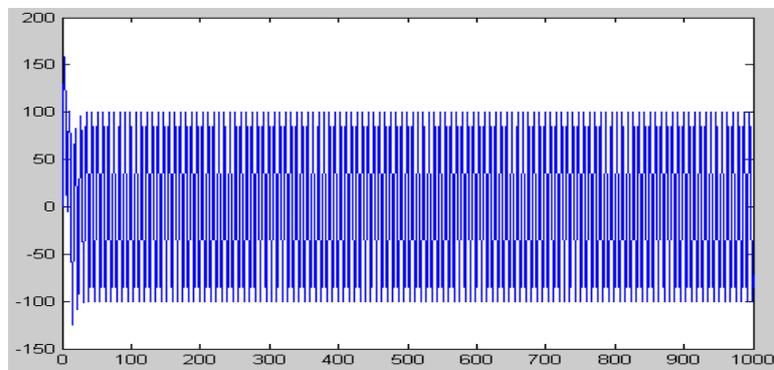


Figure 4. Simulation of high-voltage impulse signal interfered by propulsion current

## 4. The Proposed Algorithms

The high-voltage impulse track circuit receiver primarily relies on two sets of CPUs to effectively collect and operate the high-voltage impulse signal. The CPUs adopt two different types of software algorithms so as to improve the reliability and safety of the system. Whether the interval is occupied or not can be determined by the consistency of compared results. The two sets of CPUs employ software Fast Fourier Transform and Mallat respectively [6].

### 4.1. Fast Fourier Transform (FFT)

Fast Fourier Transform, abbreviated as (FFT), was proposed by Cooley & Turkey in 1965. It is a really new and fast algorithm, which increases the operation's speed by several hundred times, causing a brand-new subject—Digital Signal Processing to appear [7].

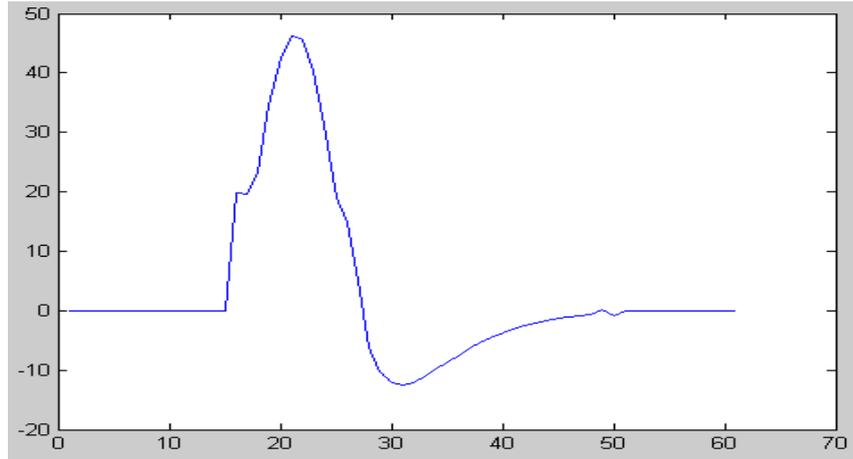


Figure 5. The signal after filtering 50Hz traction current

The procedure for transforming Sequence  $\{A_k\}$  to Sequence  $\{x_j\}$  which has the same length as  $\{A_k\}$  is listed below.

$$x_j = \sum_{k=0}^{N-1} A_k W_N^{-jk}, \quad j = 0, 1, \dots, N-1 \quad (1)$$

$$A_k = \frac{1}{N} \sum_{j=1}^{N-1} x_j W_N^{jk}, \quad k = 0, 1, \dots, N-1 \quad (2)$$

$$W_N = \exp\left(\frac{2\pi i}{N}\right)$$

Here, In order to process DFT and its reverse transformation with a unified program we revise the Formula (2) as the following shows:

$$A_k = \frac{1}{N} \sum_{j=0}^{N-1} x_j W_N^{-jk} \quad (3)$$

Or

$$A_k = \frac{1}{N} \sum_{j=1}^{N-1} x_j W_N^{jk}, \quad k = 0, 1, \dots, N-1 \quad (4)$$

Only a constant factor differs here and for the narrative convenience, we merely assume DFT rather than FFT algorithm and adopt the same program to request  $x_j$  and  $A_k$  by simply calculating  $x_j$  and  $A_k$  according to formula (1). It must be made known that formula (1) can be indicated as a linear system as shown below.

$$\begin{pmatrix} 1 & 1 & 1 & \dots & 1 \\ 1 & W_N^1 & W_N^2 & \dots & W_N^{N-1} \\ 1 & W_N^2 & W_N^4 & \dots & W_N^{2(N-1)} \\ \dots & \dots & \dots & \dots & \dots \\ 1 & W_N^{N-1} & W_N^{2(N-1)} & \dots & W_N^{(N-1)(N-1)} \end{pmatrix} \begin{pmatrix} A_0 \\ A_1 \\ A_2 \\ \vdots \\ A_{N-1} \end{pmatrix} \tag{5}$$

$$W_N^{jk} = \cos \frac{2\pi jk}{N} + i \sin \frac{2\pi jk}{N} \tag{6}$$

$$W_N^{jk} = \cos \frac{2\pi jk}{N} + i \sin \frac{2\pi jk}{N}$$

If we don't consider the calculation amount produced by the one complex number processing includes its multiplication and addition. Obviously, it takes  $N^2$  times of complex number multiplications to calculate  $\{x_j\}$  from  $\{A_k\}$  in accordance with formula (1). While under any normal circumstance people can actively choose  $N$  to meet certain conditions so as to greatly reduce the calculation amount derived from multiplications [8]. For example, let  $N=2^r$ , therefore  $N^2=2^{2r} = 4^r$ , and then the complex number calculation amount becomes  $o(N \log_2 N) = r2^{2r}$ . It will significantly and notably reduce the calculation amount when  $N$  is big enough.

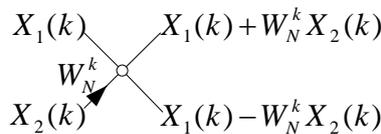
This paper adopts radix-2 FFT algorithm. Suppose the length of sequence is  $N=2^M$  ( $M$  is a positive integer), here it will be called radix-2 FFT algorithm based on time extraction since the sequence is decomposed into shorter sub-sequences according to parity of chronological order.

The following is the formula for calculating FFT:

$$X(k) = X_1(k) + W_N^k X_2(k) \quad k = 0, 1, \dots, N/2 - 1$$

$$X(N/2 + k) = X_1(N/2 + k) + W_N^{(N/2+k)} X_2(N/2 + k)$$

$X(k)$  is the former part of the sequence and  $X(N/2 + k)$  is also the latter part of the sequence. Similarly, the two formulas above can be presented in butterfly algorithm.



Descriptions:

- (1) The left side is the input source;
- (2) The right side is the output source;
- (3) The central small circle represents operations addition and subtraction, with the upper right being addition and the lower right being subtraction.

Take  $N=8$  as an example, so the relation between input order and output order is shown in the following chart.

Chart 1. The relation between input and output of the sequence

The basic order of sequence of input	Decimal numeral	Binary code	Code inversion results	Decimal number Out-of-order	Input order of disordered sequence
$x(0)$	0	000	000	0	$x(0)$
$x(1)$	1	001	100	4	$x(4)$
$x(2)$	2	010	010	2	$x(2)$
$x(3)$	3	011	110	6	$x(6)$
$x(4)$	4	100	001	1	$x(1)$
$x(5)$	5	101	101	5	$x(5)$
$x(6)$	6	110	011	3	$x(3)$
$x(7)$	7	111	111	7	$x(7)$

It must be read backwards since the input series is sequential and the output frequency-domain is disorderedly arranged by the regulation that the codes bit need to be read backwards in the 2FFT operation extracted by frequency. The basic requirement of 2FFT is  $N = 2^m$  where M is a positive integer. It is easy to meet this requirement since  $N$  can simply be selected using one's initiative. However, if we are unable to select  $N$ , we may use the method of expanding sequence by zeros which is the smallest integer. The flow chart of changing code bits` position operation is shown below. Since we know the theory of changing the code's position, we can now manage to operate the code's sequence.

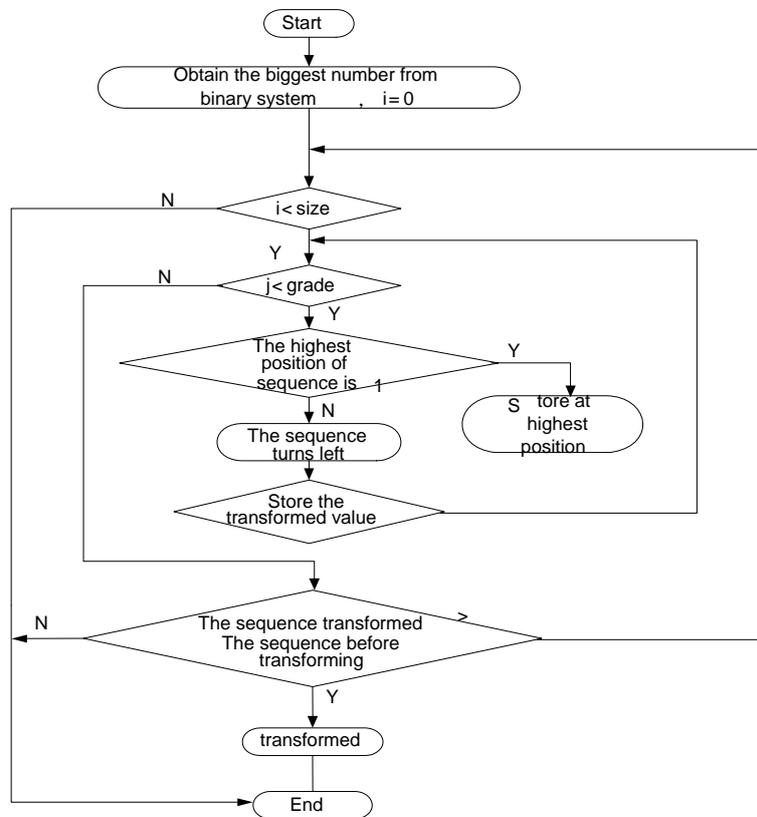


Figure 6. The flow chart of changing code position

The flow chart of operating FFT is displayed in Fig.7. After finishing the initialization of transformation kernel and the operation of code bits, we may start the operation of FFT. The operation of FFT is mainly geared towards commencing butterfly algorithm on the results, stored in register, after changing code's positions. The recurrent for-sentences in program will output the final results for FFT operation.

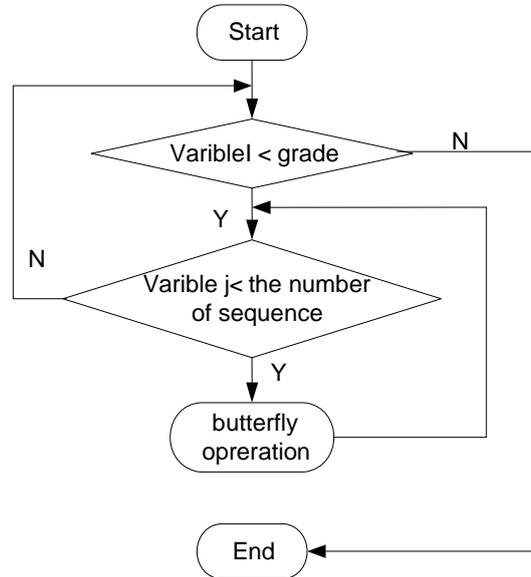


Figure 7. The flow chart of butterfly algorithm

#### 4.1. Fast Wavelet Transform (Mallat)

The application of wavelet transformation is tightly connected to the theoretical research of wavelet transformation analysis. Presently, DSP technology is one of the most important components of the modern science and technology. The main purposes of the signal processing are, to precisely analyze and diagnose, encode and compress, quantize and transmit the signal quickly and accurately. Mathematicians are of the view that the disposition of both signals and images should be considered as the signal processing (images can be treated as two-dimensional signal). Because of this we can attribute several applications of wavelet operation to the problems of signal processing. However, the ideal tool for some signals, for which the properties stay steady beyond time, is still Fourier analysis. In reality, however, almost all of the signals are unsteady in practical use. The wavelet operations are particular cases of the whole unsteady signals.

Suppose  $W_j$  is the complementary space of  $V_j$ , that is to say,  $V_{j-1} = V_j \oplus W_j, V_j \perp W_j \Rightarrow W_j = V_{j-1} - V_j$ , every  $W_m$  and each  $W_n$  is mutually orthogonal, namely  $W_m \perp W_n, m \neq n$ , so a series of orthogonal subspaces of  $L^2(R)$  have been composed by  $L^2(R) = \bigoplus_{j \in Z} W_j, \{W_j\}_{j \in Z}$  [9], and  $f(t) \in W_0, f(2^{-j}t) \in W_j$  existed.

Suppose  $\{\psi_{0,k}; k \in Z\}$  is a group of orthogonal basis in space  $W_0$ , and  $\psi(t)$  meets the allowance conditions, then every  $j \in Z, \{\psi_{j,k}; k \in Z\}$  will be a group of orthogonal basis in space  $W_j$ , so the whole  $\{\psi_{j,k}; j \in Z, k \in Z\}$  will be a group of orthogonal basis of  $L^2(R)$ .  $\psi(t)$  is a wavelet function,  $W_j$  is regarded as wavelet space at scale  $j$  [10].

Tower fast disintegration formulas of Mallat are below:

$$\begin{cases} c_{j+1,k} = \sum_m h_0(m-2k)c_{j,m} \\ d_{j+1,k} = \sum_m h_1(m-2k)c_{j,m} \end{cases} \quad (7)$$

The formula of disintegration and reconstruction is shown below:

$$c_{j-1,k} = \sum_m h_0(k-2m)c_{j,m} + \sum_m h_1(k-2m)d_{j,m} \quad (8)$$

The diagram of disintegration and reconstruction of multi-resolution is shown as Figure 5.

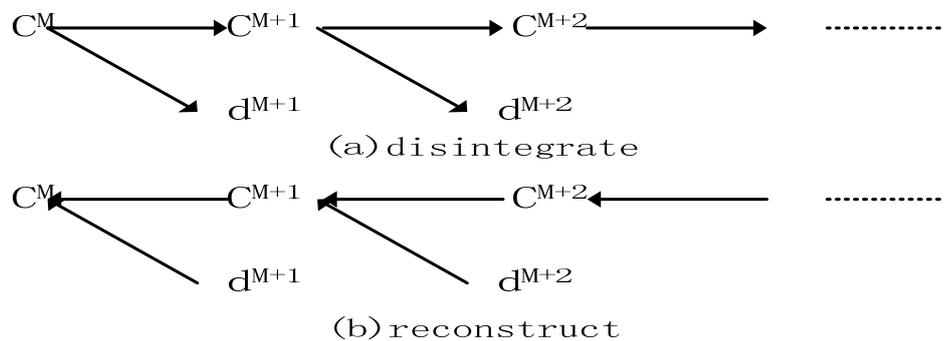


Figure 5. The picture of disintegration and reconstruction

The designing-accuracy of high-voltage impulse receiver is closely connected to the security of moving trains and people's life and properties. Therefore we have to ensure high accuracy and low failure of the receiver. This type of algorithm can run under the circumstance of AVR Studio but the running result is not intuitive, so the program is implanted into Visual Studio 2010 and compared to the result obtained by MATLAB. The length of FFT sequence N is set as 256. Chart 2 is a list of compared results of FFT and Mallat after being allowed to run in Visual Studio 2010 and MATLAB.

Chart 2. The results of comparing FFT and Mallat separately in VS2010 and MATLAB

FFT	Visual Studio 2010	MATLAB	Mallat	Visual Studio 2010	MATLAB
X(0)	36.000000+0.000000j	36.0000	desh[0]	4.760300	4.7603
X(1)	-4.000000+9.656854j	-4.0000+9.6569i	desh[1]	7.588700	7.5887
X(2)	-4.000000+4.000000j	-4.0000+4.0000i	desh[2]	10.417100	10.4171
X(3)	-4.000000+1.656854j	-4.0000+1.6569i	desh[3]	2.689500	2.6895
X(4)	-4.000000+0.000000j	-4.0000	desg[0]	0.000100	0.0001
X(5)	-4.000000-1.656854j	-4.0000-1.6569i	desg[1]	0.000100	0.0001
X(6)	-4.000000-4.000000j	-4.0000-4.0000i	desg[2]	0.000100	0.0001
X(7)	-4.000000-9.656854j	-4.0000-9.6569i	desg[3]	2.828100	2.8281

## 5. AD Program Implementation

The system needs to compare the results which are verified by VS2010 with output after simulation of ATmega128 microcontroller, whose main function is to implement AD conversion. The detailed process is introduced as following [11].

The AD conversion is set at 64 frequency divisions and adopts the microcontroller which has 8MHz crystals. After frequency divisions the crystals become 125 KHz. The system counts time once AD conversion begins. We have to sample the inputted pulse signal in order to know how long it takes for a complete cycle of AD conversion to be completed and also the time taken for it to be restarted [12].

The timepiece is designed to adopt 256 frequency divisions. In other words, the counter will increase by one after 32us. A complete turn of conversion time is listed as  $32 \times 6 = 192\text{us}$ . The cycle of high-voltage signal is 1/3s. We should only take samples at 256 points since the storage of microcomputer is rather limited. In this case, samples may be taken at every 1302us and the delay is listed as  $1302 - 192 = 1110\text{us}$ .

We should set a standard, which may be obtained from MATLAB, for comparing the converted results of two CPUs since the two algorithms are totally different and then output the compared results. The AD conversion in AVR has a 10-bit precision, with the maximum conversion value being 1023 and 0 being the minimum value. The pulse signal that is generated by MATLAB ranging from 0 to 1023 replaces the value converted in AD which makes it possible for the pulse signal to be transformed by both FFT and Mallat. Place 256 values into an array of the microcontroller in accordance with the same proportion of values in the microcontroller and compare the results of AD conversion and FFT and Mallat. There is a "check" function used to compare results in AVR. If the results are consistent, then the output of the seventh pin of PB should be higher than the usual result.

## 6. Conclusion

The design of high-voltage pulse track circuit receiver has solved problems such as the safety of train operation and the security of signaling interlocking systems. It adopts a redundancy approach by installing two sets of CPUs which obviously improves the reliability and safety of equipments. Meanwhile, the entire open-loop system is also designed as a closed-loop detection system merely for the principle of fail-safe. It meets the requirements for railway signal communication system. The paper has vividly accomplished the works, presented as followings:

- 1) Employing AVR as the core hardware, where CPU processes and analyzes the high-voltage pulse signal has greatly increased the system's ability to resist disturbance and improve precision.
- 2) Using redundancy of hardware and heterogeneous software.
- 3) The simulating circumstance of high-voltage pulse signal is MATLAB and the use of Butterworth low-pass to filter out 50Hz traction current. In other words, hardware redundancy which adopts two types of CPU, outputs dynamic square wave when the two CPUs' computed results are consistent. Heterogeneous software, which uses two kinds of algorithms, displays the final result when compared with the standard set before.
- 4) Analyzing and optimizing the ability to resist 50Hz power frequency interference has effectively boosted the anti-interference of the receiver.

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