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A low-power high speed full adder cell using carbon nanotube field effect transistors

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ABSTRACT

The adder circuit is basic component of arithmetic logic design and that is the most important block of processor architecture. Moreover, power consumption is the main concern for real-time digital systems. In recent times, carbon nanotube field effect transistors (CNTFET) used for arithmetic circuit designs with high performance. A creative substitute for highspeed, less power, and small size in area designs is the CNTFET. This paper presents 1-bit full adder with CNTFETs for low power and high performance. Using the computer aided design (CAD) tool the proposed 1-bit full adder design model is simulated using 32 nm with CNTFET technology, a voltage supply of +0.9V. Performance comparisons between various proposed designs and existing 1-bit full adder design have been made in terms of the delay, power, and power delay product (PDP). The proposed CNFET logic also design for n-bit carry look adder (CLA) and compare it to other CLAs to evaluate performance and reliability. The simulation results shows that the proposed adder consume less power than existing adders.

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1. INTRODUCTION

Short channel effect, increased leakage power, limited gate control, and parameter fluctuations are a few of the issues that have arisen as a result of shrinking metal oxide semiconductor (MOS) transistor size. The scaling down of MOS transistor forcing designers to switch to new competitive methods instead of metal oxide semiconductor field effect transistors (MOSFETs). In order to perform various complex applications like digital image processing, digital signal processing, and graphics processing units, a more number of transistors must be integrated on a one chip [1]. Max speed, low energy consumption, great chip density, and high efficiency are also requirements for these applications. The best solution, in accordance with Moore's law, was thought to be scaling down the circuits [2]. The technology encounters challenges like decreased gate controllability, short channel effect, andhot electron effect. One of the technologies that has sparked the development of additional technologies for making low-power, low-delay designs is the MOSFET [3]. There are benefits and drawbacks to every technology [4], [5].

Industrial researchers are motivated by this to create alternative materials, technologies, and devices [6], [7]. Carbon nanotube field effect transistors (CNTFETs) are flexible to scale and face challenges like short channel effect, hot electron effect, and drain induced barrier lowering (DIBL) [8]-[12]. Currently, one of the

effective and promising options to MOSFET technology is these devices. A basic digital circuit known as a full adder adds two input bits and outputs carry and sum. Any digital circuit must utilise a full adder circuit [13]. Utilizing different adder implementations can improve device performance and boost the performance of digital circuits [14]. There are several full adder implementations that have been published that aim to increase performance, such as conventional complementary metal oxide semiconductors (C-CMOS) and transmission gate array (TGA) [15], transmission function array (TFA) [16], transmission gate array (TGA) [17], complementary pass transistor logic (CPL-TG) [18], full mirror adder SERF [19], 13A full adder [20], static energy recovery full adder [21], static CMOS output device and hybrid pass transistor logic (HPSC) level-restoring, complementary, and new-(HPSC) carry logic (CLRCL) [22], double pass transistor logic [23], and hybrid CMOS logic with transmission gate logic (HCTG) [24], removed single driving full adder (RSD-FA) [25], 18 transistor 1-bit full adder (18T-FA) [26], hybrid multi threshold fault adder (HMTFA) [27], and carbon nanotube full adder (CNTAFS) [27].

2. LITERATURE REVIEW

The steady increase in performance requirements and the complexity of applications are the primary causes behind the development of conventional very large scale integrated circuit design and cutting-edge implementation techniques. Regardless of the applications, hard computing always adheres to strict accuracy standards. Due to the requirement for maintaining accuracy throughout the design process, implementation prices rise; also, new, emerging applications encounter considerable challenges. The fundamental building blocks of all computing systems are arithmetic circuits. The researchers are used various full adder designs with different transistor technologies and various existing implementation of full adders summarized as shown in Table 1.

Table 1. Existing implementation of full adders with various technologies

Ref.	Transistor technology	Number of transistors	Critical data path delay of transistors	Merits	De-Merits
Weste and Eshraghian [1]	C-CMOS	28	5	It produces full swing output voltage without inverted inputs.	Largest propagation delay, Low sensitivity.
Weste and Eshraghian [1]	TGA	20	4	Full adder required less area and avoid short circuit of current.	Lack of driving capabilities for large fan out for cascading stages.
Zhuang and Wu [2]	TFA	16	4	No of transistors used is less and Power consumption is also reduced.	Suffers in its driving capabilities for large fan out for cascading stages.
Abu-Khater *et al.* [3]	CPL-TG	36	3	Better driving capabilities for large fan out for cascading stages.	More number of transistors required and area is more.
Zimmermann and Fichtner [4]	M-Full adder	28	4	It produces full swing output voltage.	High response time and more number of transistors.
Shalem *et al.* [5]	SERF	10	3	Less number of transistors, required less area.	Suffers from threshold loss.
Bui *et al.* [6]	13A Full Adder	10	3	Power consumption is high and not full swing output voltage.	Effect with threshold loss.
Chang *et al.* [7]	HPSC	26	4	Feedback loop transistors are used to eliminate threshold loss.	Due to inverters, power consumption is increased.
Goel *et al.* [8]	N-HPSC	24	4	Less no of transistors required compared to HPSC.	Power consumption is increased.
Lin *et al.* [9]	CLRCL	10	3	Design used only10 transistors required less area, less supply and full swing output voltage.	Power consumption is increased with inverter circuits.
Aguirre-Hernandez and Linares-Aranda [10]	DPL	28	3	It provides Full output swing voltage with the presence of transmission gates.	Suffers in its driving capabilities for large fan out for cascading stages, Area is high.
Bhattacharyya *et al.* [11]	HCTG	16	4	Design offers high speed with low power consumption.	Poor driving capabilities for large fan out for cascading stages.
Mehrabani and Eshghi [12]	RSD-FA	26	4	Exhibits full driving capabilities and Low power consumption	More number of transistors required
Saini *et al.* [13]	18T-FA	18	4	Average power consumption is less compare to HPSC, CPL, C-CMOS and TGA and PDP is less to C-CMOS, HPSC, TGA but higher than CPL	Delay is more compare with CPL and C-CMOS
Maleknejad *et al.* [14]	HMTFA	23	4	It provides full output swing voltage	Threshold problem due to more number of inverters
Ghadiry *et al.* [25]	CNTAFS	20	4	It consumes less power	Threshold problem due to more number of inverters

3. HISTORY OF CARBON NANO TUBE FIELD EFFECT TRANSISTORS (CNTFET)

In contrast to conventional field-effecttransistors like MOSFETs, which use bulk silicon as the channel, CNTFETs us semiconducting "carbon nano tubes (CNTs) as the channel". This is seen in Figures 1 and 2. These CNTs, which are shaped into tubes and typically have one wall that is just one atom thick, share the same atomic structure as graphite. Though they work similarly to a MOSFET, they have been demonstrated to have significant performance advantages [15], which may allow for more compact central processing unit (CPU) architectures like three dimensional-very large scale integration (3D-VLSI) [16]. Since a CNT acts as aone-dimensional electron channel, there is no electron scattering [17]. In comparison to bulk silicon, CNTs have some advantages, such as a higher threshold voltage and sub-threshold slope, higher electron mobility because of the one-dimensional structure of the mono-atom thick nanotube, higher current density, higher linearity in the voltage-current relationship, and higher transconductance [18], [19]. Different chemical doping in the channel can produce n-type and p-type transistors, which are similar to MOSFET transistors [21].

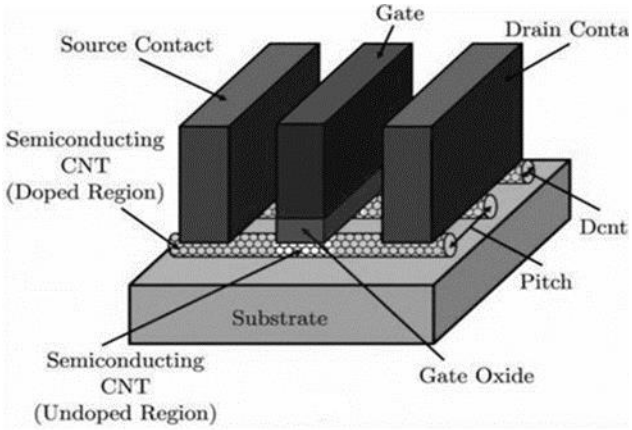

Figure 1. Typical CNTFET

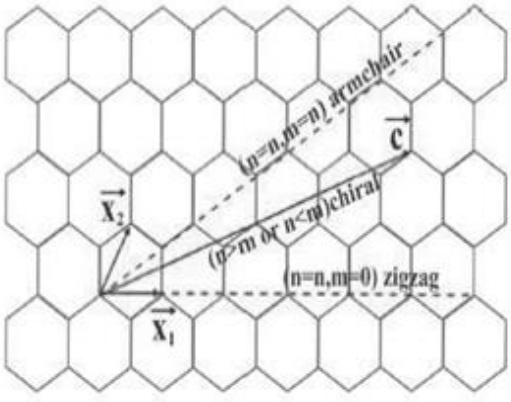

Figure 2. Representation of chiral vector

Carbon nanotubes are carbon allotropes with cylindrically rolled-up graphite-like structural characteristics. They also display characteristics of semiconductors and metals. The property under consideration will affect the classification in Table 2. For instance, they can be classified into Armchair, Zigzag, and Chiral types [20]-[25] based on their structural make-up. Additionally, layering is used to categories structural types; thus, a structure may be in mono-walled or multi-walled. They can exhibit the characteristics of either a metal or a semiconductor due to their capacity to reach the aforementioned configuration [23], [27]. As shown in Figure 2 and quantified by the chirality vector (C), which is defined by (1), these connections between sheets are measure:

$$C = nX1 + mX2 \quad (1)$$

the final structure depends on the relationship between (n, m); for instance, if n=m, the structure is an arm chair; if n=m and m=0, it is a zigzag; and if n>m or n m, it is chiral [24]. In (1), the unit vectors are x1 and x2. The suggested circuit is created using the zigzag structure, with n=19 and m=0. (19, 0) [25], [26].

It has been used in the implementation of logic circuits due to M-operational CNTFET's and intrinsic similarities to MOSFET [26], [27]. In (2) can be used to approximation the CNTFET gate width:

$$W \approx min\ (W_{min}, N \times S) \quad (2)$$

half of the band gap of a CNFET is given as the threshold voltage for SB-CNFETs and MOS-CNFETs [27],

$$Vth = Ebg/2e = 0.436/DCNT\ (nm) \quad (3)$$

where DCNT is the diameter of the nanotubes, e is the electron charge, and Ebg is the band gap of the CNFET. In (3) illustrates the connection between the energy band gap and the threshold voltage. In (4) shows the connection among DCNT, n, and m.

$$Dcnt = \frac{\sqrt{3}do}{\pi}\sqrt{n^2 + m^2 + nm} \quad \text{nanometer} \tag{4}$$

The electrons are parallel to the atomic plane for the carbon allotrope, where they are present in a sorted array [22]-[25]. These electrons can only travel in a direction parallel to the tube axis due to structural alignment restrictions.

Table 2. CNTFET parameters, values and their description

CNTFET description	CNTFET parameter	Value
Gate supply voltage	Supply	0.9
Physical channel length	Lch	3.20E-08
The S/D tube's doped Fermi level	Efi	0.6
In the intrinsic CNT channel, the mean free path	Lgeff	1.00E-07
The size of the source-side extension of doped CNT	Lss	3.20E-08
Gate oxide dielectric constant	Kox	16
How far the doped CNT drain-side extension extends	Ldd	3.20E-08
Number of CNTs	Tubes	3
Temperature	Temp	25
The capacitance between the channel and substrate	Csub	4.00E-11
The high-k top gate dielectric material's thickness	Tox	4.00E-09
The distance between the centers of two adjacent CNTs	Pitch	2.00E-09

4. PROPOSED FULL ADDER

A digital logic circuit known as a full adder performs arithmetic sum. Adders are a fundamental component of on-chip libraries and are used to compute table indices, ads, and other related operations. By adding the two input operands (A, B) and previous stage carry, a complete adder produces a resulting sum and carries output (Cin). In Figure 3, a block diagram of a 1-bit complete adder is presented [23], [27].

In (5) and (6) provide expressions for the relationship between input and output bits, respectively. In Table 3 a 1-bit complete adder's truth table is displayed. SUM and CARRY are the outputs, where Cin stands for any carry input and both A and B are the inputs. Figure 4 depicts the suggested 10 transistor full adder circuit using CNFET technology. The proposed 10T-FA circuit features a three-delay critical route and offers complete output voltage swing as shown in Figure 5.

$$\text{SUM} = \text{A xor B xor C} \tag{5}$$

$$\text{CARRY} = (\text{A and B}) \text{ or C } (\text{A xor B}) \tag{6}$$

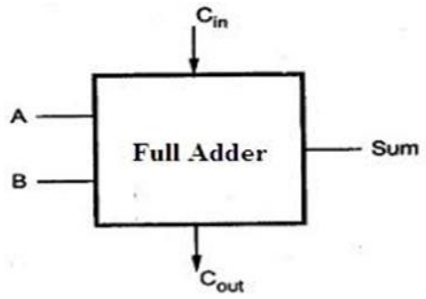

Figure 3. Block diagram of 1-bit full adder

Table 3. TruthTable of 1-bit full adder

A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

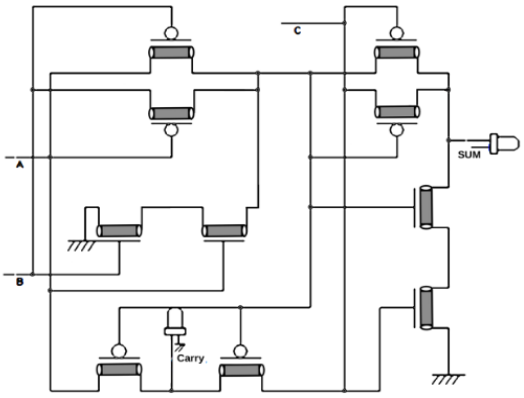

Figure 4. Proposed full adder using 10 CNTFET

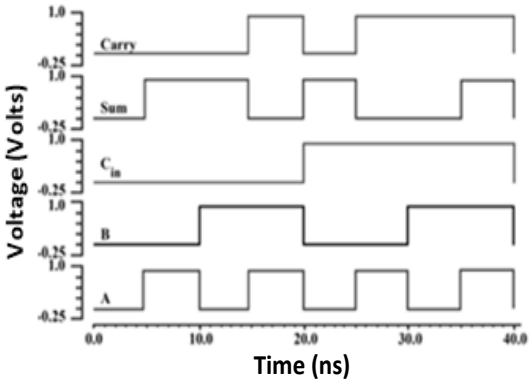

Figure 5. Output response of 10T-FA by CNTFET

5. SIMULATION RESULTS

Using 32 nm CNFET technology, the proposed 1-bit full adder was simulated for the suggested designs using the Cadence Virtuoso computer aided design (CAD) tool at supply voltage +0.9 V, threshold voltage Vth=0.289 V, and chirality vector (19, 0). The additional simulation tool configuration parameters are listed in Table 2. The average power and delay, and power delay product simulation results are listed in Table 4. Table 4 shows that power delay product (PDP) rises in tandem with rising VDD. Regarding the components power and delay, and power delay product, the proposed 10T-FA circuit out performs the conventional circuit by 69.2, 71.2, and 68.2%, respectively as shown in Figures 6 and 7. Table 4 compares the power, delay, PDP.

Table 4. Comparison of full adder's performance with various technologies

1 bit full adder designs	Transistor count	Power (µW)	Delay (ps)	PDP (aj)
C-CMOS [1]	28	0.124	12.355	1.532
CPL-TG [3]	36	0.139	14.26	1.982
TGA [1]	20	0.135	10.104	1.364
13A [6]	10	5.819	9507.8	55325.9
SERF [5]	10	3.326	9852.7	32770.1
RSD-FA [12]	26	0.091	9.427	0.857
TFA [2]	16	0.109	11.701	1.275
CLRCL [9]	10	5.903	231.18	1364.65
18T-FA [13]	18	0.088	8.93	0.785
Hybrid PSC [7]	26	0.095	30.454	2.912
NEW-Hybrid PSC [8]	24	0.123	30.132	3.718
Mirror [4]	28	0.126	12.321	1.552
HCTG [11]	16	0.124	12.116	1.502
Hybrid-MTFA [14]	23	0.121	16.709	2.026
Proposed 10T-FA	10	0.029	5.876	0.258

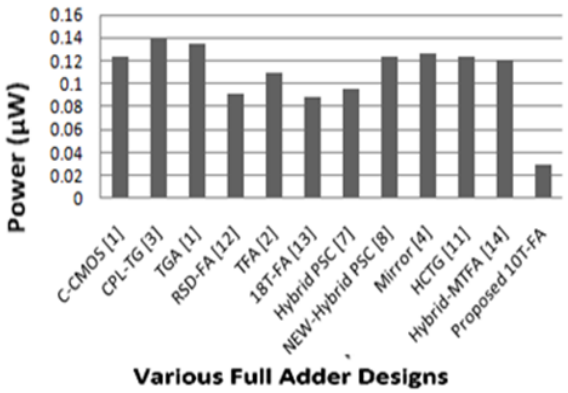

Figure 6. Analysis of FA performance for power

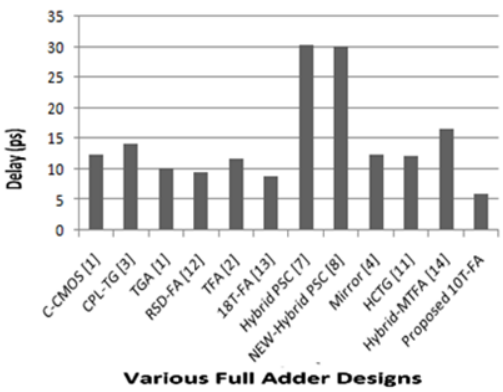

Figure 7. Analysis of FA performance for delay

6. IMPLEMENTATION OF CLA USING CNTFETs BASED 4-BIT FULL ADDERS

Development and comparison of carry look adder (CLA) for n=4, 8 is done. Table 5 verifies these findings, and Figures 8 and 9 show how various CLAs perform in regard to latency, power, and PDP. The analysis of full adder performance for power and delay are shown in Figures 10 and 11.

Table 4 displays the comparative evaluation of the potential designs. Additional information in Table 5 demonstrates that the average power usage is 0.099 µW, the power-delay product is 2.407 aJ, and the delay in 4 b-CLA is 24.121 ps. These findings categorically demonstrate that the suggested 1-bit full adder architecture is better than those already in use.

Table 5. Analysis of full adder design with VDD supply +0.9 V

FA design technology	4b full adder			8b full adder		
	Power (µW)	Delay (ps)	PDP (aj)	Power (µW)	Delay (ps)	PDP (aj)
C-CMOS [1]	0.184	33.881	6.258	0.33	67.337	22.251
TGA [1]	0.224	46.391	10.399	0.645	158.23	102.139
TFA [2]	0.215	85.345	18.414	0.651	424.54	276.511
CPL-TG [3]	0.309	39.342	12.159	0.564	77.269	43.623
MIRROR [4]	0.185	32.498	6.015	0.327	62.766	20.535
HPSC [7]	0.28	119.63	33.568	0.513	241.92	124.204
NEW-HPSC [8]	0.299	130.7	39.091	0.574	279.19	160.352
OURS1 [10]	0.241	89.685	21.645	0.596	396.18	236.162
HCTG [11]	0.201	51.467	10.365	0.552	195.42	107.94
RSD-FA [12]	0.179	29.141	5.236	0.306	59.552	18.28
18T-FA [13]	0.156	27.93	4.35708	0.303	51.69	15.66207
HMTFA [14]	0.218	35.15	7.6627	0.411	72.69	29.87559
Proposed 10T-FA	0.099	24.121	2.407	0.213	35.2.634	7.582

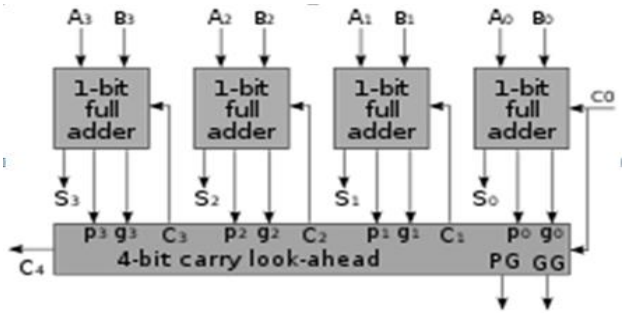

Figure 8. Implementation of 4-bit CLA with full adder

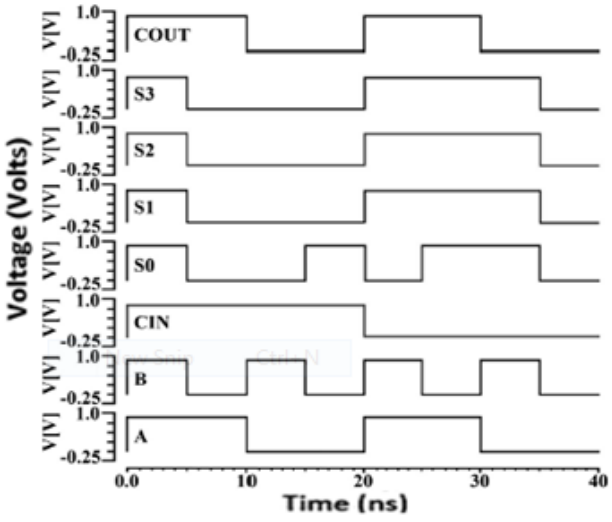

Figure 9. 4-bit CLA with full adder response

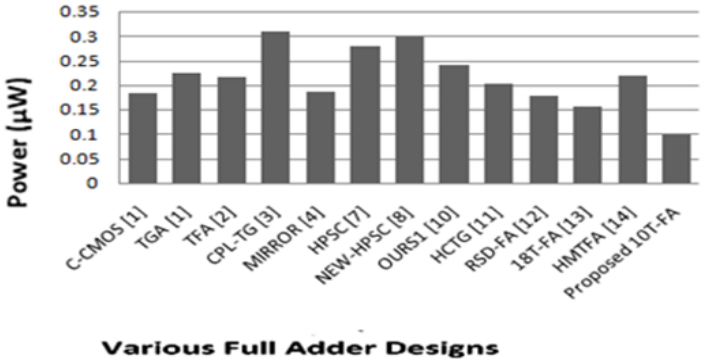

Figure 10. Analysis of full adder performance of power for 4-bit FA

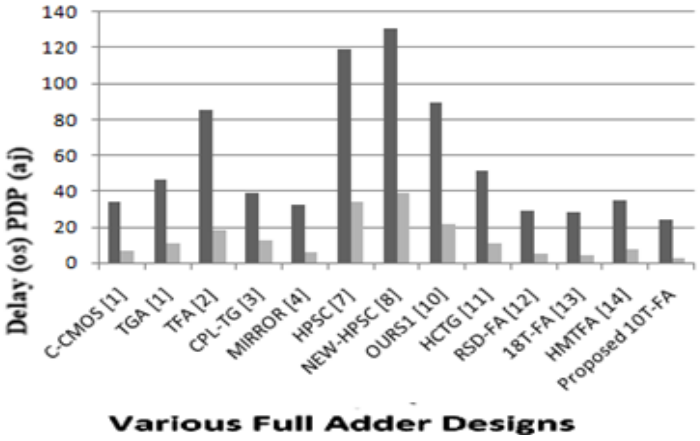

Figure 11. Analysis of full adder performance of delay for 4-bit FA

7. LAYOUT OF PROPOSED FULL ADDER USING 10 CNTFET

Layout designs are designed through using the dsch2 and micro wind software. The layouts are designed for the suggested 10 T full adder to find area. The proposed full adder design required only 10 transistors, provides full swing output voltage, avoid threshold voltage drop and improve the driving capabilities for cascading stages as shown in Figure 12.

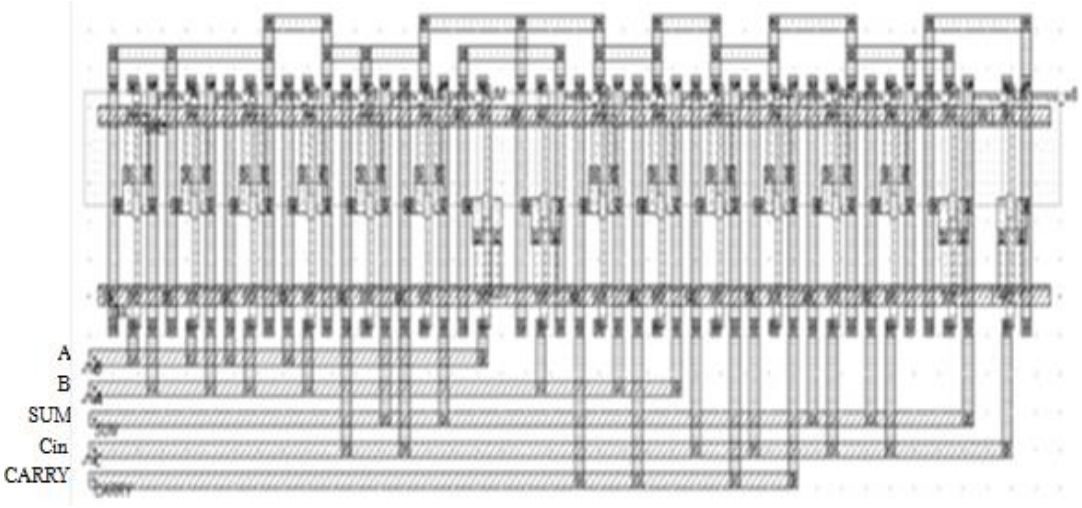

Figure 12. Layout of proposed full adder using 10 CNTFET

8. CONCLUSION

In this paper, a 1-bit full adder and carry look adder were implemented using CNTFETs with minimum number of transistor count. The suggested design outperformed the earlier full adder designs, according to specifications related to power, delay, as well as the power delay product. The observation showed that the simulations' results further confirmed the conclusions that the average power would drop as the amount of transistors increased. Therefore, the proposed 1b-FA10 has been used to design the 4b-CLA. The suggested circuit 1b-FA10 had an overall power requirement of 0.062 W and a measured delay of 5.876 ps, according to simulation findings utilizing 32 nm CNTFET technologies. The efficient usage of powerful computational design, arithmetic, and logical unit cores. Is made possible by the recommended 1b-FA10 design, which may be used instead of MOSFET design. The simulation results of 1-bit full adder and carry look adder shows that the CNTFET technologies mostly suitable for low power applications.

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