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Single-phase grid-connected power control in dq synchronous reference frame with space vector modulation using FPGA

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ABSTRACT

This paper presents the performance of controlling the active and reactive power of single-phase grid connected inverter by dq synchronous reference frame and space vector modulation (SVM) which is implemented by using field programmable gate array (FPGA) due to the flexibility they offer in comparison to other digital signal processors, hence it become the standard instruments for implementing various types of pulse width modulation (PWM) digital signal processors (DSPs). The SVM method has used because of its superiority in terms of harmonic distortion, switching losses and utilization of direct current (DC) bus. The synchronization is achieved by using second order generalized integrator (SOGI) due to its simple structure, certain filtering ability and frequency adaptability, in which the phase locked loop (PLL) ensures high performance for single-phase inverter. The active and reactive inverter current has been controlled and decoupled from each other and the dynamic response has been improved and became fast with proper feed-forward and decoupling grid voltage term. The system has simulated by MATLAB and the result shows robust control of injected grid current, active and reactive power control and DC link voltage control.

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1. INTRODUCTION

Single-phase voltage source inverters with regulated current are used widely in many grid-integrated systems, such as applications of photovoltaic power system, active power filter, controller of power factor. Recently, there is intense to use such converter due to high penetration of distributed energy sources. The inverter is connected to the grid through certain type of filter such as L, LC or LCL filter, and the control strategy of the current is adopted to control the injected current to the grid. Meanwhile, the direc current (DC) link voltage is controlled with control loop relatively slower than that of current control loop [1]–[4]. Proportional integral (PI) based current controller is employed to control the single-phase grid-connected inverter due to its great advantage of providing infinite gain at the steady-state operating point, which gives zero steady-state error. However, this type of controller can not be implemented directly for single-phase grid-connected inverter, where it is required to create a second quantity that would be in quadrature with the available physical one [5]–[10].

Many technical literatures have attempted to obtain the orthogonal quantity. In this paper, second order generalized integrator (SOGI) provide the dq components and it provides the required transformation angle from αβ to dq, thus it serves as phase-locked loops (PLL) at the same time. The orthogonal inverter current quantity is obtained by using orthogonal signal generator (OSG), which is phase shift circuit that would

shift the variables by quarter cycle of the fundamental period. The obtain of orthogonal quantity would deteriorate the system dynamic response, but as long as the SOGI-PLL has filtering stage within its system, the deteriorating effect could be managed [11], [12].

This paper introduces the performance control of active and reactive power per requirement for single-phase grid-connected inverter, where the vector control of active and reactive inverter power is controlled by decoupling the inverter active and reactive current. The deterioration caused by obtaining the orthogonal signal is cope with SOGI-PLL which improve the system dynamic even if the grid voltage is weak. The DC link voltage has controlled as well. The utilization of DC bus is achieved by employing space vector modulation (SVM) techniques for inverter switches operation, moreover the switching losses are reduced. The field programmable gate array (FPGA) is employed to implement the SVM, and the result would be similar to that of simulation by MATLAB. In addition to the effect of SVM which reduce the harmonics, an LCL filter is used to obtain current with reduced total harmonics distortion (THD).

2. CURRENT CONTROL IN DQ REFERENCE FRAME

The injected current from the inverter and grid voltage must be in phase to deliver active power to the grid, and this phase would change according to the reactive power whether it is injected to the grid or absorbed from the inverter. The grid voltage and inverter current are transformed from the stationary reference frame to the synchronous reference frame, where the control would be applied. The transformation to $\alpha\beta$ frame is achieved by using SOGI and then apply Park transformation and the required angle θ_{PLL} for the transformation is provided from the SOGI-PLL. Assume the grid voltage V_{grid} is given by (1).

$$V_{grid} = V_{max}\, sin\,(\omega t) \tag{1}$$

The orthogonal αβ pairs of the grid voltage would be:

$$V_{g\alpha}(t) = V_{max}\, cos\,(\omega t) \tag{2}$$

$$V_{g\beta}(t) = V_{max}\, sin\,(\omega t) \tag{3}$$

where ωt and V_{max} are the angular frequency of grid voltage and maximum voltage of the grid respectively. The orthogonal pairs of inverter current $I_{inv-\alpha}$ and $I_{inv-\beta}$ are given as:

$$I_{inv-\alpha} = I_{max}\, cos\,(\omega t + \varphi) \tag{4}$$

$$I_{inv-\beta} = I_{max}\, sin\,(\omega t + \varphi) \tag{5}$$

where φ is the phase angle of inverter current and I_{max} is the peak value of inverter current. With Park transformation for inverter current, the dq components are obtained and they represent DC component, thus PI controller could be employed which gives zero steady-state error [13].

$$\begin{bmatrix} I_d \\ I_q \end{bmatrix} = \begin{bmatrix} cos\theta_{PLL} & sin\theta_{PLL} \\ -sin\theta_{PLL} & cos\theta_{PLL} \end{bmatrix} \begin{bmatrix} I_\alpha \\ I_\beta \end{bmatrix} \tag{6}$$

$$\begin{bmatrix} I_d \\ I_q \end{bmatrix} = \begin{bmatrix} I_{max}\, cos(\varphi) \\ I_{max}\, sin(\varphi) \end{bmatrix} \tag{7}$$

Where θ_{PLL} is the estimated phase angle from the SOGI. If it is required to deliver active power to the grid, the phase angle (φ) should be zero, therefore the above equation become:

$$\begin{bmatrix} I_d \\ I_q \end{bmatrix} = \begin{bmatrix} I_{max} \\ 0 \end{bmatrix} \tag{8}$$

when PI controller is applied, the error signal is given as (9).

$$e_d(t) = I_{d-ref} - I_d \tag{9}$$

$$e_q(t) = I_{q-ref} - I_q \tag{10}$$

The I_{d-ref} is the active current component and it is provided from the inverter DC link voltage controller. This current is responsible for developing the active power P and delivering it to the grid. I_{q-ref} is the current which controls the reactive power Q and it is obtained from (11) and (12) [14].

$$P = V_d I_d + V_q I_q \tag{11}$$

$$Q = V_q I_d - V_d I_q \tag{12}$$

The V_q is set to zero, therefore $Q = -V_d I_q$ is used to obtain the I_{q-ref} [6], [15]. The voltage and current equations of single-phase grid connected inverter in dq rotating reference frame are expressed as follows; it should be mentioned that the capacitor filter is neglected due to its' high impedance at the fundamental frequency [3], [16].

$$V_{inv} = Ri_{inv} + L\frac{di_{inv}}{dt} + V_{grid} \tag{13}$$

By applying the transformation to dq rotating reference frame, the dynamic modelling in dq frame is based on:

$$V_{inv-d} = Ri_{inv-d} + L\frac{di_{inv-d}}{dt} - \omega L\, i_q + V_{grid-d} \tag{14}$$

$$V_{inv-q} = Ri_{inv-q} + L\frac{di_{inv-q}}{dt} + \omega L\, i_d + V_{grid-q} \tag{15}$$

where $R = R_g + R_i$ and $L = L_g + L_i$, R_g and R_i are the grid and inverter side resistance respectively and L_g is the grid side inductance, while L_i is the inverter side inductance [7], [14]. On the controller side, the dq decoupled condition is given as:

$$V_{inv-d} = Ri_{inv-d} + V_{grid-d} - \omega L\, i_q + (K_p + \frac{K_i}{s})(I_{d-ref} - I_d) \tag{16}$$

$$V_{inv-q} = Ri_{inv-q} + V_{grid-q} - \omega L\, i_d + (K_p + \frac{K_i}{s})(I_{q-ref} - I_q) \tag{17}$$

K_p and K_i are the proportional and integral gain of the PI controller. With this, the control grid current I_d is decoupled from I_q and vice versa and these currents are the input to decoupled control system. In the decoupled system, the active power is directly proportional to I_d and reactive power is proportion to I_q, and the sinusoidal grid voltage is considered the reference. By applying inverse Park transformation, the $V_{\alpha\beta}$ reference is obtained for the PWM operation [13], [17]–[19]. Figure 1 is the simulated system in this paper and it shows the items that would be controlled.

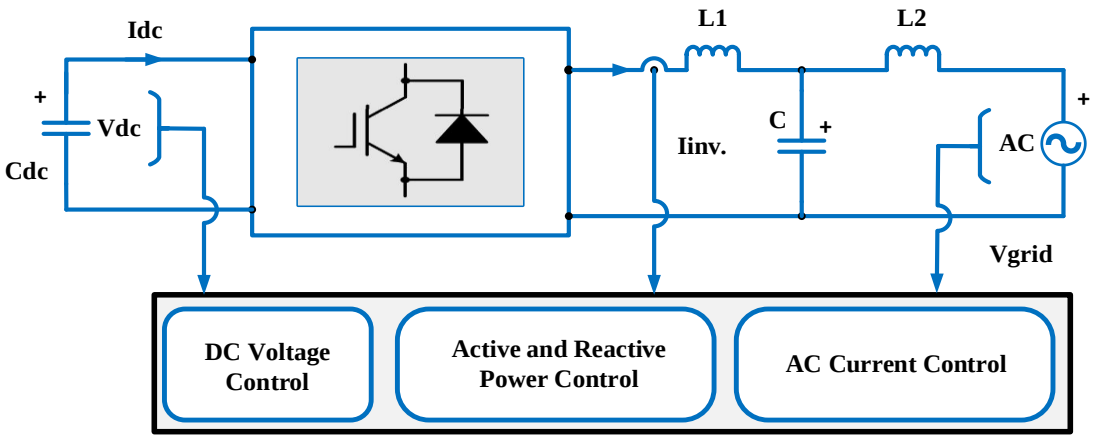


Figure 1. Simplified control diagram of single-phase grid-connected inverter

3. SOGI-BASED SINGLE-PHASE PHASE-LOCKED-LOOPS FOR GRID SYNCHRONIZATION

SOGI-PLL structure is shown in Figure 2. Where the input is the grid voltage V_{grid}, the ω_{ff} is angular frequency and it is $2\pi 50\ rad/sec$, and the control loop provide the estimated phase angle θ_{PLL} and angular frequency ω_{PLL}. A pair of orthogonal signals are generated by the SOGI, which are V_α and V_β and this is shown in Figure 2. These signals are transformed by Park transformation to obtain V_d and V_q as shown in (18).

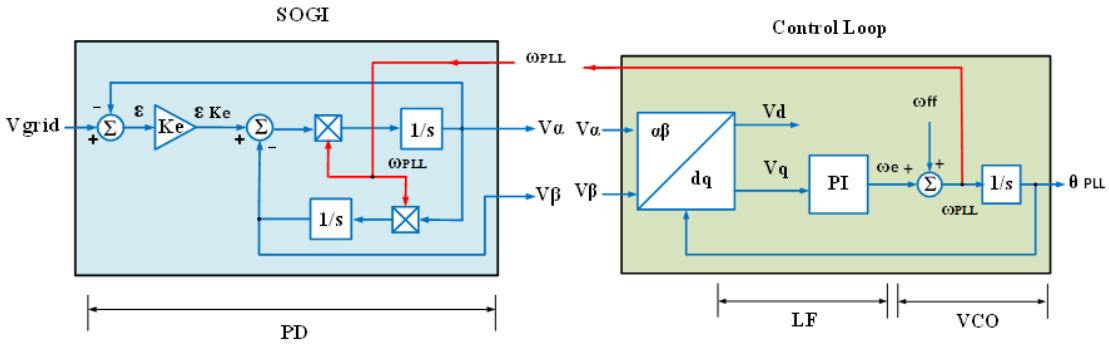


Figure 2. General structure of creating orthogonal signal for single-phase system

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} cos\theta_{PLL} & sin\theta_{PLL} \\ -sin\theta_{PLL} & cos\theta_{PLL} \end{bmatrix} \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} \tag{18}$$

Assume that the grid voltage V_{grid} is sinusoidal and represented by $V_{grid} = V_m\ cos\theta_g$. The SOGI output would provide two signals having the same amplitude of grid voltage V_{grid}, but with 90° phase shift between each other. As shown in (18) can be rewritten as (19).

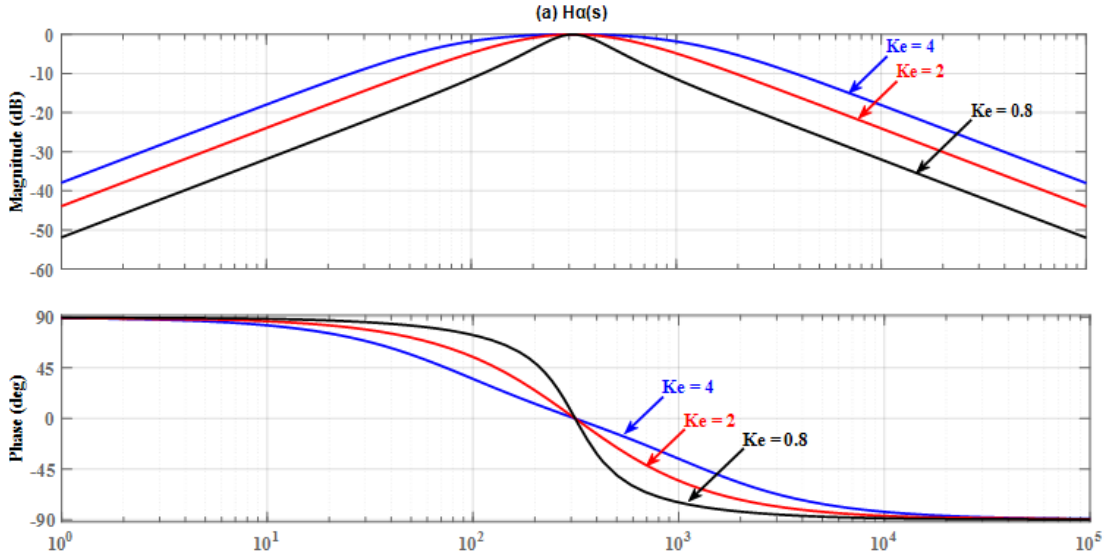
$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} V_m\ cos\ (\theta_g - \theta_{PLL}) \\ V_m\ sin\ (\theta_g - \theta_{PLL}) \end{bmatrix} \tag{19}$$

From (19), it has noticed that the amplitude information of the grid voltage is included in V_d and the phase error information is contained within V_q. Thus, the estimated phase angle θ_{PLL}, which is equal to the grid phase angle could be obtained, and this is achieved by using PI controller that serves as loop filter (LF) to regulate V_q to zero value and then send the error to voltage controlled oscillator (VOC) which is represented by integrator as shown in Figure 2. The transfer function from V_{grid} to $V_{\alpha\beta}$ could be obtained with the help of Mason formula [5], [20], [21].

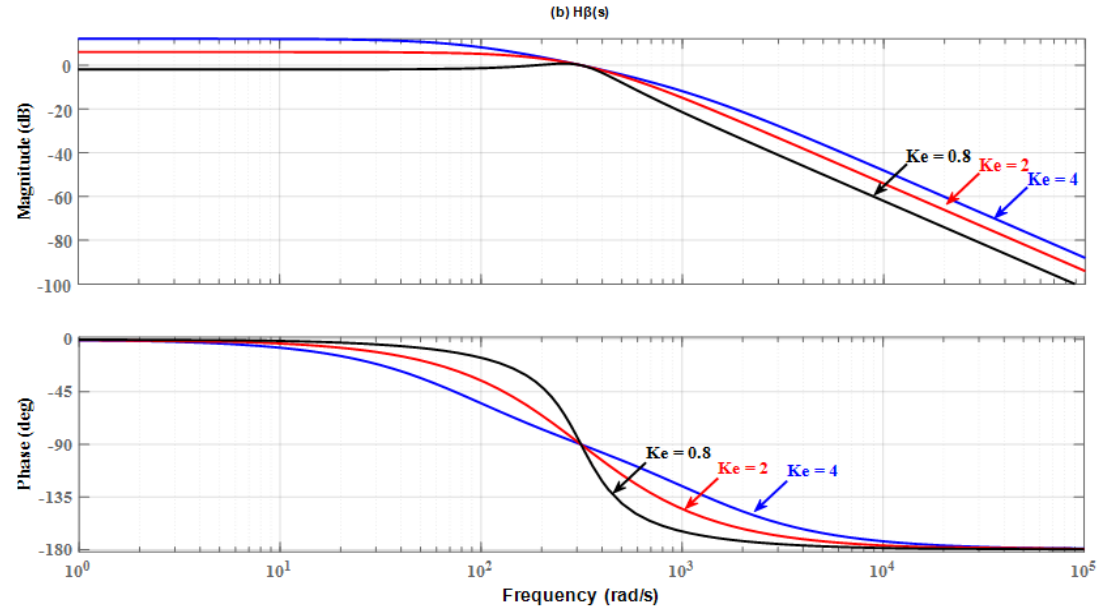
$$H_\alpha(s) = \frac{V_\alpha(s)}{V_{grid}} = \frac{K_e\omega_{PLL}s}{s^2 + K_e\omega_{PLL}s + {\omega_{PLL}}^2} \tag{20}$$

$$H_\beta(s) = \frac{V_\beta(s)}{V_{grid}} = \frac{K_e{\omega_{PLL}}^2}{s^2 + K_e\omega_{PLL}s + {\omega_{PLL}}^2} \tag{21}$$

The value of ω_{PLL} in the steady state is $2\pi 50\ rad/sec$. In Figure 3, bode plot is drawn for $H_\alpha(s)$, Figure 3(a) and $H_\beta(s)$, Figure 3(b) at different values of K_e [22], [23]. From bode plot, it has observed that $H_\alpha(s)$ acts as band-pass filter (BPF) with frequency centred at $\omega_{PLL} = 50\ Hz$ and it has unity gain with zero phase lag at this frequency. While, the $H_\beta(s)$ behaves like low-pass filter (LPF) at cut-off frequency of ω_{PLL}. The gain of $H_\beta(s)$ is unity with 90° phase lag at ω_{PLL}. The system bandwidth is varying according to the value of K_e. However, at the ω_{PLL}, the gain of the amplitude and phase remains unchanged for both for $H_\alpha(s)$ and $H_\beta(s)$. It has concluded that SOGI provide quadrature signals having the same amplitude of the input signal, but with 90° phase difference and it can suppress high frequency disturbances [22]. From Figure 2 of SOGI-PLL, the estimated angular frequency ω_{PLL} is feedback to SOGI module to act as resonance frequency for SOGI, and it is called ω_r. At the steady state, the value of the estimated angular frequency ω_{PLL} is equal to the angular frequency of the input, that would make the SOGI-PLL as a frequency adaptive PLL.



(a)



(b)

Figure 3. Bode plot of the SOGI transfer function block for different values of K_e: (a) $H_\alpha(s)$ and (b) $H_\beta(s)$

Figures 4 and 5 show the SOGI-PLL control structure, implementing the SOGI to obtain the reference currents and the structure of feed-forward and decoupled current control [17], [22], [24]–[32]. The reference value of I_{d-ref} is produced by the first closed loop control unit of the voltage controller, and the reference value of I_{q-ref} is established using (12) with $V_q = 0$. To determine the reference $d-axis$ component grid current I_{d-ref} through PI controller, the voltage regulator compares the measured DC voltage Vdc with the DC reference voltage $Vdc - ref$. The PI control strategy with feed-forward is suggested, as shown in Figure 5, in order to reduce the burden associated with performing the task of the PI controller and to give the system the ability to respond quickly in the event of a disturbance. To enhance the PI controller performance, Cross-coupling terms and voltage feed-forward are typically utilized, Figure 5, where it would reduce the stability problem which comes from the delay in the system that caused by the voltage feed-back filter, Figure 5. Despite all these advancements, PI controllers still have a relatively poor capacity to compensate for low-order harmonics, which is a significant disadvantage when used in grid-connected systems.

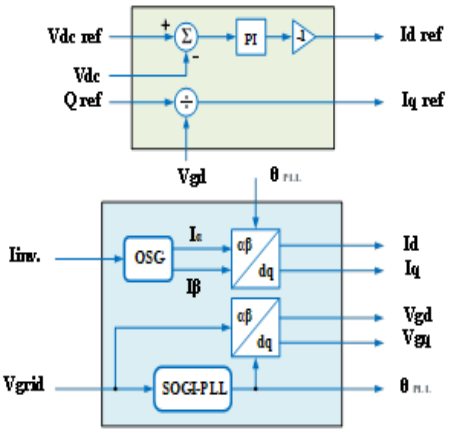


Figure 4. Block diagram of implementing SOGI-PLL to obtain actual and reference quantity

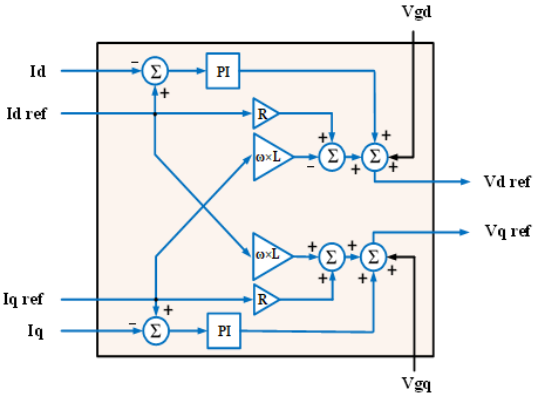


Figure 5. Diagram of feed-forward and decoupling current control

4. SPACE VECTOR MODULATION SVM OF SINGLE-PHASE INVERTER

Nowadays different PWM techniques are available, which have crucial impact on some criteria, particularly harmonic distortion, losses of switching and the utilization of DC bus. The SVM considered one of the most popular methods that has well achievement on these requirements. It is applied to a variety of inverter topologies, such as single-phase, three-phase and multilevel inverters [33]–[35].

In this section, SVM-PWM of single-phase full-bridge is presented. In order to cope shoot-through failures, complementary operations of both inverter legs are operated, hence there are four possible switching states, which are shown in Table 1. The switches are shown in Figure 6.

Table 1. Switching vectors of single-phase full-bridge inverter

S1	S3	VAo	VBo	VAB	Vector
0	0	0	0	0	V_0
0	1	0	1	-1	V_1
1	0	1	0	1	V_2
1	1	0	0	0	V_3

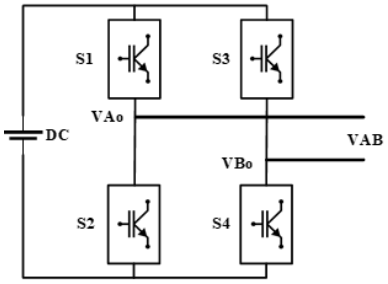


Figure 6. Diagram of single phase inverter

These switching states are arranged in one dimensional space vector as depicted in Figure 7. because the inverter terminals are connected to same potential point, therefore no energy is transferred to load. Thus, among these four switching states, two are represented a null value, and their location is at the origin of the space vector.

The arrangement of space vector has two active operation regions, each one of these regions is adjacent to the rest of active vectors, V_1 and V_2. The potential switching states is characterised by two numbers, which are corresponding to the inverter legs operation states. State 1 is the conduction of the upper switch and 0 is the conduction of the lower switch.

The instantaneous output voltage of the inverter is determined by a command vector V. This vector at the same frequency of the desired output voltage of the inverter is oscillated between the two operated regions. When the desired operation region is identified, it is crucial to find the time length at which the switching vector must be applied at each commutation time T_s.

When V is lied in a particular operation region, sum of the vectors would provide the required output voltage, as expressed by:

$$V = V_0 + V_x + V_3 \tag{22}$$

V_x is depending on the operation region and it could be either V_1 or V_2 in order to complete the switching pattern. The null vectors V_0 and V_3 are used. The correspondent switching times of V_0, V_x and V_3 are calculated from:

$$T_x = \frac{V}{V_{cc}} T_s \tag{23}$$

$$T_0 = T_3 = \frac{(T_c - T_x)}{2} \tag{24}$$

T_c is the commutation period divided to 2 sections and T_x represents the period at which the state of active vector is being applied to the load. When these periods have determined, a sequence of switching that have nearest switching vectors to the required output voltage V could be used. Since this would provide less ripples for the interested variables. The arrangement of switching time pattern is shown in Figure 8. This symmetrical pattern is used to suppress the harmonic distortion presence in the resulted waveform [36].

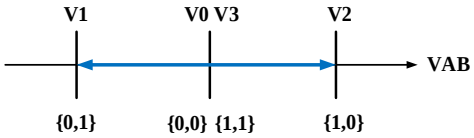


Figure 7. Inverter output voltage space vector representation

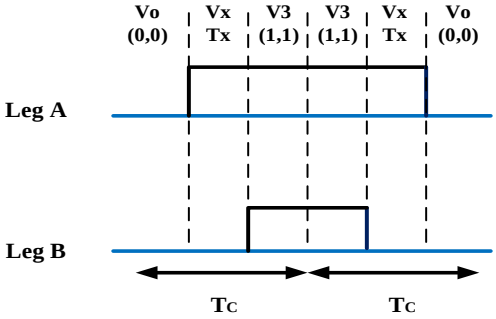


Figure 8. Arrangement of switching pulses

5. IMPLEMENTATION OF SVM-PWM BY FPGA

Configurable logic, I/O, and connectivity blocks make up the FPGA architecture. Additionally, clock circuitry will be present to drive the clock signals to every logic block. There may also be accessible additional logical resources like arithmetic logic units (ALUs), random access memory (RAM), and decoders. Static RAM, anti-fuses, and flash erasable programmable read-only memory (EPOM) are the three fundamental categories of programmable elements for an FPGA. The FPGA's logic is housed in the configurable logic blocks (CLBs). These CLBs include enough logic to construct a tiny state machine in the large grain design that is currently employed by all FPGA vendors. The block has RAM for arbitrary combinational logic functions, or look-up tables (LUTs), to be created. An FPGA's logic building blocks can be as compact and straightforward as a programmable logic devices' (PLD) macro-cell (known as fine-grained architecture) or bigger and more intricate (coarse grained architecture). They are never, however, as big as a complete PLD or a complex programmable logic device

(CPLD) logic block. However, the basic building elements of an FPGA are typically just a few logic gates or a look-up table and a flip-flop. In this paper, the SVM-PWM control signal has been implemented on FPGA board using the very high-speed integrated circuit (VHSIC) hardware description language (VHDL). The commutation and dead time are considered as the inputs, whereas the outputs are the four PWM pulses for the operation of inverter switches. Along with the, main inputs, commutation, and dead time, the main board clock was used as an input to synchronize the signals. The duty cycle of the generated PWM signals can be varied based on the inputs, which are the dead and commutation time. The schematic diagram of the implemented model is shown in Figure 9, where the inputs, outputs, and main signals are clearly indicated. The resource utilization report of the implemented model is shown in Table 2.

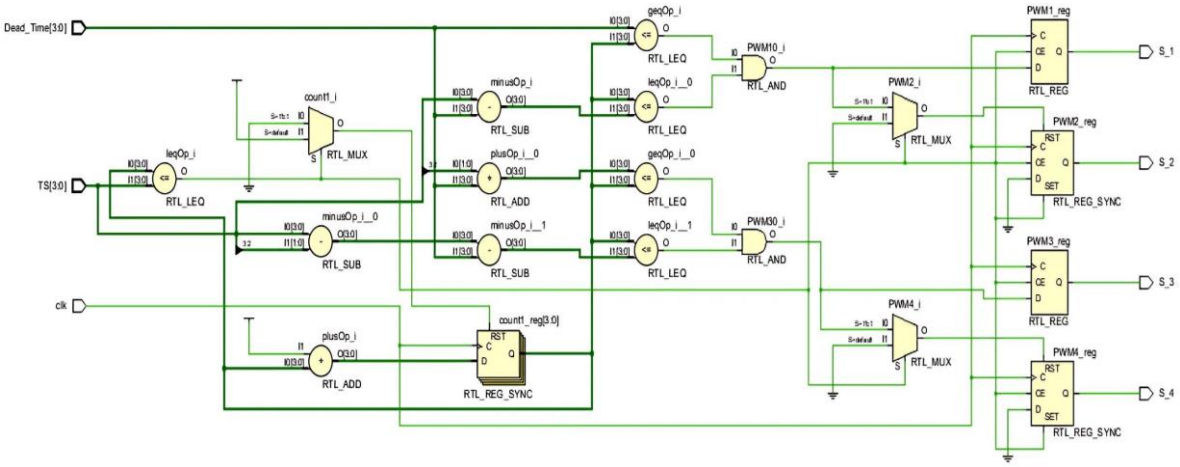


Figure 9. Schematic diagram of the implemented SVM-PWM by FPGA

Table 2. Device utilization summary of the proposed SVM-PWM

Resources	Utilization	Available	Utilization %
LUT	25	17600	0.14
Flip-flop (FF)	8	35200	0.020
Input/output (IO)	13	100	13
Ports and clock buffers (BUFG)	1	32	3.13

6. SYSTEM SIMULATION AND DISSCUSION

MATLAB/Simulink has been used to simulate the grid connected voltage source inverter (VSI). The system parameters are listed in Table 3. The responses of SOGI-PLL is shown in Figure 10. It shows good dynamic response even when the gird voltage is distorted. In Figure 10, the grid voltage is distorted by the 5th, 7th ,11th, and 13th harmonics at $t = 1.2\ sec$ and the generated orthogonal voltage $V_{g\alpha}$ and $V_{g\beta}$ are pure without harmonics, and the angular frequency follows the command at $2\pi 50$ rad/sec.

Table 3. System parameters

Parameters	Value
Line voltage	230 V
Switching frequency	10 KHz
DC Link capacitor	8.3 mF
DC Link voltage	400 V
Nominal power	4.5 KW
Inverter side inductance	3.7 mH
Grid side inductance	4.29 mH
Filter capacitor	3.3 µF
Filter capacitor resistor	15.8 Ω
Inverter side resistor	0.0134 Ω

The DC link voltage is controlled at 400 V, and the DC voltage control loop would provide the reference current I_d that is responsible for controlling the injected active power and it is decoupled from I_q which is controlling the reactive power whether it is injection or absorption. Figure 11, shows the command of quadrature current and AC reactive power. The values in Figure 11 are shown, for the purpose of explanation. The I_d command is set from the DC voltage control loop, while the I_q is controlling the reactive current based on $Q = -V_d I_q$ and that would prove the profile of AC reactive power in Figure 11 and Figure 12.

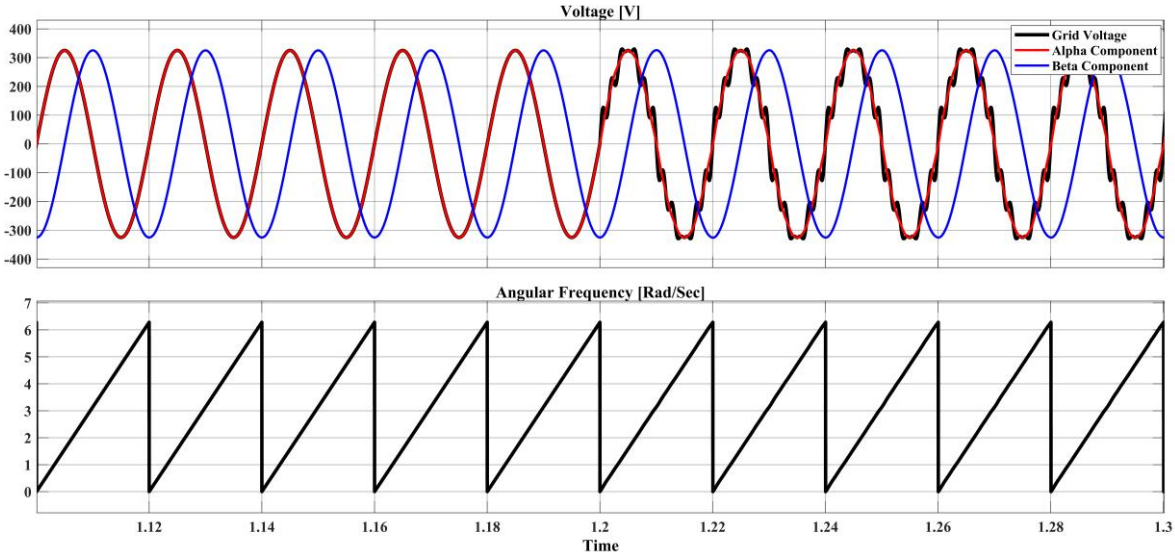


Figure 10. Distorted grid voltage and generated orthogonal voltage and angular frequency

In this simulation, the reactive power 700 VAR is injected into the grid, as shown in Figure 11. It should be mentioned that the value of the current is less than 28 A, since the active power has not been injected to the grid yet. At 0.6 sec, 4.5 KW active power is injected to the grid, the semiconductor and filter losses are neglected. Therefore; the active power at the point of common coupling (PCC) and the active power form the DC side are equal. This means that the converter acts as a constant current source of magnitude I_{dc}. At 2 sec from simulation time, the reactive power 1 KVAR is absorbed from the grid. From Figure 12, it is observed that the DC link voltage is kept at 400 V, and the active and reactive power are decoupled in the control. The overshoot in the reactive power response could be eliminated by adjusting the PI control gains of the $q - axis$ current component, however this may result in longer durations to achieve zero error.

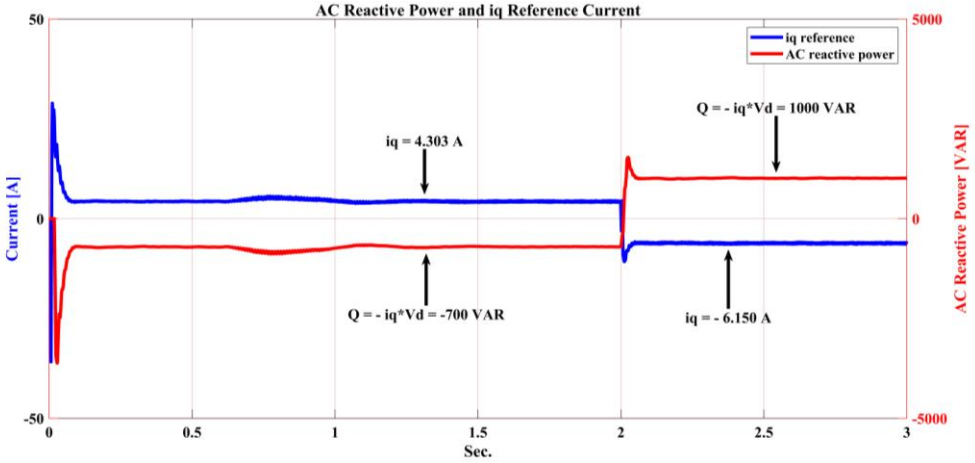


Figure 11. Iq reference current and AC reactive power

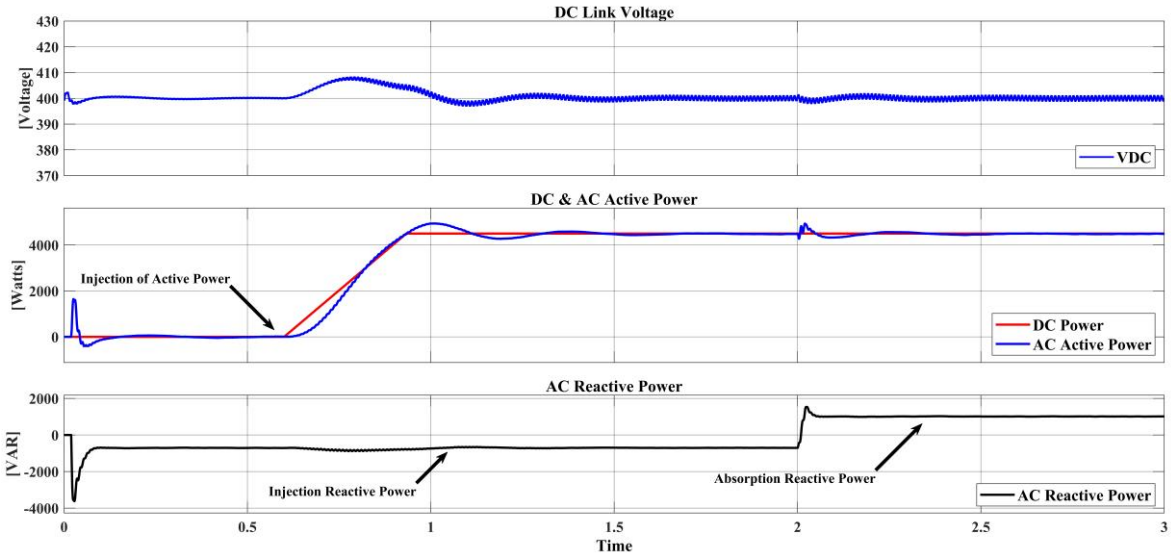


Figure 12. DC link voltage, and DC and AC active and AC reactive power flow

The SVM technique is used to reduce the harmonic distortion and switching losses. The state of active vector is being applied to the load when the switching vector is near to the desired output voltage. The sector 1 and 2, angular frequency and switching duration of leg A is shown in Figures 13 and 14 respectively.

In Figure 15, the grid voltage is scaled down for the sake of clarity with the current. When the reactive power is 700 VAR, the current is leading the grid voltage, Figure 15-A and its value is less than the rated because the active power has not injected into the system. When the active power is injected at 0.6 sec from the simulation time, the current is in-phase with the grid voltage, Figure 15-B, and its value is approximately 28 A at 2 sec from the simulation time, the reactive power 1 KVAR is absorbed, and it is seen that the current is lagging with grid voltage, Figure 15-C.

The VHDL program, written to implement the model, was simulated on VIVADO 2018.1, and the resultant waveforms are shown in Figure 16. After achieving acceptable results in simulation, the model was implemented on ZYBO FPGA board. The resource utilization report of the implemented model shown in Table 2 indicates only 0.14% of the LUT, 0.02% of the FF, 13% of the inputs/outputs, and 3.13% of the buffers have been used for the implementation purpose.

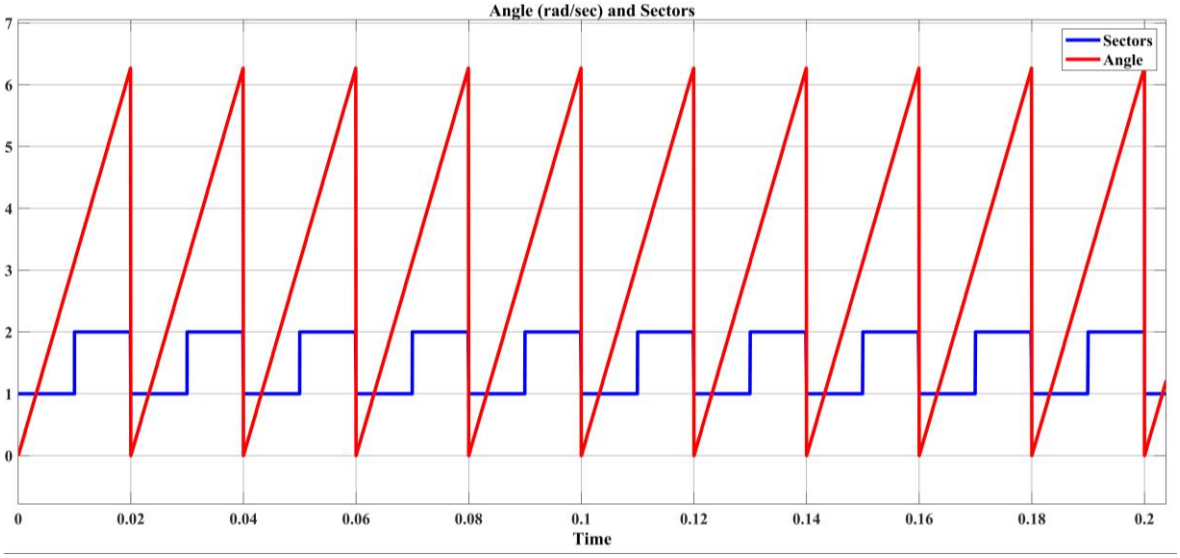


Figure 13. Sectors of SVM and angular frequency

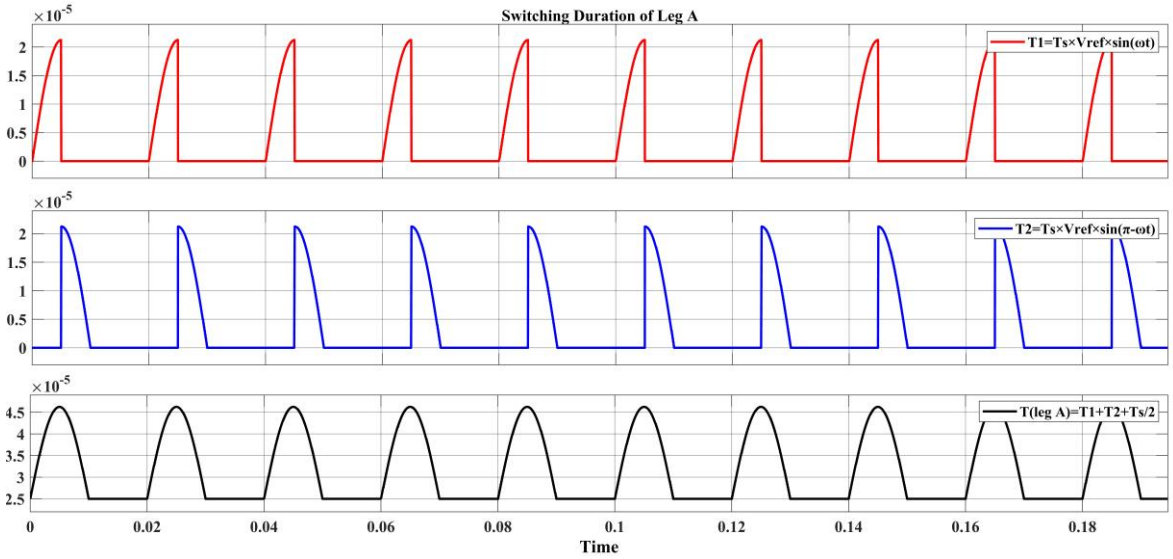


Figure 14. Switching duration of leg A by SVM

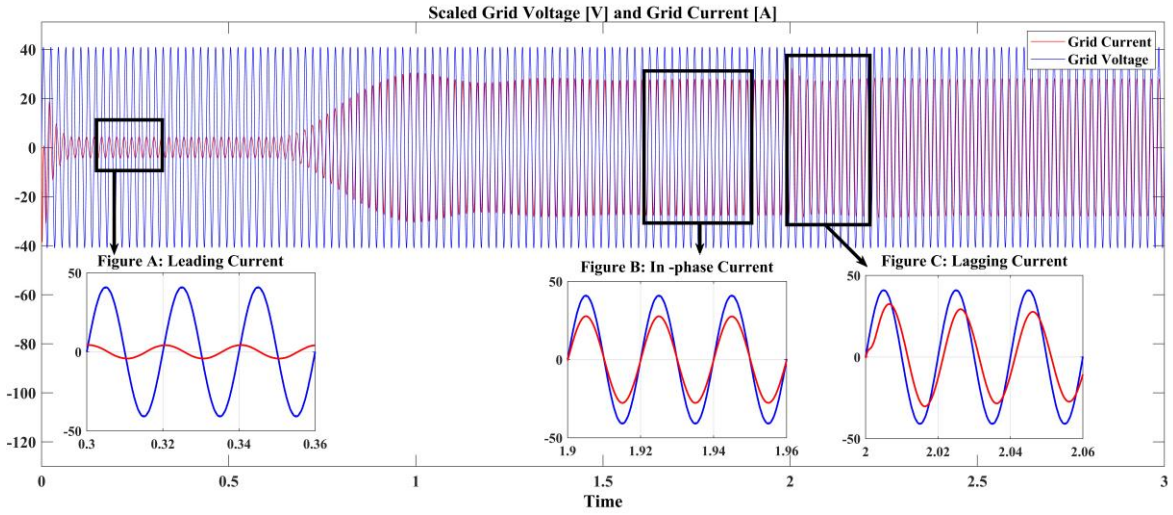


Figure 15. Scaled grid voltage and injected current

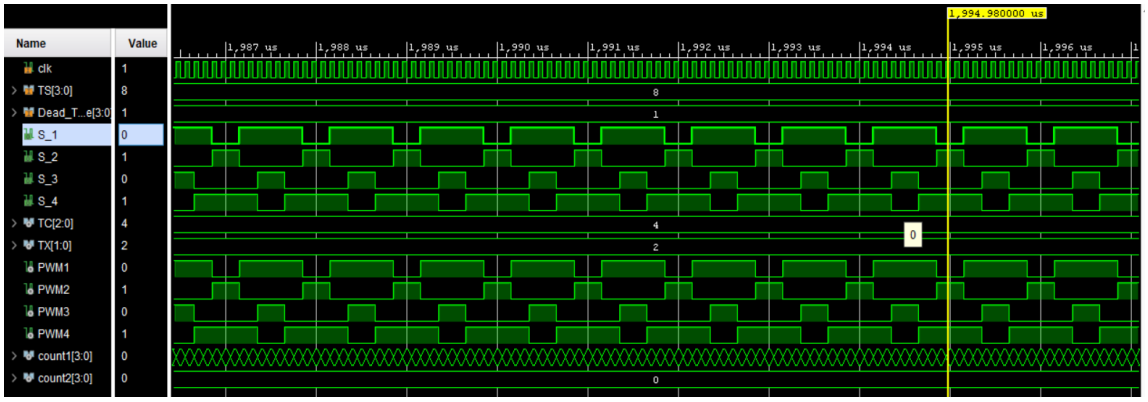


Figure 16. Generated SVM-PWM signals (S_1, S_2, S_3, and S_4)

7. CONCLUSION

Maintaining the DC link voltage and independent control of flowing active and reactive power are the goals of vector control. A grid voltage feed-forward is employed in order to obtain a good dynamic response. Due to the delay the voltage feedback filter causes in the system, this in turn causes stability issues. An enhanced grid voltage feed-forward filtering technique, which is LCL filter with damped resistor, has considered to solve this issue. However, the PI controller used has poor harmonics rejection capability, and this could be handled by using another controller. On FPGA, the space vector method has been proposed and implemented as a PWM switching operation that might be utilized to generate direct switching pulses for inverter switches. According to the simulation results, the control system has good dynamic response and is highly accurate at regulating the flow of both active and reactive power.

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