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Architectural framework and register-transfer level design synthesis for cost-effective smart eyewear

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ABSTRACT

In today's time more than 70% of the world's population suffer from eye dis-normalities leading to the usage of eyewear or spectacles. Integrating profound technologies with daily utilities could serve some of the issues improving and optimizing our lifestyle to the most. One such way is to infuse nanosized chip in eyewear i.e., powered spectacles or shades to detect the location of the spectacles whenever it is necessary. The nanosized chip proposed has features including self-designed Bluetooth operating digital circuit, timer logic, clock generation using astable multivibrator circuit, emergency button, beep alarm and impact sensor. The values of resistance and capacitace is calculated to be 18 K ohm and 47 uF to obtain 1 Hz frequency. An optimal pin placement arrangement is analyzed, and the timing waveform is simulated using Verilog as proof of logical working of the chip. 13 D flipflops have been calculated to refrain from eye related strains. This paper suggests a bottom-up approach and develops the architectural framework of the chip, its working flow, system on chip top-view, digital logic description of each block and its implementation using Verilog hardware description language (HDL). The complexity and computational cost of the designed chip is minimal thus being commercially viable.

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1. INTRODUCTION

As stated, today, more than 70% of the people ranging from all age groups suffer from eye abnormalities and hence are required to wear powered glasses. Figure 1 shows the data as per vision council of America. About 64% wear eyeglasses, and about 11% wear contact lenses, either exclusively, or with glasses. Over half of all women and about 42% of men wear glasses. Due to advancement in almost every sphere of life, the goal is to upgrade lifestyle by converting an ordinary powered glass into a smart eyewear.

The idea works on the principle of chip designing, or we say, system on chips. System on chip is an integrated circuit that inscribes in it all the features designed to accomplish one specific task performed using the analog circuitry, digital circuitry, mixed signals, radio frequency functions, clock generation, peripherals, and timers-all on a single chip [1]. The advantages of system on chip (SoC) varies from: i) compact and small size chips, ii) reduction in complete system design as compared to motherboard-based designs, iii) low power consumption, iv) better performance and efficiency, and v) economical and commercially viable.

This initiative finds its application in various domains including women and kids' safety, operating for elderly or differently abled people. In general, anyone who requires eyewear in day-to-day life will account for the beneficiary. The paper introduces the architecture of the chip designed to meet the specified features

namely detecting the location of the spectacle remotely whenever required. It includes block-level description, digital logic and implementation using Verilog logic description of each block and its implementation using Verilog hardware description language (HDL). The main objective is to form an architectural framework and register-transfer level (RTL) synthesis to meet the requirements. The design of the chip and each of its blocks including the design of the impact sensor is novel.

One of the important components of the chip is the impact sensor. The system is designed in such a way that whenever there is an impact on the spectacles either by force or by falling, the force is fed as an input to the piezoelectric sensor used which is converted to an electrical signal served to the alarm beep system as an input. The sensor needed should have piezoelectric properties, lies in the range of a few nanometres and is flexible. Because of such requirements, the sensor used here is simulated in the paper [2]. The sensitivity of the sensor is kept at a value which is used to avoid false emergency signals reporting to the owner.

Since the architecture incorporates sequential circuits for which clock generation is required, an astable multivibrator circuit is used to produce a clock frequency of 1 Hz. To get an output 1 Hz specifically, the values of capacitor and resistors have been chosen since the input is fed into timer logic. The design is inspired by [3]. In this work, designed and simulated FinFET [4]–[8] and complementary metal-oxide semiconductor (CMOS) based unstable multivibrators are mentioned. The performance of the proposed circuit was simulated by varying the resistance-capacitive delay topology, supply voltage, and operating temperature at the 45 nm technology node.

The alarm system in the eyewear is an integral component of the system. The sound generator circuit that forms the basis of the beep sound being generated is obtained using a microcomputer programmable sound generator this uses N-Channel microelectronics systems design series (MOS LSI) based architecture using minimal CPU time to interpret the I/O [9]. It is necessary to be able to incorporate sound generating capability into chipsets as technology is continuously causing wearable electronics to shrink.

The RTL is designed to control the activities on the chip. The usage of DNA fragmentation factor (DFF) in a digital circuitry is inevitable in timer applications. A suitable way to reduce the power dissipation problems in this pulse triggered DFF is the usage of embedded clock gating schemes [10]. A mux-based design is implemented and verified the logic using simulation [11]. Various clock gating schemes have been studied thoroughly and the significance of overcoming delay enlargement is given light. The proposed clock-gated pulse-triggered DFF (CGPT_DFF) in [12] can be considered in the implementation of the timer block of our proposed design. A prototype model to link IoT with hardware applications is also provided by [13]. It motivated for the idea of an upgraded lifestyle, which is the main objective this research.

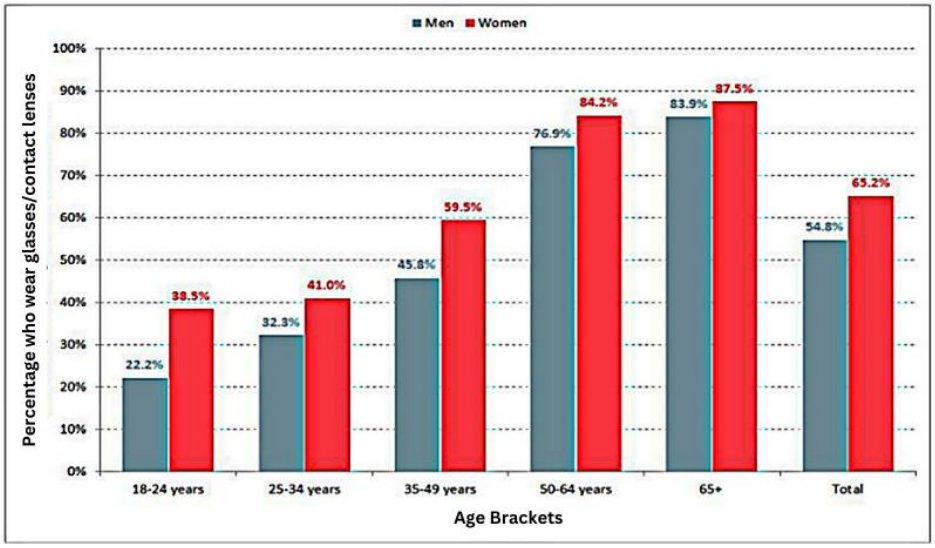

Figure 1. Percentage of men and women in different age groups wearing glasses/contacts

2. METHOD

Tradition glasses fails to solve the purpose of the upgraded lifestyle that is followed. Chip designing being the most profound and optimized solution could be applied here. The chip designed is broken down into blocks each having its own digital circuitry and the overall proof of concept is provided in the results [14]. Method includes proposed model which describes the working of chip, design flowchart which describes the

working functionality of the chip in form of a flowchart andarchitecture which discusses the SoC architecture of the overall chip including each block and peripherals.

2.1. Proposed model

Eyewear is upgraded to a smart one by incorporating a system on chip design placed inside the frame of spectacles as shown in Figure 2 with a mobile application to link it with smartphones. The size of the chip is carefully chosen to be ranging from a few milimeters since the idea is to make it cost effective and commercial. The working of the chip is designed to incorporate features including show in Figure 2.

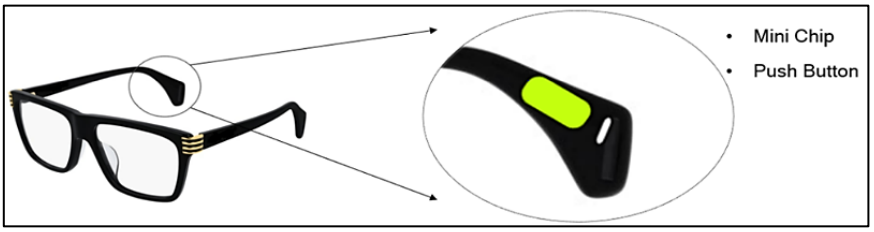

Figure 2. Proposed model and placement of chip

2.1.1. Bluetooth module with emergency signal

Executed using the mobile application linked to the infused chip. When the push button salt overly sensitive (SOS) is pressed, an auto generated signal will notify the emergency contact of the user on the linked smartphone via the Bluetooth module. A digital Bluetooth circuitry is designed to send or receive signals between the Bluetooth module and mobile phone. This is useful in case of emergencies like mishaps with kids while playing or with aged people since carrying a mobile phone is difficult for them. In such cases the signal will directly be sent to their guardians for further help.

2.1.2. Screen time overload (timer)

A 13 D-flipflop timer is designed to overcome screentime overload. The timer is adjusted for notifying the user to take short breaks between long office or school hours after every 2 hours to refrain from starining the eyes. This is helpful for keeping the eyes healthy especially in the times which are prominent for work from homes and online classes. Once cross-folded the timer restarts.

2.1.3. Impact sensor to send emergency signal for external damage

In case of an emergency, if the eyewear breaks/falls, an automatic signal sensed using this actuator would be sent to the linked cell phone. These cases shall not require the push of emergency button. False signals are reduced by increasing the sensitivity of the sensor. This sensored is designed and simulated by one of the authors herself. Hence the fabrication cost, nanometer range and good voltage output makes it a desirable one to use.

2.1.4. Alarm beep system

It is incorporated to notify the user using a beep sound as described in case of the emergency signal, find my device or screen time overload. The alarm beep system supports cases where a blink system won't be useful since the application area lies in the ballpark of elderly and kids age domain. A sound notification would be easily recognizable and acted upon than any other means of triggered stimulus.

2.2. Design flowchart

The flowchart in Figure 3. depicts the scenarios in which the alarm beeps in the eyewear or the mobile application gets a notification. The timer is set for every 2 hours of duration after which it triggers the alarm, the cycle continues infinitely. Whenever the impact sensor is actuated by means of external attacks, a signal is sent to the mobile application and the supervisor is alerted via the notification. In case the eyewear is kept elsewhere due to negligence, the "where's my device?" option in the mobile application can be enabled manually, which causes the alarm to beep by virtue of the Bluetooth module's ad-hoc network. The beep sound is said to automatically trigger after every 2 hours of inactivity.

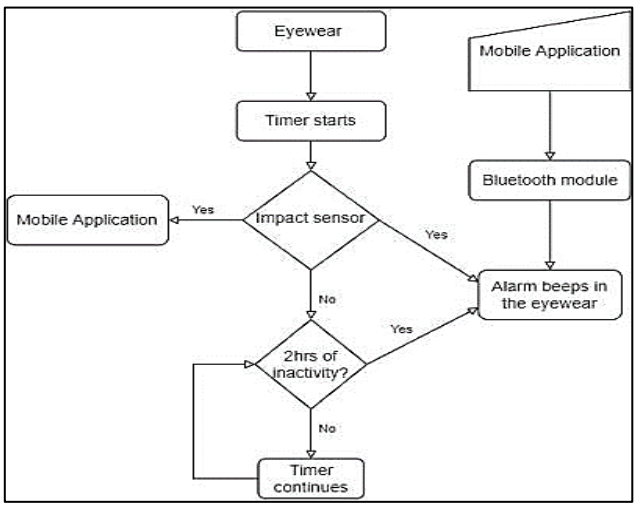

Figure 3. Design flowchart

2.3. Architecture

The overall architecture of the chip is depicted in Figure 4. It contains various I/O pins to perform input-output operations including the clock pin generated via multistable vibrator. A total of 10 pins is taken to analyze the overall pin placement which is done using cadence Innovus to get an idea regarding no. of metal layers used and total possible pins placed. Power pads are placed to provide DC power to the circuit. Individual blocks include Bluetooth module, Bluetooth digital circuitry, alarm system and timer logic. Each block is individually described in following sections. Various 2-INPUT OR gates have been used to achieve the functionality as stated in the flowchart (Figure 3).

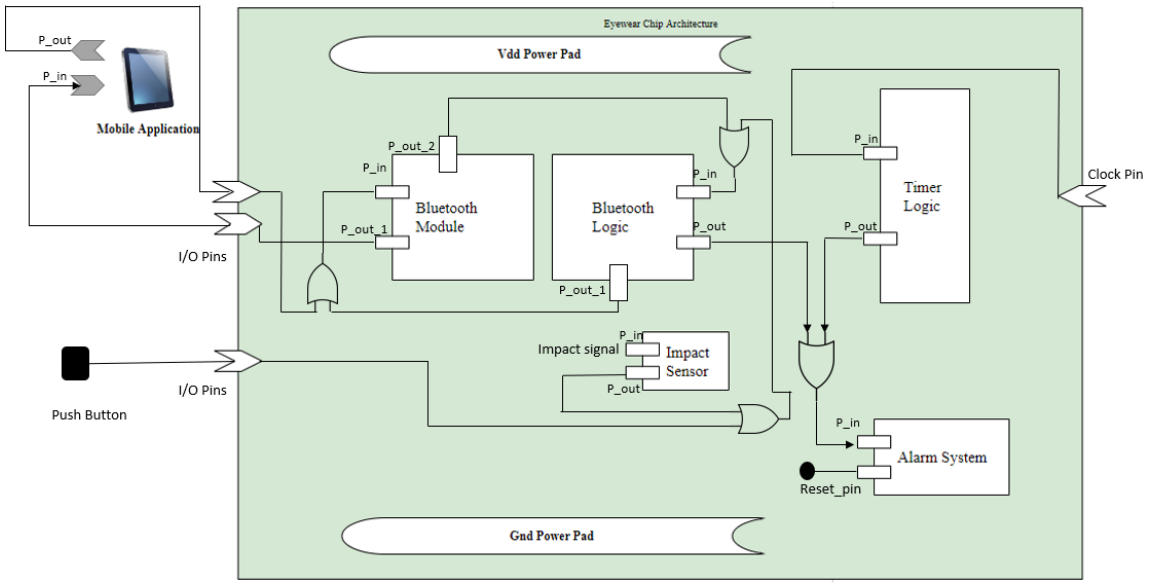

Figure 4. Eyewear SoC architecture

2.4. Block description

Blocks that are designed as per the architecture is enlisted below. The circuitry and design parameters are listed to make the chip functionally possible. The blocks include a clock generator circuit [15] using a multibivrator model. The resistor and capacitor values are calculated keeping in mind the desired output clock frequency. Timer circuit is designed to work for 2 hours then reset. It is calculated on the survey about healthy eye status and screen time preferred. A default Bluetooth module is used operating with self-designed Bluetooth logic which is implemented using Verilog code, its RTL synthesis and timing diagram as a proof of working concept.

2.4.1. Astable multivibrator as clock generator circuit

The clock is generated using a multistable vibrator as depicted in Figure 5. One of the major reasons why the 555 timer is not used to generate clock is because of its large size. Hence, calculations are performed to ensure 1 Hz of frequency being generated as an output of the circuit to be fed into the timer logic [16]. Here we assume:

$$R2 = R3 = R \tag{1}$$

$$C1 = C2 = C \tag{2}$$

hence, the expression of output frequency is given by (3):

$$F = 1/(1.38\,RC) \tag{3}$$

the required frequency is 1 Hz as output frequency, the computed values of resistor and capacitor are:

- R=18 K Ohm (Typically 15 kohm should be used but due to some degradation, a higher value is chosen).
- C=47 uF.
- V1 is set to be 5 V.

These values generate an oscillation wave at a frequency of almost 1 Hz.

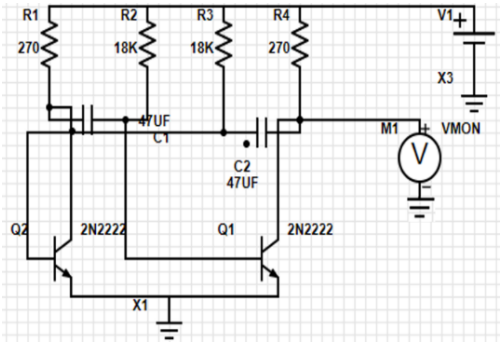

Figure 5. Astable multivibrator circuit

2.4.2. Default bluetooth module

A default Bluetooth module is used to make a wireless connection between the chip and mobile application [3]. The circuit used is as depicted by Figure 6. This module, connected with required I/O pins is used for the implementation of the chip. It is a low power embedded Bluetooth module that is required on the SoC to achieve a connection between bluetooth compliant devices, in this case, a smartphone. The communiucation developed is used to activate the location or emergency signal arrived from the eyewear to smartphone and vice versa. It is designed to achieve a low power consumption module [17].

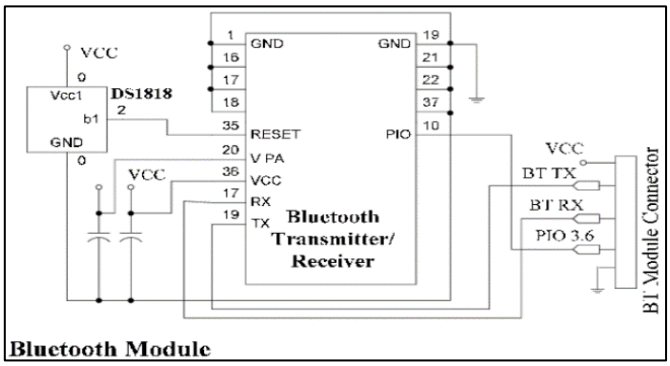

Figure 6. Bluetooth module

2.4.3. Timer

The timer block consists of an up-counter constructed using 13-bit D flip-flops (DFFs), acting as a timer on a fixed frequency clock of 1 Hz [18]. The timer counts 7,200 seconds, which constitutes 2 hours. 1 Hz frequency generated by the proposed circuit is used as clock input and is fed synchronously to all the 13 flops. This clock is the output of the proposed clock circuitry that generates a 1 Hz frequency pulse as its output. The binary for 7,200 is 1110000100000, consisting of 13-bits in totality, hence the 13-bits in the timer. The up counting starts from 0sec all the way up to 7,200 sec after which a combinational logic resets the entire 13-bits back to 0. It is at this point that a signal is also sent to the alarm system that triggers the sound generator. The combinational logic involved in giving inputs the 13 DFFs was simulated, and the result has proven to be accurate for every 2 hours as required. This has been represented below in Figure 7.

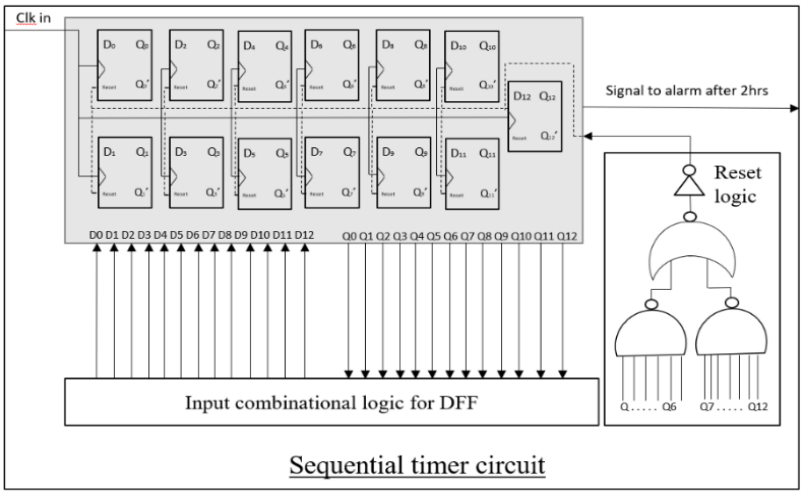

Figure 7. Timer

3. RESULTS AND DISCUSSION

The implementation is carried out using Verilog HDL and the results are depicted in the form of timing waveform and RTL logic. The heart of the circuit lies in the Bluetooth digital logic designed to drive the specifications as described. The results include final calculated values of R, C parameters required for clock generation, no. of D flipflops for timer circuit according to the screen time considering medical issues, working proof of the chip using timing waveform and RTL synthesis of the chip. The results also include the pin placement analysis using Innovus by cadence to choose the correct arrangement of pins on the chip metal layers.

3.1. Pin placement

Pin placement is the most important step in designing especially floorplanning. While using the electronic design automation (EDA) tools as cadence innovus in this, there are various options as to how we can place the pins [19]–[21]. Pin placement also depends on the number of layers used in the design. Since the number of pins here are taken to be 10 in total, and only 3 metal layers is required since circuitry is not that complex, the table show various arrangement and legalizing results when the pins are placed using the tool [22]. Each arrangement is analysed and the best one is chosen among all options as shown in Table 1. From the table we can infer that both fill_optimized and fill_sinusoidal can be used as the type of arrangement since it legalizes all pins in both 2 and 3 metal layers.

Table 1. Pin placement analysis

SL no.	Arrangement type	Pins legalized in 2 metal layers	Pins legalized in 3 metal layers	Present in layer 01	Present in layer 02	Present in layer 03
1	Fill_Track	7	10	Yes	no	Yes
2	Fill_layer	8	9	Yes	Yes	Yes
3	Fill_optimize	10	10	Yes	Yes	Yes
4	Fill _diagonal	8	7	Yes	Yes	Yes
5	Fill_sinusoidal	10	10	Yes	Yes	Yes
6	Fill_checkerboard	9	10	Yes	Yes	Yes

3.2. Astable multivibrator square wave generation

The astable multivibrator circuit as described produces the output as shown in Figure 8. Note that the circuit creates a square wave as desired with a little fluctuation due to presence of passive devices. This square wave is served as the input to the timer circuit as a clock [23].

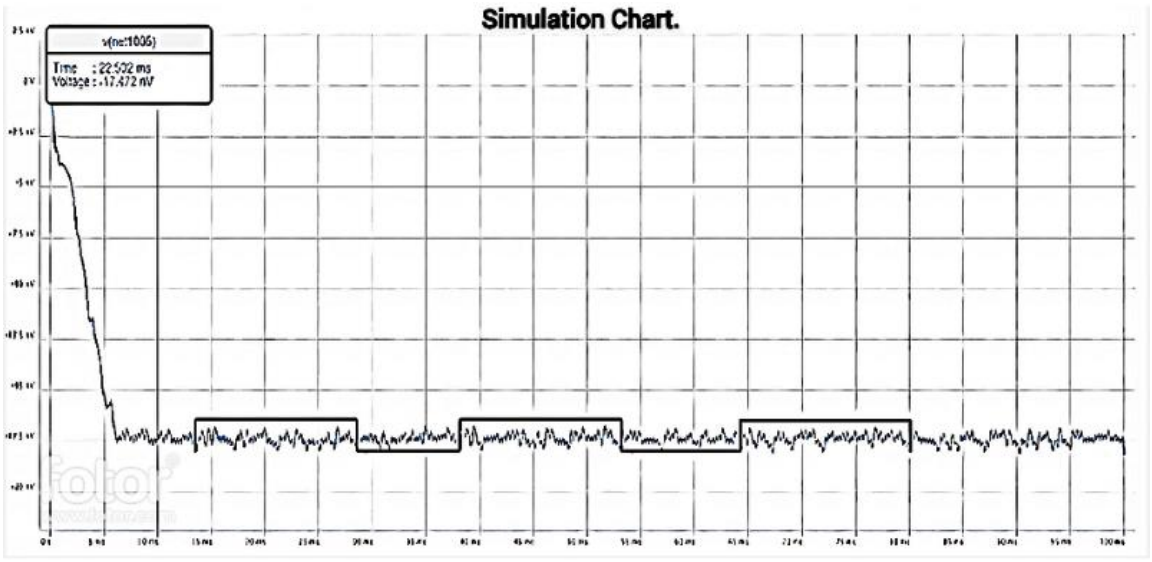

Figure 8. Multivibrator output waveform

3.3. RTL synthesis

Figure 9 shows the RTL of the Bluetooth logic. The RTL is a mux-based design to understand the scenario and trigger appropriate outputs [24], [25]. Switch press on manual press, impact signal on impact is the input signal to the logic. Alarm and reset are the output triggers of the circuit. Code and bt_code is input and output communication codes with BT module. The circuit describes the heart of the working of chip.

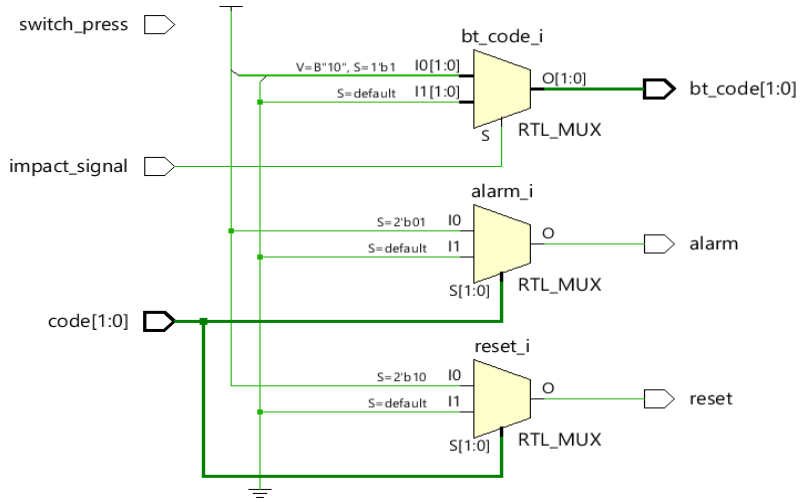

Figure 9. RTL logic synthesis

3.4. Timing waveform

The Bluetooth logic is a muxed combinational circuit that interfaces with the Bluetooth module. The Bluetooth module and Bluetooth logic communicate codes and signals for specific actions. The reset can be

initiated by a connected device and on switch press it sends the code to the Bluetooth module. It also sends signals to activate the alarm and receives the impact sensor signals to send panic code to the Bluetooth. In Figure 10, code and bt_code are the code communications to the Bluetooth module to identify the scenario. On receiving code 10, reset is triggered on the SoC and on receiving the code 01, the alarm is activated. The bt_code is the output sent to connected device. If a switch is pressed panic code 10 is sent and on impact panic code 01 is sent. The timing diagram as shown below proves the concept as simulated. It shows that the architecture is working if fabricated.

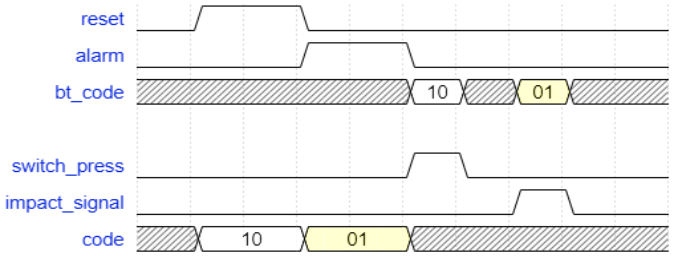

Figure 10. Result waveform

3.5. Result table

The entire result section cumulated is presented in form of Table 2. The timing results, pin placement arrangement, passive devices values and timer logic calculations are enlisted. The table consists of clock generation parameters such as resistance and capacitance with their theoretical values, timer block with its calculated frequency and time, pin placement optimized design, digital logic verification based on RTL and the simulated graph.

Table 2. Cumulated results

Sl no.	Individual blocks	Results
1	Clock generation	R=18 k ohm, C=47 uF
2	Timer block	13 D-flipflops, 2 hors time, 1 Hz
3	Pin placement	Fill_optimized, Fill_sinusoidal
4	Digital working logic	Timing and RTL verified working

4. CONCLUSION

By implementing the given ideology, the goal is to manufacture an automated eyewear/spectacles with infused chip as a deliverable. The project focuses on various application domains including women and kids' safety, operating for elderly or differently abled people. The aftereffects of corona included an increased screen time due to online classes/work from home practices leading to straining of eye that could be controlled using screen time alert system infused in the chip. The chip also contains impact sensors which, on sensing any type of unusual pressure/jerk would lead to sharing of GPS location through the interlinked emergency contact via smartphone. This happens via the Bluetooth module's input lined with signal generated by impact sensor. The beep alarm system may also be helpful for differently abled people in finding their spectacles via Bluetooth enabled feature using smart phones. All the following features are achieved by laying the required architectural framework and implementing block wise. The values of resistance and capacitace is calculated to be 18K ohm and 47 uF to obtain 1 Hz frequency. An optimal pin placement arrangement is analyzed, and the timing waveform is simulated using Verilog as proof of logical working of the chip. 13 D flipflops have been calculated to refrain from eye related strains. The RTL synthesis and results show that the chip is working as per the design and hence this may be considered for the physical design and then tapeout. The product includes the technical merit of automating day-to-day life products. The idea is novel and has not been productionized. The enhancement to the given eyewear technology is a much-needed upgrade as its applications are at par. The focus of making it cost effective is visualized by the simplistic design and optimal usage of microprocessor technology. By upgrading the present eyewear, using a small system on chip design and its architecture as mentioned above, it could revolutionalize our lifestyle. Adding a basic chip, with a specific range and functionality could prove to a boon to a general mass. Due to limited connectivity of the Bluetooth module, the application of the chip is limited to an apartment/building/society. The future goal is to use a cloud-based navigation system to provide a larger connectivity range. As the advancement in technology, a flexible chip

with performance-power-area optimization is aimed for the future. The features of the chip are kept limited to make it cost effective and used in everyday life, but research in increasing the features maintaining the low price is also aimed.

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