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Deriving equivalent structure of elements for low density parity check codes construction

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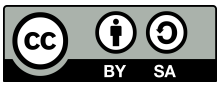
ABSTRACT

This paper proposes a method to derive equivalent coding structures of elements to construct low density parity check (LDPC) codes. We propose stairs LDPC (SLDPC) codes to demonstrate the effectiveness of the proposed method, which is expected to be beneficial for short block-length transmissions, but providing high coding rate. The equivalent coding structures are both for transmitter and receiver to: (i) reduce the encoding and decoding computational complexity, and (ii) search possibility of finding new coding scheme and observe their performances. We evaluate the validity of the method by confirming the equality in performances of the SLDPC codes in terms of bit-error-rate (BER) followed by investigation on their performance gaps to the Shannon limit via a series of computer simulations. The results show that the SLDPC codes have the same BER performance with that of the low density generator matrix (LDGM) codes confirming the validity of the proposed equivalent matrix derivation. This result indicates that different graphs can provide the same performances, because their equivalent matrices are the same. This result is expected to open new insight for the designing simple channel coding for short block-length LDPC codes having high coding rate for future less power consumption applications.



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1. INTRODUCTION

Telecommunications allows transmissions of data over long distances with constraints of low power consumption and the low error rate with the help of error correction codes (ECC). Supported by the information theory and coding theory, ECC is playing important role and is highly required to detect and correct errors caused by channel distortion and/or noise corruption [1]. According to Shannon channel coding theorem [2], the probability of error can be made arbitrarily small or close to zero, if the transmission coding rate R is less than or equal to the channel capacity C. Assuming that capacity C is achievable, we can calculate the minimum signal-to-noise power ratio (SNR) to reach zero error or arbitrarily small error, called Shannon limit, if $R \leq C$ is kept. If codes have close performance to the Shannon limit, the codes is said to have efficient transmissions, since for the given bit-error-rate (BER) level, the required SNR is smaller compared to the performance of uncoded case [2], [3].

Low density parity-check (LDPC) codes are a class of linear block codes in which the complexity of iterative decoding increases linearly with block-length [4]. As a result, LDPC codes have near-Shannon

limit performance on long block-length data transmission [5]. Gallager introduced regular LDPC codes with an equal distribution of "1" in each row and column of the parity-check matrix $\mathbf{H}$ [6], whereas Luby developed irregular LDPC codes with an unequal distribution of "1" in the matrix $\mathbf{H}$. It has been proven that irregular LDPC codes perform better than regular LDPC codes [7], [8].

The idea of using LDPC-like codes for short block-length transmission, e.g., Internet-of-Things applications has been proposed by [9] with Raptor codes based on LDPC and [10] based on low density generator matrix (LDGM), of which the optimal the degree distribution is investigated in [11]. However, the applications of LDPC for large block-length has been investigated to in [12] and [13] for Digital Video Broadcasting Terrestrial 2nd generation (DVBT2) and recently for the fifth telecommunication generation (5G) new radio and [14], where Raptor-like structure is used to have rateless coding scheme capability. Recently, we revealed that irregular degree distribution is more beneficial since we have additional degree of freedom to construct better LDPC-like coding scheme as in [15]. In this paper, we extract those benefits of irregularity to design better codes for short block-length transmissions.

The decoding process for LDPC codes uses a sum-product algorithm [16] exchanging the log-likelihood ratio (LLR). This algorithm is represented by a Tanner graph [17] involving variable nodes and check nodes. The check node receives the LLR from the variable node, which is subsequently returned to the variable node via a box-plus operation. This process is repeated until we obtain the desired outcome [18].

There are numerous problems in the data transmission process. Efficient data transmission is indicated by the low power consumption, but keep minimum errors [19]. Higher redundancy coding tends to perform better, but as the size of the data conveyed grows larger, so does the amount of power required [20]. Therefore, we introduce Stairs LDPC (SLDPC) codes, obtained from modification of the general simple LDPC for short block-length, to demonstrate the effectiveness of the equivalent structure derivation method. The coding structure is expected to help source compression to increase transmission efficiency. We also do this to increase R, resulting in a more reliable transmission system. However, because this can affect the error correction performance of the proposed codes, it is important to investigate which structures have smaller gap to the Shannon limit.

Therefore, this paper proposes equivalent structures for various compression structures to minimize encoding complexity. The equivalent structure is created by combining the two encoding procedures into a single, simpler step while keeping the transmitted bits unchanged. It is worth discussing here to investigate whether utilizing the equivalent structure improves SLDPC codes performance or not. The contributions of this paper are summarized as follows:

1. The idea of stairs in the SLDPC codes is presented that the parity check is used to "combine" the information bits such that higher coding rate is achieved.
2. The derivation of complex graph is presented using cascaded generator matrix and parity check matrix such that the equivalent structure is obtained to minimize the complexity the encoder and receiver. We found that complex graph can be simplified into a simpler graph having the same performance.
3. Validity of the derivation is confirmed using performance evaluation in terms of BER performance. We found that single parity check (SPC)-like codes are good for high coding rate.

The rest of this paper is organized as follows. Section 2 presents the system model of the transmission, where additive Gaussian noise (AWGN) channel is the main channel used for the evaluation. This section also propose the SLDPC codes with 4 structures to be evaluated and compared with the 3 well-known existing codes structures. Section 3 evaluates the proposed codes performances followed by conclusions in Section 4.

2. METHOD

In this section, we separate the discussion of methods into two subsections. Subsection 2.1. presents system model of the transmitter and receiver structure. Subsection 2.2. presents method to derive equivalent coding structures of elements to construct LDPC codes.

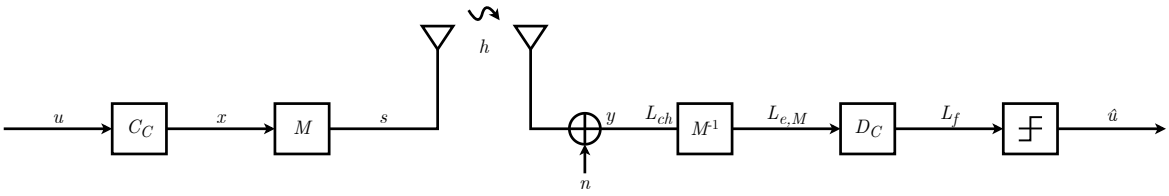


Figure 1. Transmitter and receiver structures of SLDPC codes.

2.1. System Model

A set of tests are presented in this paper to examine the error-correcting capability of SLDPC codes throughout data transmission. To maximize the coding rate, we introduce a concept of a compression structure followed by the equivalent structure. Figure 1 illustrates the system model considered in this paper.

The information bits u are random binary bits encoded in channel coding block C_C with a block length and various coding rates. The encoded bits x are then modulated by M to obtain s prior to the transmission by the antenna. At the receiver, the signal $\mathbf{y}$ experiences the channel h and corrupted by noise $\mathbf{n}$ resulting in

$$\mathbf{y} = h \cdot \mathbf{s} + \mathbf{n}. \tag{1}$$

The LLR of the channel

$$L_{ch} = \frac{2}{\sigma^2}\Re\{\mathbf{y}\} \tag{2}$$

is then demapped to obtain $L_{e,M}$ with $\Re\{\cdot\}$ being the operation to take the real part of y. The $L_{e,M}$ is then used by the SLDPC decoder D_C resulting L_f. Finally, hard decision is performed to obtain $\hat{u}$.

We use binary phase shift keying (BPSK) modulation since it has a simple modulation mechanism and a longer transmission range. This process changes the bit "0" to "1" and bit "+1" to "−1". The result of BPSK modulation is given by

$$s = \begin{cases} +1, \ x = 0 \\ -1, \ x = 1. \end{cases} \tag{3}$$

The modulation results s are then transmitted across the transmission channel.

We use additive white Gaussian noise (AWGN) channel as the transmission channels, however, extension to fading channel is rather straightforward by modifying (1). The terms of additive refers to noise that is simply superimposed or added to a signal without any kind of multiplication mechanism [21] and is the same regardless the frequency band inside the used bandwidth. Theoretically, the bit-error-rate (BER) of uncoded BPSK under the AWGN channels can be expressed as

$$P_{e,AWGN} = \frac{1}{2}\text{erfc}\left(\sqrt{\frac{E_b}{N_0}}\right) = \frac{1}{2}\text{erfc}\left(\sqrt{\frac{1}{2\sigma^2}}\right), \tag{4}$$

with $\frac{E_b}{N_0}$ being the energy bit per noise, which is used to confirm the validity of the computer simulation and the baseline of the performance comparison. The variance is given by [22]

$$\sigma^2 = 10^{-\gamma[\text{dB}]/10} \tag{5}$$

with γ being the SNR in dB. Since we use BPSK modulation, $L_{e,M}$ equals to L_{ch}. Interested readers on mapping other than BPSK can refer, for example, the demapper for bit-interleaved coded modulation (BICM). The $L_{e,M}$ is then used as the input of soft decoding process to return back information $\hat{u}$ from the received signal.

The sum-product algorithm is one of the optimal iterative decoding techniques in the logarithmic domain based on soft-decision. The "sum" represents operations on variable node (VND), which is the summation over all incoming messages. On the other hand, "product" represents operations on check node (CND), which is expressed using a "box-plus" operation, that perform a special multiplication over all the incoming messages. Figure 2 shows the operations for VND and CND, of which the outgoing message is $L_{e,\text{VND}}$ and

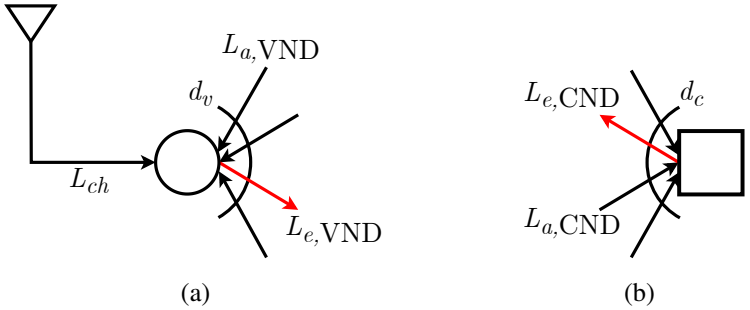


Figure 2. Principle of operations for (a) VND and (b) CND for equations in (6) and (8).

$L_{e,\mathrm{CND}}$, respectively. This figure also shows that L_{ch} is only connected to the VND, while the CND only depends on the $L_{a,\mathrm{VND}}$.

The operation on VND is divided into two parts, i.e., (i) extrinsic LLR and (ii) *a posteriori* LLR. The extrinsic LLR for the i-th edge outgoing from the VND is expressed as

$$L_{e,\mathrm{VND},i} = L_{ch} + \sum_{j=1,j\neq i}^{d_v} L_{a,\mathrm{VND},j}. \tag{6}$$

The symbol $L_{a,\mathrm{VND},j}$ is the j-th *a priori* LLR coming to the VND from CND with exception of $j \neq i$. The *a posteriori* LLR is calculated in the end of decoding after the number of iterations is assumed to be enough and is expressed as

$$L_{p,\mathrm{VND}} = L_{ch} + \sum_{j=1}^{d_v} L_{a,\mathrm{VND},j}, \tag{7}$$

where we omit the index i, since for the final process, we need only a single LLR for each desired symbol.

The box-plus operation at CND is expressed as

$$L_{e,\mathrm{CND},i} = \sum_{j=1,j\neq i}^{d_c} \boxplus L_{a,\mathrm{CND},j}, \tag{8}$$

where the box-pus arithmetic operation is given by [23]

$$L_1 \boxplus L_2 = \mathrm{sign}\left(L_1 \cdot L_2\right) \min\left(|L_1|, |L_2|\right) \tag{9}$$

for the case of two edges. Referring to (9), the box-plus operation is performed by multiplying the sign of L_1 and L_2, then multiplying it by the smallest absolute value of L_1 and L_2 [23]. This equation indicates that zero LLR coming to the CND should be avoided since all results are becoming zero causing no benefit in decoding. This is one of the reason that LT codes require more protections, for example, by using accumulator as in [15].

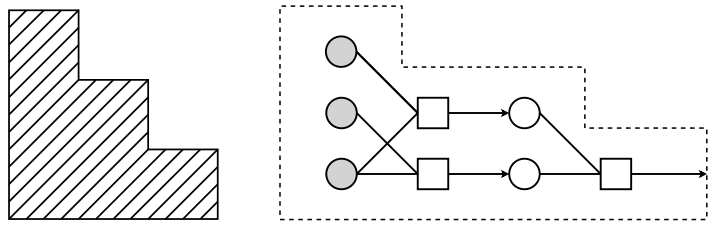
The outcomes of $L_{p,\mathrm{VND}}$ are then returned to bits using hard decision of

$$\widehat{u}_i = \begin{cases} 0, & L_{p,\mathrm{VND}} > 0 \\ 1, & L_{p,\mathrm{VND}} \leq 0, \end{cases} \tag{10}$$

where $\hat{u}_i$ is i-th bit of final decoding. In this paper, we use hard decision based on LLR as follows. If $L_{p,\mathrm{VND}}$ is greater than 0, $\hat{u}$ is 0. On the other hand, if $L_{p,\mathrm{VND}}$ is less than 0, $\hat{u}$ is 1. This is to be consistent with the mapping rule in (3).

However, because the focus of this paper is on the design of SLDPC codes with high coding rate, we start the design from the encoder graphically via a generator matrix $\mathbf{G}$ before converting it to matrix $\mathbf{H}$ using

$$\mathbf{G} = \left[-\mathbf{I}_k \quad | \quad \mathbf{P}\right], \quad \mathbf{H} = \left[\mathbf{P}^T \quad | \quad \mathbf{I}_{n-k}\right] \tag{11}$$



(a) (b)

Figure 3. Illustrations of (a) the stairs principle and (b) their realizations for data compression by CND.

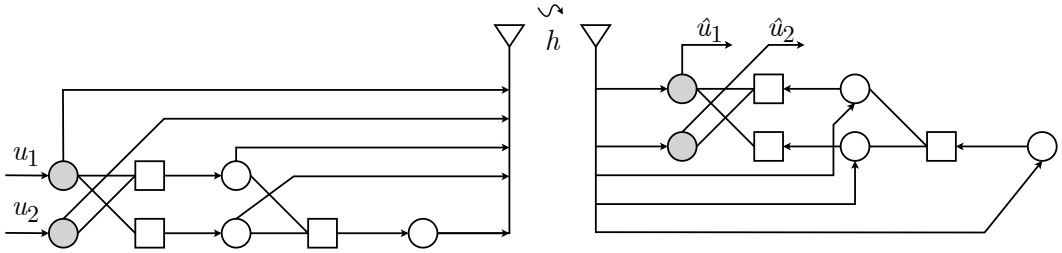


Figure 4. The graphical structure of SLDPC1 codes.

where $\mathbf{G}$ is $k \times n$ generator matrix, $\mathbf{I_k}$ is $k \times k$ identity matrix, and $\mathbf{P}$ is $k \times (n-k)$ designed matrix. This technique is similar to the design of LDGM codes [9], [10], however, in this paper, we seek the high coding rate and small block-length. The scalability of the codes can then be extended by using protograph-based extension technique [24].

2.2. Deriving the Equivalent Coding Structure

In this section, we present a method to derive equivalent coding structures of elements to construct LDPC codes using SLDPC as a toy example. The principle idea of SLDPC codes is presented and shown in Figure 3. Figure 3(a) illustrates the stairs principle representing a compression encoding to obtain higher coding rates to help transmissions of source compressed data. Figure 3(b) realizes how the CND can be used to compress the data such that higher coding rate is achievable.

We present SLDPC codes having 4 structures compared to the existing well-known coding schemes as shown in Figures 4–10, which are then summarized in Table 1. All structures are having unique properties and is intended for data compression such that rate is kept high. Please note that in this paper, we start the discussion on the structure from the generator matrix $\mathbf{G}$ with the graphical viewpoint prior to the conversion to parity check matrix $\mathbf{H}$.

2.2.1. SLDPC1 Codes Structure

Structure 1 of SLDPC codes, called SLDPC1 codes, shown in Figure 4, is the initial structure of the proposed SLDPC codes. Based on the structure of encoding processes, we split the generator matrix into

$$\mathbf{G}_{1l} = \begin{bmatrix} 1 & 0 & 1 & 1 \\ 0 & 1 & 1 & 0 \end{bmatrix}, \quad \mathbf{G}_{1r} = \begin{bmatrix} 1 & 0 & 1 \\ 0 & 1 & 1 \end{bmatrix}, \tag{12}$$

where $\mathbf{G}_{1l}$ is for the left part graph and $\mathbf{G}_{1r}$ is for the right graph at the transmitter side. We are now ready to convert matrices $\mathbf{G}_{1l}$ and $\mathbf{G}_{1r}$ into matrices $\mathbf{H}_{1l}$ and $\mathbf{H}_{1r}$, respectively, based on (11). The matrices $\mathbf{H}_{1l}$ and $\mathbf{H}_{1r}$ are therefore becoming

$$\mathbf{H}_{1l} = \begin{bmatrix} 1 & 1 & 1 & 0 \\ 1 & 0 & 0 & 1 \end{bmatrix}, \quad \mathbf{H}_{1r} = \begin{bmatrix} 1 & 1 & 1 \end{bmatrix}. \tag{13}$$

Since performing two decoding processes in (13) are considered to have higher decoding complexity, we propose to simplify it using the concept of Cascaded LDPC codes [25], such that we only have both a single equivalent $\mathbf{G}_{1eq}$ and $\mathbf{H}_{1eq}$.

We start from the equivalent matrix $\mathbf{H}_{1eq}$ since it is easy to construct as

$$\mathbf{H}_{1eq} = \begin{bmatrix} \mathbf{H}_{1l} & \mathbf{0}_a \\ \mathbf{0}_b & \mathbf{H}_{1r} \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 & 0 & 0 \\ 1 & 0 & 0 & 1 & 0 \\ 0 & 0 & 1 & 1 & 1 \end{bmatrix}, \tag{14}$$

where the $\mathbf{0}_a$ has the size of $k \times 1$, while $\mathbf{0}_b$ has $1 \times k$ adjusting the size of $\mathbf{H}_{1l}$ and $\mathbf{H}_{1r}$, where $k = 2$.

The matrix $\mathbf{H}_{1eq}$ represents VND and CND of the SLDPC1 codes. The number of VND and CND is equal to the number of columns k and rows n, respectively. Refering to (14), SLDPC1 codes are in the class of irregular LDPC codes due to unequal distribution of "1" in the matrix $\mathbf{H}_{1eq}$.

Similar to the case of parity check matrix case, the encoding generator matrix is also simplified into the equivalent matrix $\mathbf{G}_{eq}$, which is obtained from $\mathbf{G}_{1l}$ and $\mathbf{G}_{1r}$. The matrix $\mathbf{G}_{eq}$ can be obtained based on the cascaded principle as

$$\mathbf{G}_{1cascaded} = \begin{bmatrix} \mathbf{G}_{1l} & \mathbf{0}_x \\ \mathbf{0}_y & \mathbf{G}_{1r} \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1 & 1 & 0 \\ 0 & 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 & 1 \\ 0 & 0 & 0 & 1 & 1 \\ & & p_1 & p_2 & p_3 \end{bmatrix}, \tag{15}$$

where the $\mathbf{0}_x$ has the size of $k \times 1$, while $\mathbf{0}_y$ has $2 \times k$ following the number of row of $\mathbf{G}_{1l}$ and number of column of $\mathbf{G}_{1r}$, where $k = 2$.

The input length is only 2 bits, for example b_1 and b_2. The parity bits generated by $\mathbf{G}_{1l}$ are, therefore,

$$p_1 = b_1 \oplus b_2, \tag{16}$$

$$p_2 = b_1. \tag{17}$$

We then further adjust the matrix by locating the last parity check bit of $\mathbf{G}_{1r}$ in the last column of $\mathbf{G}_{1eq}$ such that the input length is kept 2 bits. The matrix $\mathbf{G}_{1r}$ indicates that the last generated parity check is

$$p_3 = p_1 \oplus p_2 = (b_1 \oplus b_2) \oplus b_1 = b_2. \tag{18}$$

Therefore, the last parity check in the matrix $\mathbf{G}_{eq}$ is $[0; 1]^T$ selecting only the bit b_2. The final equivalent generator matrix is

$$\mathbf{G}_{1eq} = \begin{bmatrix} 1 & 0 & 1 & 1 & 0 \\ 0 & 1 & 1 & 0 & 1 \end{bmatrix}. \tag{19}$$

Based on (19), the parity check matrix $\mathbf{H}_{1eq'}$ for SLDPC1 codes is

$$\mathbf{H}_{1eq'} = \begin{bmatrix} 1 & 1 & 1 & 0 & 0 \\ 1 & 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 0 & 1 \end{bmatrix}. \tag{20}$$

The last step is to confirm, whether the matrices in (20) and (14) is the same or not, since they are obtained from two different ways. $\mathbf{H}_{1eq}$ in (14) is obtained from cascaded $\mathbf{H}_{1l}$ and $\mathbf{H}_{1r}$, while $\mathbf{H}_{1eq'}$ in (20) is from the cascaded $\mathbf{G}_{1l}$ and $\mathbf{G}_{1r}$. Here, with Gauss-Jordan elimination by XOR-ing: (i) the first and the third rows followed by (ii) the second and the third rows, we obtain

$$\mathbf{H}_{1eq'} = \begin{bmatrix} 1 & 1 & 1 & 0 & 0 \\ 1 & 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 0 & 1 \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 & 0 & 0 \\ 1 & 0 & 0 & 1 & 0 \\ 1 & 0 & 1 & 0 & 1 \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 & 0 & 0 \\ 1 & 0 & 0 & 1 & 0 \\ 0 & 0 & 1 & 1 & 1 \end{bmatrix} = \mathbf{H}_{1eq} \tag{21}$$

confirming the equality of $\mathbf{H}_{1eq'} = \mathbf{H}_{1eq}$ and validity of the equivalent matrix. The coding rate of SLPDC1 codes is $R_1 = \frac{2}{5}$, since 2 bits are encoded into 5 bits as shown in Figure 4.

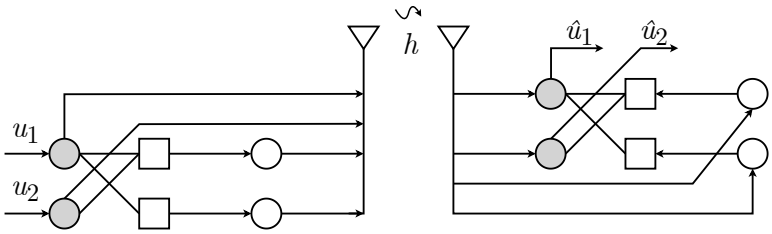


Figure 5. The graphical structure SLDPC2 codes.

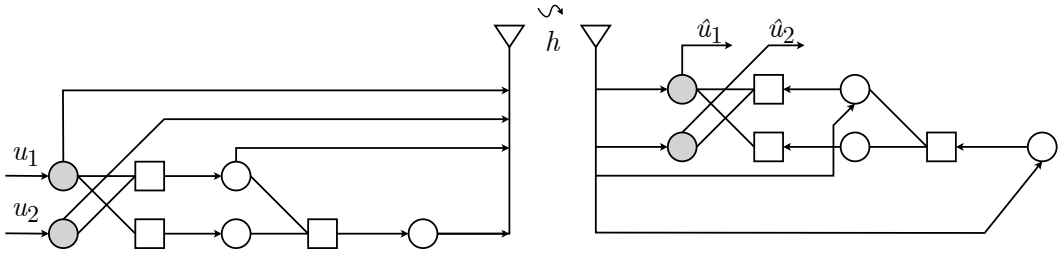


Figure 6. The graphical structure of SLDPC3 codes.

2.2.2. SLDPC2 Codes Structure

To obtain many possible high coding rate, we also propose the second structure of SLDPC codes, called SLDPC2 codes, as shown in Figure 5 with the coding rate of $R_2 = \frac{2}{4} = \frac{1}{2}$. This SLDPC2 codes are obtained from SLDPC1 codes by removing the last parity check of $\mathbf{G}_{1r}$. The generator matrix is

$$\mathbf{G}_2 = \begin{bmatrix} 1 & 0 & 1 & 1 \\ 0 & 1 & 1 & 0 \end{bmatrix} = \mathbf{G}_{1l}. \tag{22}$$

Please note that the VND in Figure 5 can be ignored since the degree is two, which is similar to a line. The parity check matrix for SLDPC2 codes is

$$\mathbf{H}_2 = \begin{bmatrix} 1 & 1 & 1 & 0 \\ 1 & 0 & 0 & 1 \end{bmatrix} = \mathbf{H}_{1l}. \tag{23}$$

It is interesting to observe here, whether the SLPDPC1 codes with additional parity check p_3 has better performance or not compared to this SLDPC2 codes.

2.2.3. SLDPC3 Codes Structure

We also propose the third SLDPC codes, called SLPDC3 codes, by modifying the SLDPC1 codes with removal the link of VND but keep the parity check CND as shown in Figure 6. The channel coding rate of SLDPC3 codes is $R_3 = \frac{2}{4} = \frac{1}{2}$, of which the generator matrix is the same as $\mathbf{G}_{1eq}$ in (19) except in the forth column, which should be removed, indicated by ~~$[1\ 0]^T$~~ in the 4-th column, due to the deletion of the link connecting VND and antenna. Therefore, the equivalent matrix is

$$\mathbf{G}_{3eq} = \begin{bmatrix} 1 & 0 & 1 & ~~1~~ & 0 \\ 0 & 1 & 1 & ~~0~~ & 1 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1 & 0 \\ 0 & 1 & 1 & 1 \end{bmatrix}. \tag{24}$$

The parity check matrix is, therefore,

$$\mathbf{H}_{3eq} = \begin{bmatrix} 1 & 1 & 1 & 0 \\ 0 & 1 & 0 & 1 \end{bmatrix}. \tag{25}$$

Please note that the matrix $\mathbf{G}_{3eq}$ and $\mathbf{G}_2$ is similar except at the last column suggesting their performances comparison is of our interest.

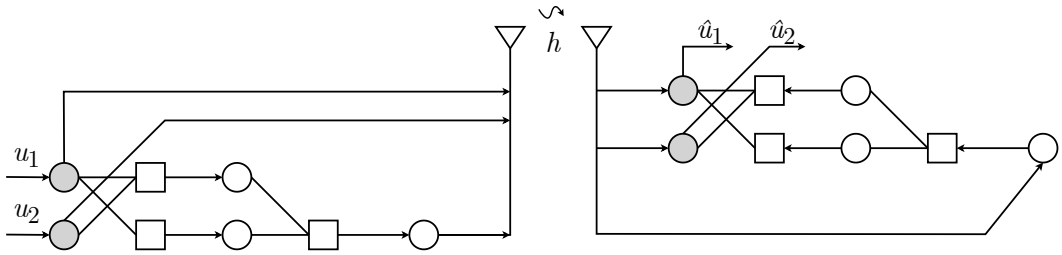


Figure 7. The graphical structure of SLDPC4 codes.

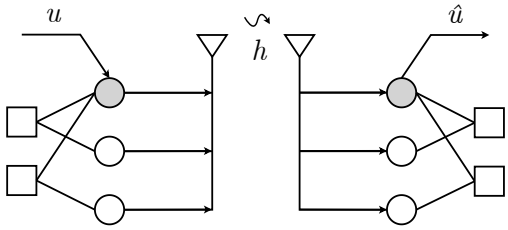


Figure 8. The graphical structure of Repetition codes.

2.2.4. SLDPC4 Codes Structure

To further reach the high coding rate, we further modify the SLPDC3 codes by removing the link Connection VND to the antenna, called SLDPC4 codes, such that the channel coding rate is $R_4 = \frac{2}{3}$ as shown in Figure 7. This SLDPC4 codes structure has the highest channel coding rate R among all the proposed SLDPC codes. The generator matrix is obtained by further deleting the third column of $\mathbf{G}_{3eq}$, indicated by $[1\ 1]^T$ in the 3-rd column, as

$$\mathbf{G}_{4eq} = \begin{bmatrix} 1 & 0 & 1 & 0 \\ 0 & 1 & 1 & 1 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 1 \end{bmatrix}. \tag{26}$$

The equivalent parity check matrix is, therefore, given by

$$\mathbf{H}_{4eq} = \begin{bmatrix} 0 & 1 & 1 \end{bmatrix}. \tag{27}$$

It is important to note here that the evaluation on the performance of SLDPC4 codes is important since $\mathbf{H}_{4eq}$ has zero element resulted, which is in general useless.

2.2.5. Repetition Codes Structure

To make our investigation complete, we also provide comparison with the existing famous Repetition codes, since the Repetition codes are simple and have easy adjustable coding rate. The structure of Repetition codes with rate $R_5 = \frac{1}{3}$ is shown in Figure 8 with the generator and parity check matrices are, respectively, given by

$$\mathbf{G}_5 = \begin{bmatrix} 1 & 1 & 1 \end{bmatrix} \text{ and } \mathbf{H}_5 = \begin{bmatrix} 1 & 1 & 0 \\ 1 & 0 & 1 \end{bmatrix}. \tag{28}$$

2.2.6. LDGM Codes Structure

In this paper, we also investigate a comparison of the proposed SLDPC codes with the existing well-known low density generator matrix (LDGM) codes. To keep comparable simple structure, we use LDGM with $R_6 = \frac{2}{5}$ as shown in Figure 9. The generator and parity check matrices of the considered LDGM codes are, respectively, expressed as

$$\mathbf{G}_6 = \begin{bmatrix} 1 & 0 & 1 & 0 & 1 \\ 0 & 1 & 1 & 1 & 0 \end{bmatrix} \text{ and } \mathbf{H}_6 = \begin{bmatrix} 1 & 1 & 1 & 0 & 0 \\ 0 & 1 & 0 & 1 & 0 \\ 1 & 0 & 0 & 0 & 1 \end{bmatrix}. \tag{29}$$

Table 1. Summary of the proposed SLDPC codes and the existing well-known codes.

No	Codes	Matrix $\mathbf{G}$	Matrix $\mathbf{H}$	Rate R
1	The proposed SLDPC1	$\mathbf{G}_{1eq} = \begin{bmatrix} 1 & 0 & 1 & 1 & 0 \\ 0 & 1 & 1 & 0 & 1 \end{bmatrix}$	$\mathbf{H}_{1eq} = \begin{bmatrix} 1 & 1 & 1 & 0 & 0 \\ 1 & 0 & 0 & 1 & 0 \\ 0 & 0 & 1 & 1 & 1 \end{bmatrix}$ $\mathbf{H}_{1eq'} = \begin{bmatrix} 1 & 1 & 1 & 0 & 0 \\ 1 & 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 0 & 1 \end{bmatrix}$	$\frac{2}{5}$
2	The proposed SLDPC2	$\mathbf{G}_2 = \begin{bmatrix} 1 & 0 & 1 & 1 \\ 0 & 1 & 1 & 0 \end{bmatrix}$	$\mathbf{H}_2 = \begin{bmatrix} 1 & 1 & 1 & 0 \\ 1 & 0 & 0 & 1 \end{bmatrix}$	$\frac{2}{4}$
3	The proposed SLDPC3	$\mathbf{G}_{3eq} = \begin{bmatrix} 1 & 0 & 1 & 0 \\ 0 & 1 & 1 & 1 \end{bmatrix}$	$\mathbf{H}_{3eq} = \begin{bmatrix} 1 & 1 & 1 & 0 \\ 0 & 1 & 0 & 1 \end{bmatrix}$	$\frac{2}{4}$
4	The proposed SLDPC4	$\mathbf{G}_{4eq} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 1 \end{bmatrix}$	$\mathbf{H}_{4eq} = \begin{bmatrix} 0 & 1 & 1 \end{bmatrix}$	$\frac{2}{3}$
5	Repetition	$\mathbf{G}_5 = \begin{bmatrix} 1 & 1 & 1 \end{bmatrix}$	$\mathbf{H}_5 = \begin{bmatrix} 1 & 1 & 0 \\ 1 & 0 & 1 \end{bmatrix}$	$\frac{1}{3}$
6	LDGM	$\mathbf{G}_6 = \begin{bmatrix} 1 & 0 & 1 & 0 & 1 \\ 0 & 1 & 1 & 1 & 0 \end{bmatrix}$	$\mathbf{H}_6 = \begin{bmatrix} 1 & 1 & 1 & 0 & 0 \\ 0 & 1 & 0 & 1 & 0 \\ 1 & 0 & 0 & 0 & 1 \end{bmatrix}$	$\frac{2}{5}$
7	SPC	$\mathbf{G}_7 = \begin{bmatrix} 1 & 0 & 1 \\ 0 & 1 & 1 \end{bmatrix}$	$\mathbf{H}_7 = \begin{bmatrix} 1 & 1 & 1 \end{bmatrix}$	$\frac{2}{3}$

2.2.7. SPC Codes Structure

Since the well-known single parity check (SPC) codes are having high coding rate of $R = \frac{k}{k+1}$ with k being the information bits, we also investigate the performances of the proposed SLDPC codes compared to the SPC codes. Figure 10 shows the SPC codes structure used in this paper, where the channel coding rate is $R_7 = \frac{2}{3}$, since we select $k = 2$ bits. The generator and parity check matrices of the $(2, 3)$ SPC codes are, respectively, given by

$$\mathbf{G}_7 = \begin{bmatrix} 1 & 0 & 1 \\ 0 & 1 & 1 \end{bmatrix} \text{ and } \mathbf{H}_7 = \begin{bmatrix} 1 & 1 & 1 \end{bmatrix}. \tag{30}$$

We summarize all coding schemes and their corresponding channel coding in Table 1 with their corresponding generator and parity check matrices $\mathbf{G}$ and $\mathbf{H}$, such that their differences are also comparable and visible.

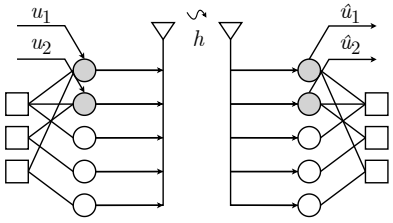


Figure 9. The graphical structure of LDGM codes.

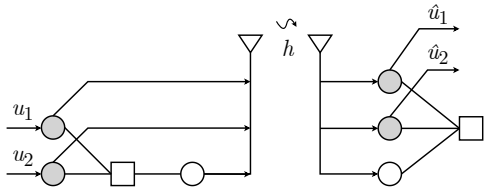


Figure 10. The graphical structure of SPC codes.

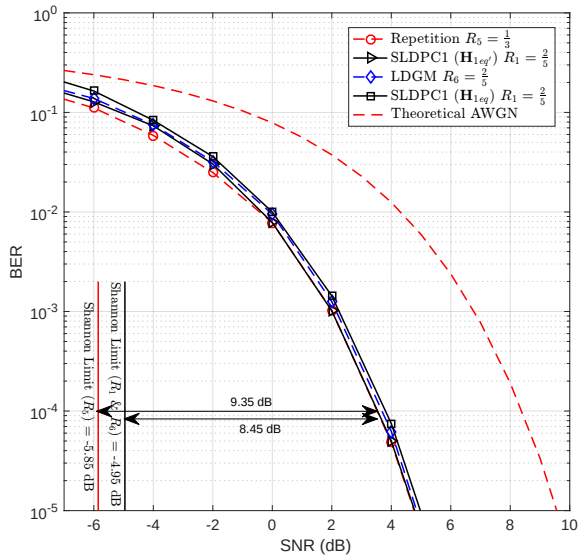


Figure 11. BER performances of SLDPC codes under AWGN channels.

3. RESULTS AND DISCUSSION

In this section, we present performance evaluation in terms of BER under AWGN channels. We have conducted a series of computer simulations to figure out the performances of the proposed SLDPC codes and find the best SLPDC coding structure among 4 possible structures. We use signal-to-noise power ratio (SNR) ranging from -7 to 10 dB under the AWGN channels and the corresponding coding rates R in Table 1. As a baseline comparison, we use the theoretical BER performances of AWGN channel to confirm the validity of our simulations and the performances comparison to the proposed SLPDC codes. We present the simulations result into two figures of BER performances to make the BER curves visible and comparable. We also plot the Shannon limit of

$$\gamma_{\text{Lim}} = 10 \cdot \log_{10}(2^R - 1) \tag{31}$$

with γ_{Lim} being the SNR minimum to be theoretically achieved with the given channel coding rate R from channel capacity

$$C = B \cdot \log_2(1 + \gamma) \tag{32}$$

with B being the bandwidth to fairly evaluate the efficiency of each coding structure. The limit is said to be achieved when $C = R$ for arbitrarily small BER. Figure 11 depicts the BER performances of SLDPC1 with $\mathbf{H}_{1eq}$, SLDPC1 with $\mathbf{H}_{1eq'}$, Repetition, and LDGM codes, while BER performances of SLDPC2, SLDPC3, SLDPC4, and SPC codes are shown in Figure 12 completed by the Shannon limits for the corresponding rates.

We performed soft iterative decoding for all coding structures. The iteration process is carried out by repeating the sum-product algorithm until a steady LLR value is reached. Since the other structures had reached a stable LLR value by the time of the first iteration, we only repeated the iteration process for SLDPC1 and LDGM codes. Figure 11 shows BER performances evaluated in terms of SNR(dB), where the Repetition codes has gap of 9.35 dB to the Shannon limit, while SLDPC1 codes with $\mathbf{H}_{1eq'}$, LDGM codes, and SLDPC1 codes with $\mathbf{H}_{1eq}$ have the same gap of 8.45 dB. All gaps are measured at BER level of 10^{-4}. The results show that different bipartite graphs of SLDPC1 codes and LDGM codes can provide the same BER performances indicating that the proposed method of equivalent structure derivation is correct.

Figure 12 shows that SPC codes have the best performance indicated by the smallest gap of 8.01 dB. SLDPC2 and SLDPC3 codes have better BER performance compared to SPC but have less efficiency. Figure 12 also shows that SLPDC2 and SLDPC3 codes have the same performances because the generator and parity check matrices is the same. The SLDPC4 codes have high rate but the performance is the worst with gap of 10.31 dB. This is because $\mathbf{H}_{4eq}$ in (27) has zero element for a single parity check meaning that LLR to that VND is useless.

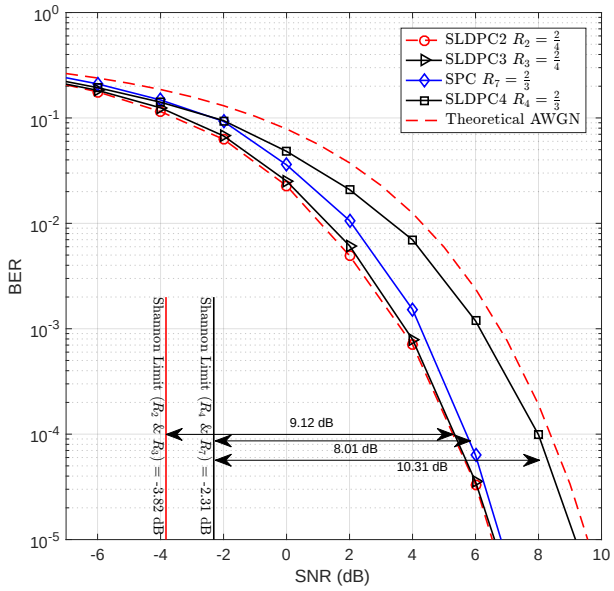


Figure 12. BER performances of SLDPC codes under AWGN channels.

4. CONCLUSION

In this paper, we have proposed a method to derive equivalent coding structures of elements using SLPDC codes that can be extended to help the construction of larger LDPC codes for short block-length transmission applications. We used the cascaded principle to construct the equivalent generator and parity-check matrix that is also beneficial for minimizing the computational complexity of the encoder and decoder. The equivalent structure of $\mathbf{G}$ can be obtained from the cascading of two (or more) matrices by modifying the second matrix to have identity matrix with size of parity check length and shifting to the right k bits. On the other hand, the equivalent structure of $\mathbf{H}$ can be obtained by just cascading directly the second matrix and shifting to right k bits. We have evaluated the validity of the proposed method by confirming the equality in performances of the SLDPC codes and other well-known coding scheme under the AWGN channel. According to the simulation results, the proposed method is valid since SLDPC1 codes have the same BER performance with that of LDGM codes. Although some bipartite graphs are different to each other, they can share the same equivalent matrix and provide the same performances indicating that the equivalent structure derivation is important. Among all the channel coding structures evaluated in this paper, we found that SPC codes are the most efficient codes (for the given block-length) since SPC codes have the smallest gap to the Shannon limit. The results in this paper are expected to provide new insight for the designing simple channel coding of short block-length LDPC codes having high coding rate for future less power consumption applications.

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