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Fault simulation for design for testability inserted designs

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ABSTRACT

Systematic design for testability (DFT) is a technique to enhance the testability of design so that it is further organized and self-regulating. The objective of systematic DFT is to enhance a circuit's operability and evidence. This can be performed in a variety of ways. The scan pattern method is the extremely predominant, and it modifies the design's internal sequential circuitry. In this manuscript, frequently used industry standard functional register-transfer level (RTL) designs are chosen. Structured DFT approach is adopted to do scan insertion and automatic test pattern generation (ATPG) to enhance the testability. Proposed methodology provides the controllability and observability for the clocks and reset used in chosen RTL designs by eliminating S rule and D rule violations by adding test logic. Also able to insert stuck at faults and achieve fault coverage of 97.78% and test coverage of 99.26% for DFT architecture for Wallace tree multiplier design, and found different classes of faults as testable and untestable faults and also performed fault simulation for the intended designs to detect fault from the created deterministic patterns.

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1. INTRODUCTION

In the process of designing a hardware product, “design for testability” conversely “design for test” acronymic as DFT comprises Integrated circuit (IC) design proficiencies that includes analysis characteristics that is considered to be an advantage. These appended characteristics results in much simpler approach to develop and employ industrial production analyses are required with the intention of hardware layout. DFT often is associated with pattern transformations that allow enhanced approach to the elements in the internal circuit components in a manner that the specific intrinsic conditions be able to monitored, furthermore noticed effortlessly. In the current trend, extremely complicated patterns, majority of the logic gates are deep down embedded even though the test facilities are attached to the essential input as well to the outputs (I/Os) in addition to some actual test positions. The included logic gates, supposed to be handled through intermediary levels of logic. If the intermediary logical system includes state components, subsequently the issue of an aggressively increasing manner and state transition sorting generates a problem that is challenging to resolve for the trial creation. To make trial creation a cumbersome free process, DFT deals with the accessibility issues by eliminating the necessity for complex state changeover sorting, in the attempt to control as well to observe the occurrences at certain inner circuit component. Scan is an approach for scan design, intended to substitute all memory components in the design with the scannable correspondents. All the scans are will be linked into a chain called scan chains. The conception is to regulate and follow the estimates in all the design’s memory components. For a combinational circuit, memory components can be resulted in origination of sequential test circuits and error model analysis.

The intention of automatic test pattern generation (ATPG), is for developing a set model with intention to accomplish definite level of test report. The test report is the overall percentage of flaws that will be subjected for testing and error coverage is the overall percentage of testable errors. The two major steps are involved in ATPG, they are: pattern creation and simulation support for fault detection that identifies fault patterns. "Mentor graphics" has developed a ATPG tool that has amalgamated aforementioned steps into a one-step process of ATPG. The procedure is sophisticated to generate patterns that can be custom built based on the tester's requirement, this enables the tester to position the design data into a integrated circuit with scan storage.

Substantial research attempts by several groups are observed in order to minimize the power dissipation at the time of initial steps and apprehension of at-speed testing. The authors have mentioned few considerable published manuscripts that supports the proposed work and the shortcomings of the earlier published work. Saeed and Sinanoglu [1] the proposed approach had given assistance over DFT that was supposed to reinstate the load state in user interface registers amongst launch/capture operations in the patterned regions, allowing decreased power in launch of capture (LOC), launch on shift (LOS) and combined at-speed testing. In this manner, a group of that have been optimised for cost and quality can be utilized as it was obtained. However, this was obtained by compromising with area cost by keeping test flow and optimality are preserved. DFT was proposed for three scan designs with intention to reduce test application times by Hosokawa *et al*. [2] from the research results it was evident that the schemes of DFT, it decreased the test utilization times by 46% to 82% matched with a conventional full scan design method. Despite that there was requirement for a better algorithm with test point insertion to decrease the number of test points and also there was scope for built-in self-test (BIST).

The big concern for the very-large-scale integration (VLSI) industry is faults due to power related problem that the time of scan testing and high probability of introducing redundant loss and the other reason would be time. An attempt was made to address insertion related to scan and flow based on ATPG that has been one of the enhanced criteria by employing more or less a competent method such as engineering change order (ECO) as well by using 28 nm technology on which fault grading method will be implemented. This results in originating test vectors equally for faults transitions also to stuck. Although attempts have been made to address several issues but as the solution is moved towards technology that has lower number of nodes. This will result in more and more difficulties to include DFT in any design [3].

As mentioned in the previous discussion, designing automated testing is required. However, a hybrid ATPG was proposed by employing staggered LOC. A coordinated LOC system, out of the two aligned types launch and capture whichever is suitable will be chosen in the scan test for synchronous domain tests. The hybrid ATPG resulted in reduction of test pattern count from 1.7X to 2.1X and it also gave rise to increase in ATPG runtime closely by 10% to 50% when it was correlated with one-hot type alone. This was achieved as one-hot clocking will always be utilized after staggered clocking, leading for no loss in fault report in the hybrid testing. This approach failed as the parameters of the previously existing approach did not match with the proposed approach, as the existing work had the potential to be applied for all synchronous clock domains [4]. In hybrid ATPG switches alternative approach was proposed, from the staggered type to one-hot type post determined proportion of errors have been processed. This decreases time required for ATPG by compromising slightly with the rise in design count. There is lot of scope for selection switch ratio in automatic manner [5].

As the usage of integrated circuits are increasing in various domains, identification and correction of faults will be important parameter, that helps in meeting the quality of the test to the expectations. One of the familiar methods to increase the coverage of the faults is by introducing test points that intensifies the capability of the logic's controllability and observability. ATPG method are established on optimization-satisfiability (SAT) are applied to measure a minimal group of effectual test points. This enables to form all previous unnoticeable errors of a group named 'F' that was traced. It was evident from the experimental results that the proposed minor group test points, it presented 100% error report for stuck-at errors. But the results are not available for the error group that has large group test points [6].

Efthymiou *et al*. [7] proposed a 3φ level sensitive scan design (LSSD), it was mentioned by implementing the aforementioned approach, automation of insertion of scan and ATPG were implemented effortlessly in asynchronous circuits. It was tested for smaller number of groups of test patterns for the interconnect. It was observed the complete coverage of test was around 99%. However, there were no experimental proofs to support the same bring implemented for larger pattern type, where its coverage could be proved. Several tools including the open source are mentioned in Abdelatty *et al*. [8] for ATPG, scan chain testing, insertion scan and faults.

To compute the fault coverage in digital circuits, register transfer level (RTL) approach was proposed. The outcome of achieved using the proposed methodology, fault covering was established with the help of the fault model generated using RTL that was compared with the fault detection in the gate level. However, this approach was not tested on the complex sequential circuits [9]. Another principal objective of

RTL is to cut the time required for DFT that in turn reduces the time to market. This will also open the doors for the current functional path between sequential elements in the original circuit for beginning scan chains [10]. To overcome the aforementioned problem an alternative approach was proposed and it is by implementing extended weighted transition metric (eWTM). It was employed to direct the scan chain pattern computation that can approximation of the power change in shift in as well as shift out [11]. Effectual algorithms that provided more dependent testability of VLSI chip using fusion of RTL stye with full scan chain method along with ATPG. It as well includes and explains the approach of allocating DFT connections connected with scan chain for the purpose to decrease the cost of packaging because of DFT were proposed by Lo *et al*. [12].

Security is one of the important parameters in that need to be improved considerably that needs to be improved by modifying the key for all test condition vectors. This will also give information related to the location of the bit in test vector by claiming the effective possibility out of accessible test vector created by multi polynomial linear feedback shift register (LFSR) [13]. It is well-known that flip-flops are memory units, using this a method was proposed to integrate Q-flop component for the purpose of normal synthesis and the flow of the DFT. This allows insertion scanning into the Q-flop registers. Very minimal increase in the experiential values were observed in the testable version compared with the actual Q-flops. Considering, in the circuit that were tested numeral synchronizers were characteristically small when compared with the other memory elements. Complete pattern automation is possible in the proposed method; however, this also results in rise in critical components testability that confirms the proper behaviour of a circuit that is still needed to established [14]. A technique was proposed to check for the double error without completing the path fully and the method was competent. Single error test set is sufficient to detect the double error that are present, and only the double errors that are untouched which will be recognised by the path of traverse of single errors [15].

A novel test point insertion methodology was proposed by Lin *et al.* [16] and it resulted to be a low operating cost scan pattern technique to create scan paths with the help of functional logic. Lot of scope has been observed in the domain of decreased area or timing reduction, in this direction considerable attempts were made and the same was evident with the experimental results. If some mismatch in the shift in and shift out was observed that would directly convey the presence of an error in the circuit. The shortcoming of this work was failing to examine the data of scan-out, as few errors would disturb the error free scan chain that can be tested prior implementing scan chain.

A two-level process, where insubstantial synthesis with models of graph were combined concluding logical approximation from the pattern, later implementing typical estimation of methods for the traveling salesman challenge to decide the scan-stitching classification. The work scope lot of advancement that includes piling of local and global optimization parameters, challenge of power while testing has been discussed to in Zaourar *et al*. [17]. Employing DFT has been discussed in short by employing 28 nm technique, this also comprises of insertion scan and creation of patterns so that it can be implemented for a specific design. In this manuscript several other demanding parameters were discussed, are the ones that ASIC industry are going through in recent days [18].

Specifically, a methodology was designed for indigenous scan cell style for low-power scan with high efficiency with respect to power. This offers clarification for decreasing the complete mean power in set of two that is scan cell and combinational part at the time of capture and shift mode [19]. Error report was scaled for estimation of the errors that are called stuck-at range of visionary test sequences that is introduced by evading sequential error simulation [20]. This paper proposes novel lfsr method to reduce number of transitions which appear at scan inputs implemented on circuit under test. Multiple input signature register (MISR) is used to receive compressed test responses and able to save test power by 7 % without increasing length of test sequences [21]. Goswami *et al*. [22] Path oriented methods produce accurate atspeed patterns without any limitations and it is performed on five industry standard designs. A design to detect faults on security operation center (SOC) which comprises on chip clock controller and Patterns are generated by ATPG tool and Design verification is done on synopsis tool were proposed by Lin and Shi [23].

Complete on-chip power depreciation was showcased by employing nonlinear-feedback shift register (NLFSR) as design creator and it was used instead of LFSR. ATPG was accomplished by employing synopsys Tetramax tool. In the aforementioned NLFSR method, error was introduced manually and designs were added to the circuit under test (CUT) to obtain the error report [24]. A novel method of raising the unidentified bits (usage of n-detect relaxed algorithm). The process is analysed using the S27 Benchmark circuit, where single Stuck-at-faults are introduced at random and the test is run using a 4-bit sequence pattern with 16 variations. Using LFSR, these patterns are produced at random. The created patterns are then run across the complete circuit and contrasted with the component faults that are present, either at the input or output. If the component response and the pattern response agree throughout the comparison, the

component is regarded as fault-free. Detection and diagnosis of faults were proposed by Dhiliban and Govindaraju [25].

As it is evident several considerable works are available in this domain and they are mentioned above. An attempt has been made by the authors here to overcome the abovementioned drawbacks by employing scan inserted netlist approach. This is discussed in detail in multiple sections and it the sections are proposed method, proposed solution, results and discussion and lastly conclusion of the work proposed.

2. METHOD

In this section proposed methodology is discussed for the intended research work. Figure 1 shows the flow diagram for generic systematic design for testability. Flow diagram elaborates on test flow for detection of faults through efficient scan insertion and deterministic ATPG methods. Fault simulation is performed for the fault list found by adding stuck at and transition type faults. Steps describe the entire flow.

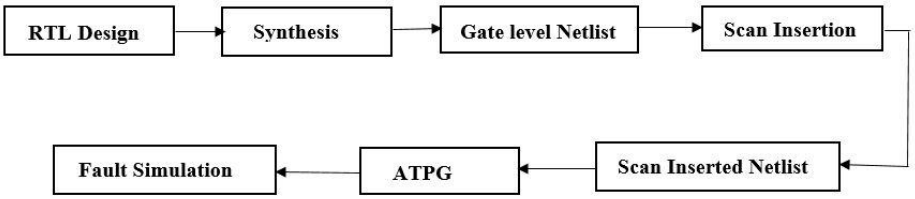

Figure 1. Generic DFT flow

2.1. RTL design

Here two functional RTL designs are chosen. The RTL designs are:

- DFT architecture for 16-bit shift register
- DFT architecture for Wallace tree Multiplier

2.1.1. Design 1

DFT architecture for 16-bit shift register. Top module name is dft_arch_top. This design has 30 s1 violations and 15 D5 violations (unstable non scan cells when clocks are off). There are 153 sequential cells. 138 sequential library cells are scannable. Number of transparent latch is one.2 scan clock/set/reset have been identified. All scan clocks successfully passed off state check. 138 sequential cells passed clock stability checking. 16 non scan memory elements are identified. In that 15 non scan elements are identified as INIT-X.1 non scan memory element as TLA.

- S1 violation: Set and reset including clocks are not at off states in design 1. Hence, S1 rule is violated.
- D5 violation: Non scan flipflops are found even when clocks are off in design 1. Hence D5 rule is violated.

Proposed solution: The concept of test logic insertion is used to resolve this issue. Test logic is the circuitry that the tool adds to improve the testability of a design. The command "set test logic" inserts test logic to control the set, reset, clock, enable or write control signals to make them scannable when scan chains are inserted. The command used to fix the issue in this case is: "set test logic -set on -reset on -clock on". This command is used in the dofile to get control over clock set and reset; tool has tied the value to logic value X to set and reset paths to get controllability on the clocks.

2.1.2. Design 2

DFT architecture for Wallace tree multiplier. Top module name as: lfsr_wallace_arch_top. It has 26 sequential elements. Cell instances=613 and gates 1009, PIs=19,POs=34. This design has no violations. 2 scan clock/set/reset have been identified. All scan clocks successfully passed off state check. 26 sequential cells passed clock stability checking.

2.2. Synthesis

Synthesis is a process to convert RTL design into gate level netlist. Here, synthesis of RTL designs was done using design compiler using 14 nm technology, which is power, area and time efficient. Steps to perform synthesis are:

- Read RTL design
- Read SDC file (synopsis design constraints)

- Invoke DC-shell to obtain gate level netlist
- File format of netlist is filename.gn

2.3. Gate level netlist

For DFT, initially gate-level netlists are generated, post netlist generation insertion of scan chain is performed. All standard cells and macros are connected sensibly as information of this is stored in Netlist, also it offers the specifics of nets and connectivity. The file format for gate level netlist is. v and .vg files.

2.4. Scan insertion

Scan circuitry makes test generation easier and reduces the need for external testers. Internal scan and boundary scan are the two primary types of scan techniques. Here Internal scan, often known as scan design, is a method of increasing testability by modifying the circuitry of a design internally.

The design now contains two more inputs, sc in and sc en, as well as one new output. sc out, an extra output. When shifting is enabled (the sc en line is active), scan data is read in from the sc in line, which replaces the original memory components. The operating procedure of the scan circuitry is as shown in:

- Enable the scan operation to allow shifting (to initialize scan cells).
- After loading the scan cells, hold the scan clocks off and then apply stimulus to the primary inputs.
- Measure the outputs.
- Pulse the clock to capture new values into scan cells.
- Enable the scan operation to unload and measure the captured values while simultaneously loading in new values via the shifting procedure (as in step1).
- Inputs to scan insertion are Synthesis Netlist, Library Model, Do file commands.
- Outputs of scan insertion, Scan inserted Netlist, ATPG Do file, ATPG Test proc, Scan Def.

2.4.1. Scan design rules

The two basic checks performed by the tessent tool are:

- It ensures all the defined clocks including set and reset are at their off states, where sequential element remain stable and inactive.
- It ensures for each defined clocks can capture data when all other defined clocks are off.

2.4.2. Scan design rule violation

Types of violations:

- Violation that prevents scan insertion because of uncontrolled clocks and reset.
- Violation that prevents data capture because clock is used as data or black box is feeding clock or synchronous signal.
- Violation that reduces coverage because combinational feedback loop or black box.

2.5. ATPG

The aim of ATPG is to generate a set of designs that realizes a given test report in which test report is the complete proportion of testable errors the design set essentially notices. ATPG consists of two main steps: i) design creation and ii) execution simulation to determine the error patterns. The two furthermost characteristic approaches for design creation are arbitrary and deterministic.

Stuck at faults: When a signal, or gate output, is stuck at a 0 or 1 value, independent of the inputs to the circuit, the signal is said to be "stuck at" and the fault model used to describe this type error is called a "stuck at fault model". ATPG- STUCK-AT Steps:

- Read scan inserted netlist and test procedure files.
- Read the Library model.
- Do file provides the commands to add stuck at faults and generate serial and parallel patterns.

2.6. Fault simulation

The purpose of fault simulation is to determine the fault coverage of the current pattern source for the faults in the active fault list. The purpose of "good" simulation is to verify the simulation model. Typically, you use the good and fault simulation capabilities of the ATPG tool to grade existing hand-or ATPG-generated pattern sets.

The following subsections discuss the procedures for setting up and running fault simulation using the ATPG tool; Fault simulation runs in analysis mode without additional setup. You enter analysis mode using this command: SETUP> set_system_mode analysis.

The steps to perform Fault simulation:

- Fault type designation
- Faults list creation
- Pattern source designation
- Fault simulation execution

3. RESULTS AND DISCUSSION

3.1. Design 1

Design name is DFT architecture for 16-bit shift register. Top level Module named as dft_arch_top which is shown in the Figure 2 it has four inputs named as clk, ld_lfsr, ld_lfsr_values and rstn .it has four outputs as Fail, Pass, r_out and shift_reg_out. This top schematic view is obtained after doing RTL simulation of the design 1 using Questasim tool.

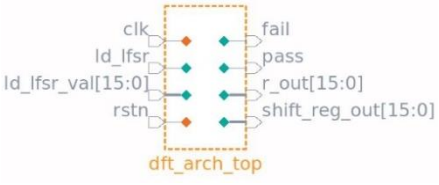

Figure 2. dft_arch_top schematic

3.1.1 Description of design 1

Description of design 1 is obtained by performing Scan insertion on design 1 using tcl scripting by adding scan logic to each and every node of the design by adding 5 scan chains by converting normal flip flops into scannable flipflops using DFT libraries in tessent tool. But violations have occurred in the design which is cleared by adding test logic which are reported in detail:

- Number of shift registers flops recorded for scan insertion is 143
- Number of shift registers recorded for scan insertion is 16
- Longest shift register has 23 flops
- Shortest shift register has 8 flops
- Potential number of nonscan flops to be converted to scan cells is 16
- Number of targeted sequential library cells is 153
- Reading group test procedure file. dft_arch_top.testproc
- Simulation of load and unload procedure completed after scan insertion
- 153 scan cells are identified in 5 scan chains
- Longest scan chain has 31 scan cells

In Figure 3 there is D5 violation is shown for one of the dffsr design where unstable non-scan cells are seen where clocks are off. In Figure 4, D5 violation are resolved by adding test logic, by tieing logic value to X i.e TIEX by taking controllability and observability of clock set and reset. In Figure 5 S1 violation is shown for dff design named as lfs_reg [5]. Figure 6 shows solution by adding test logic by tieing the logic value to X,ie TIEX inturn get controllability and observability of clocks set and reset paths.

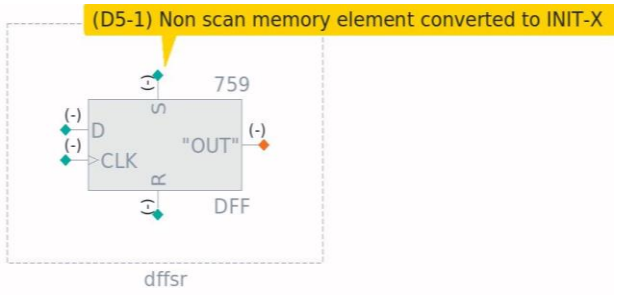

Figure 3. D5 violation

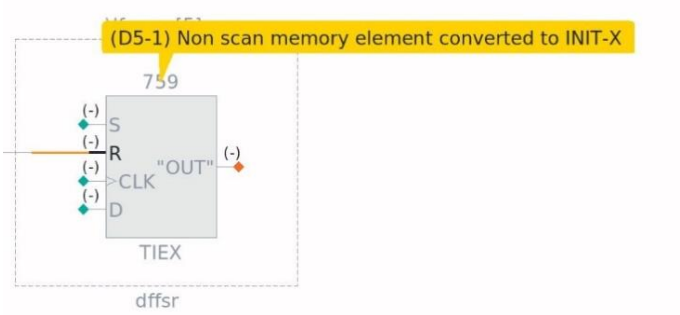

Figure 4. Solution to D5 violation

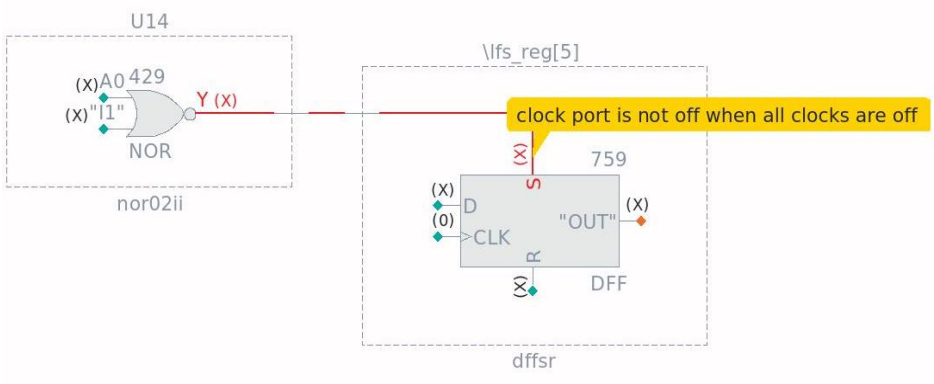

Figure 5. S1 violation

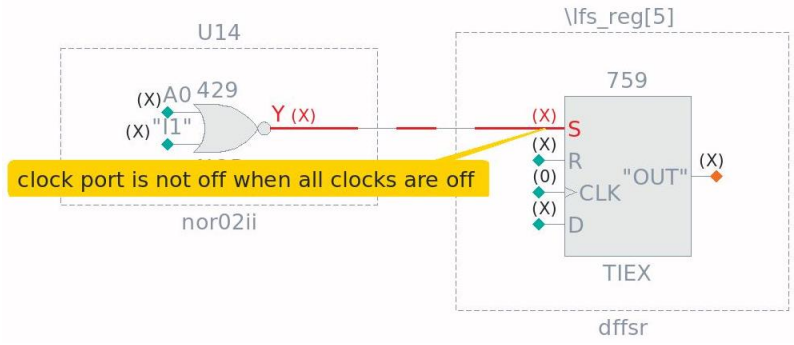

Figure 6. Solution to S1 violation

3.1.2. Serial Fault Simulation for Design 1

Here Faults are simulated one by one, so serial fault simulation takes many clock cycles to obtain the patterns. Serial Fault Simulation is performed from the fault list obtained for design 1. As a result, error is found in simulated and Expected waveform in 46 th cycle in ts so [1] which is indicated in Figure 7. In this expected was 1 but got 0 which is depicted as error. Fault list for design 1 shows all internal possible faults of stuck at type in design 1 which is indicated in Figure 8.

Commands to find fault list are listed as shown in:

```
add_ faults –all
write_faults
report_faults
type indicates whether pin is stuck at 0 or stuck at 1
code indicates fault classes
pin_pathname indicates names of pin in design 1
```

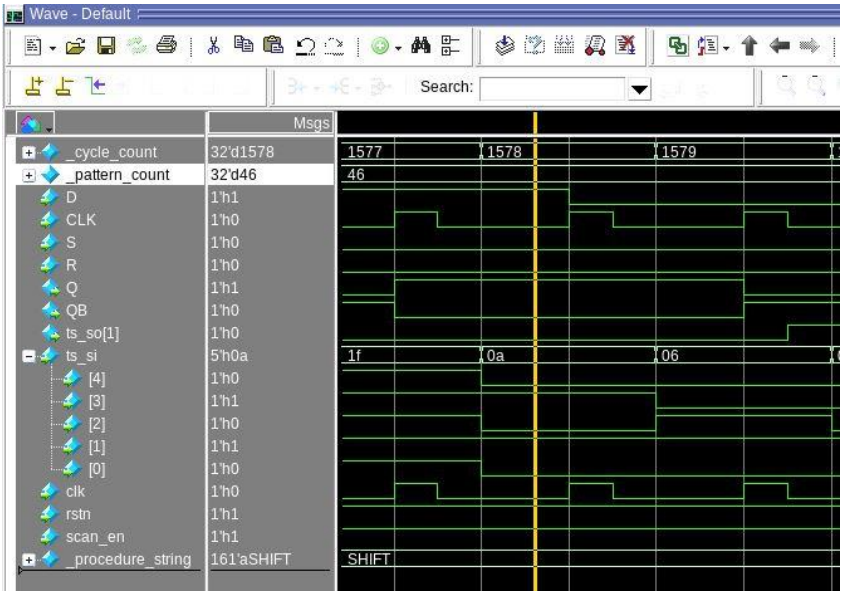

Figure 7. Serial fault simulation for design

type	code	pin_pathname
0	DI.CLK	/clk
1	DI.CLK	/clk
0	DS	/rstn
1	DS	/rstn
0	DS	/ld_lfsr
1	DS	/ld_lfsr
0	AU.PC	/ld_lfsr_val[15]
1	AU.PC	/ld_lfsr_val[15]
0	AU.PC	/ld_lfsr_val[14]
1	AU.PC	/ld_lfsr_val[14]
0	AU.PC	/ld_lfsr_val[13]
1	AU.PC	/ld_lfsr_val[13]
0	AU.PC	/ld_lfsr_val[12]
1	AU.PC	/ld_lfsr_val[12]
0	AU.PC	/ld_lfsr_val[11]
1	AU.PC	/ld_lfsr_val[11]
0	AU.PC	/ld_lfsr_val[10]
1	AU.PC	/ld_lfsr_val[10]
0	AU.PC	/ld_lfsr_val[9]
1	AU.PC	/ld_lfsr_val[9]
0	AU.PC	/ld_lfsr_val[8]
1	AU.PC	/ld_lfsr_val[8]
0	AU.PC	/ld_lfsr_val[7]

Figure 8. Fault list for design 1

3.2. Design 2

Design name is DFT architecture for Wallace tree multiplier. Top level module named as dft_wallace_arch_top which is shown in the Figure 9 it has four inputs named as clk, ld_lfsr, ld_lfsr_values and rstn .it has four outputs as Fail, Pass, r_out and q0 which is of 16 bit. This top schematic view is obtained after doing RTL simulation of the design 1 using Questasim tool.

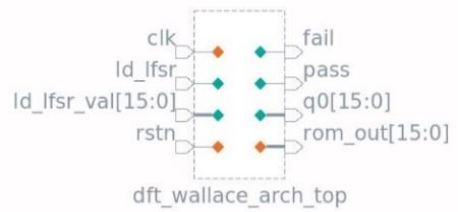

Figure 9. dft_wallace_arch_top Schematic

3.2.1. Description for design 2

Description of design 2 is obtained by performing Scan insertion on design 1 using tcl scripting by adding scan logic to each and every node of the design by adding 5 scan chains by converting normal flip flops into scannable flipflops using DFT libraries in tessent tool. No violations found in this design it passes all scan checks nd proves as efficient design.

- Potential number of no-scan flops to be converted to scan cells is 16
- Number of targeted sequential library cells is 26
- Analysis on ATPG
- Reading group test procedure file.dft_arch_top. testproc
- Simulation of load and unload procedure completed after scan insertion
- 26 scan cells are identified in 5 scan chains
- Longest scan chain has 6 scan cells

3.2.2. Parallel fault simulation for design 2

In this waveform, no error is found in expected and simulated patterns. When scan enable is low Launch_capture of the data happens, when scan enable is high, loading and shifting of the data happens. Parallel simulation takes less clock cycles, cycle count is 135 and pattern count is 44 which is shown in Figure 10. Fault list for design 2 shows all internal possible faults of stuck at type in design 2 which is shown in Figure 11. Commands to find fault list is instructed in previous section. Formulas to find fault and test coverage as shown in:

- Test coverage = Detectable faults/total number of testable faults
- Faults Coverage = Detectable Faults/total of faults in the design
- Total number of testable faults = Total number of faults − (RE + UU+ BL + TI)

Figure 10. Parallel fault simulation for design 2

type	code	pin_pathname
0	DI.CLK	/clk
1	DI.CLK	/clk
0	DS	/rstn
1	DS	/rstn
0	DS	/ld_lfsr
1	DS	/ld_lfsr
0	DS	/LFSR_inst/U13/A0
0	EQ	/LFSR_inst/U13/A1
0	EQ	/ld_lfsr_val[15]
1	DS	/ld_lfsr_val[15]
1	EQ	/LFSR_inst/U13/A0
1	DS	/LFSR_inst/U17/B0
1	EQ	/LFSR_inst/U17/B1
1	EQ	/LFSR_inst/U27/Y
0	EQ	/LFSR_inst/U27/A
0	EQ	/ld_lfsr_val[14]
0	DS	/LFSR_inst/U27/Y
1	EQ	/LFSR_inst/U27/A
1	EQ	/ld_lfsr_val[14]
0	EQ	/LFSR_inst/U17/B0
0	DS	/LFSR_inst/U19/B0
0	EQ	/LFSR_inst/U19/B1
0	EQ	/ld_lfsr_val[13]
1	DS	/ld_lfsr_val[13]
1	EQ	/LFSR_inst/U19/B0
0	DS	/LFSR_inst/U20/B0
0	EQ	/LFSR_inst/U20/B1
0	EQ	/ld_lfsr_val[12]

Figure 11. Fault list for design 2

3.3. Comparison and Justification of the results

From experimental results on design 1 and design 2, we were able to tabulate simulated patterns, test patterns, total faults, test coverage and fault coverage for the proposed two designs in Table 1. From comparison Table 2 the proposed method is able to increase fault coverage by 27% and test coverage by 9% using structural testing through scan insertion and deterministic ATPG which is compared to references [18], [21]. Hence justified efficient fault simulation is done from fault list written for DFT inserted designs.

Table 1. Experimental results on design 1 and design 2

Sl. No.	Design	Simulated patterns	Test patterns	Total faults	Test coverage	Fault coverage
1	DFT architecture for 16-bit shift register	74	47	4108	90.23%	79.60%
2	DFT architecture for Wallace tree multiplier	83	45	4278	99.26%	97.78%

Table 2. Comparison table of the proposed method with existing methods

Sl.No.	Parameters	Functional Testing for stuck at type fault [21]	ECO method for stuck at type fault [18]	Structured testing for stuck at type fault [Proposed]
1	Fault coverage	70%	-	97.78%
2	Test Coverage	-	90.07%	99.26%

4. CONCLUSION

In this paper, the controllability and observability of the clocks set and reset is achieved by scan insertion for area and power efficient RTL designs using 14 nm technology using Tessent scan tool. Elimination of S1 and D5 Violatiotions are achieved using test insertion. Better usage of tessent and synopsis tool are done. Different classes of faults are found. Better fault and test coverage is obtained using deterministic ATPG followed by Serial and Parallel fault simulation from the fault list obtained with suitable pattern count and cycle count. In Future better compression techniques can be used to enhance testability features and to reduce scan chains.

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