

Analysis of Dither in Electro-Hydraulic Proportional Control

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Abstract

Pulse with modulation (PWM) is widely used in proportional control systems for it is efficient, flexible and anti-interference. Due to the friction and hysteresis of electromagnet, hysteresis exists when hydraulic valve in steady-state, and hysteresis influences the dynamic characteristics of the valve seriously, the hysteresis can be improved by superimposing dithers with certain frequency and amplitude to the valve coil. Aiming at the character of anti-unloading power driver circuit, this paper analyzed the parasitic dither which exists in $\pm 24V$ PWM control, besides, the experiment shows that in a high frequency PWM, dither with independent frequency and amplitude can be generated by changing the frequency of the PWM, in this way, the dithers and average current of coil can be adjusted separately by changing PWM frequency and PWM duty cycle.

Keywords: PWM, anti-unloading, dither, hysteresis

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1. Introduction

Hydraulic proportional valves are currently used in a wide range of applications involving high precision proportional control systems [1-4]. And PWM technique has become the standard for electro-hydraulic proportional valve amplifiers for it is efficient, flexible and anti-interference [6-8]. And it is applied to the servo valve by Murtaugh for the first time in 1959 [5].

Chinese scholars such as WenBin Gong, Yutian Zhu have theoretically analyzed the parasitic dither which exist in 0 - +24V PWM drive signal [7, 9]. Aiming at the character of anti-unloading power driver circuit [10], this paper analyzed the parasitic dither which exist in $\pm 24V$ PWM drive signal both theoretically and experimentally. Besides, we have generated independent dither by changing the frequency of PWM.

2. Design of Drive Circuit

The Anti-unloading power driver circuit is shown in Figure 1. It is principle diagram of driver module of the controller developed in this study.

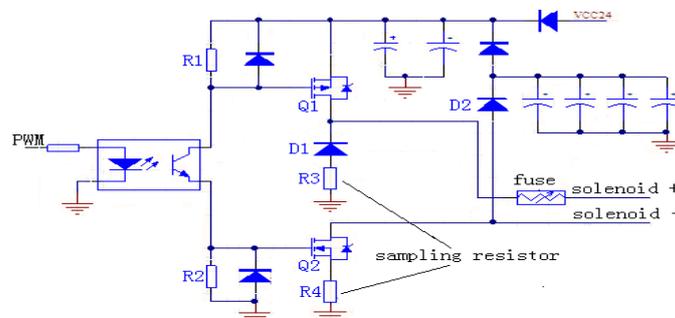


Figure 1. Anti-unloading Power Driver Circuit

When the PWM signal is high level, the field effect transistors(Q1 and Q2) open at the same time, then the direction of the current is $+24V \rightarrow Q1 \rightarrow \text{electromagnet} \rightarrow Q2 \rightarrow R4 \rightarrow \text{GND}$, at this time, the voltage of electromagnet is $+24V$. When the PWM signal is low level, the two field effect transistors close at the same time, due to the inductor performance of electromagnet, the direction of faradic current is $\text{GND} \rightarrow R3 \rightarrow D1 \rightarrow \text{electromagnet} \rightarrow D2 \rightarrow +24V$, and the voltage of electromagnet is $-24V$, in this case, the speed of discharge of the electromagnet is largely improved, so does the system flexibility. Meanwhile, the voltage of electromagnet is $\pm 24V$ and this is the working principle of anti-unloading power driver circuit.

3. Theoretical Analysis of Parasitic Current

The current of electromagnet showed an increasing tendency when the PWM signal is high level, and was downtrend when the PWM signal is low level, which caused the cyclical fluctuation of the current, and this is so called parasitic current or parasitic dither [3]. The simulation waveform of parasitic current is shown in Figure 2.

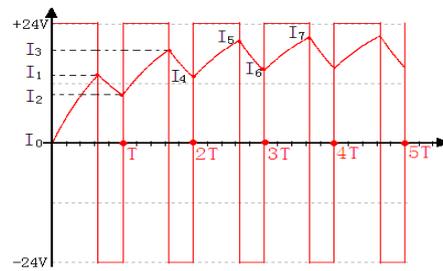


Figure 2. Simulation Waveform of Parasitic Current

The electromagnet is equivalent to a RL circuit. R is the DC resistance of the coil, and L is the inductance of the coil. The i is the current of coil, and U is the voltage of the coil, On the basis of Kirchoffs voltage law, the voltage equations is [11]:

$$Ri + L \frac{di}{dt} = U$$

The change law of the current can be expressed as:

$$i = \frac{U}{R} (1 - \exp(-\frac{t}{\tau}))$$

In which time constant $\tau = L / R$ (s), as is shown in Figure 2, the initial electric current is I_0 , PWM period is T , duty cycle is $D(0 \leq D \leq 1)$, so, at the rising edge of PWM:

$$I_1 = I_0 \cdot \exp(-\frac{DT}{\tau}) + \frac{U}{R} \left[1 - \exp(-\frac{DT}{\tau}) \right]$$

At the fall edge:

$$I_2 = I_1 \cdot \exp(-\frac{(1-D)T}{\tau}) - \frac{U}{R} \left[1 - \exp(-\frac{(1-D)T}{\tau}) \right]$$

Simultaneously:

$$I_3 = I_2 \cdot \exp(-\frac{DT}{\tau}) + \frac{U}{R} \left[1 - \exp(-\frac{DT}{\tau}) \right]$$

$$I_4 = I_3 \cdot \exp\left(-\frac{(1-D)T}{\tau}\right) - \frac{U}{R} \left[1 - \exp\left(-\frac{(1-D)T}{\tau}\right)\right]$$

$$I_5 = I_4 \cdot \exp\left(-\frac{DT}{\tau}\right) + \frac{U}{R} \left[1 - \exp\left(-\frac{DT}{\tau}\right)\right]$$

$$I_6 = I_5 \cdot \exp\left(-\frac{(1-D)T}{\tau}\right) - \frac{U}{R} \left[1 - \exp\left(-\frac{(1-D)T}{\tau}\right)\right]$$

Let $A = \exp\left(-\frac{DT}{\tau}\right)$, $B = \exp\left(-\frac{(1-D)T}{\tau}\right)$, $I_0 = 0$, the peak of the stable value of the current is:

$$\begin{aligned} I_{\max} &= I_1(1 + AB + A^2B^2 + A^3B^3 + \dots) \\ &\quad - \frac{U}{R}(1-B) \cdot A \cdot (1 + AB + A^2B^2 + A^3B^3 + \dots) \\ &\approx \frac{U(1-2A+AB)}{R(1-AB)} \end{aligned}$$

The value of wave trough is:

$$\begin{aligned} I_{\min} &= I_1B \cdot (1 + AB + A^2B^2 + A^3B^3 + \dots) \\ &\quad - \frac{U}{R}(1-B)(1 + AB + A^2B^2 + A^3B^3 + \dots) \\ &\approx \frac{U(2B-AB-1)}{R(1-AB)} \end{aligned}$$

Therefore, the the amplitudes of the parasitic current is:

$$I_{\max} - I_{\min} = \frac{2U}{R} \cdot \frac{1-A-B+AB}{1-AB} \quad (1)$$

The average value of the parasitic current is:

$$\frac{I_{\max} + I_{\min}}{2} = \frac{U}{R} \cdot \frac{B-A}{1-AB} \quad (2)$$

We can get the relationship between the amplitudes of parasitic current and PWM (Duty cycle and frequency) from formula (1), the relationship is shown in Figure 3.

Figure 3 shows that the amplitudes of parasitic current were affected both by duty cycle and frequency of PWM. At the same duty cycle, the higher the frequency of PWM, the smaller the amplitudes of parasitic current; At the same frequency, the amplitudes of parasitic current is the maximum when the PWM duty cycle is 50%. Besides, the frequency of PWM is same as the frequency of parasitic current.

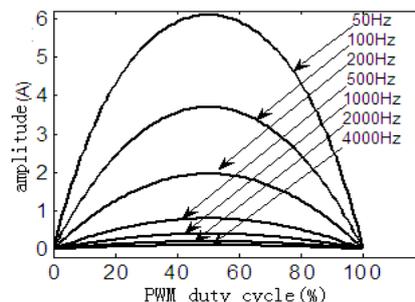


Figure 3. The Relationship between Amplitude and PWM

4. Experimental Study of Parasitic Current

This article focuses on some type proportional flow valve of Rexroth, of which the DC resistance is 6Ω , Inductance Value is 30mH. In the experiment, the frequency of PWM were 4KHz, 500Hz and 200Hz separately, and PWM duty cycle is fixed value.

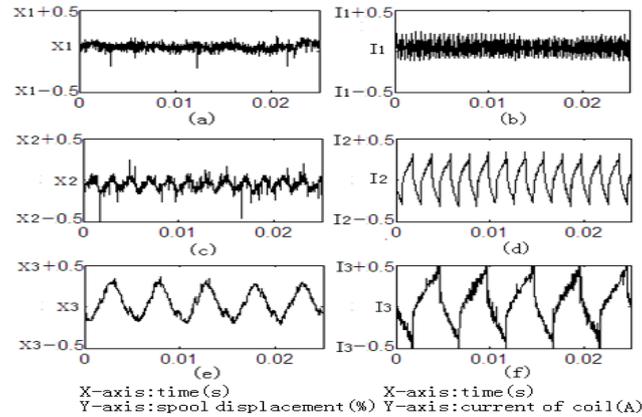


Figure 4. Valve Core Flutter and Parasitic Current

Figure 4(a) shows the flutter of valve core when the frequency of PWM is 4KHz, Figure 4(c) and Figure 4(e) correspond to 500Hz and 200Hz separately. Figure 4(b), Figure 4(d) and Figure 4(f) are the parasitic current of the coil when the frequency are 4KHz, 500Hz and 200Hz separately. In order to compare, the Coordinates were all calibrated, in which x_1 , x_2 and x_3 refer to spool displacement, and I_1 , I_2 and I_3 refer to the current of coil.

The experiment showed that when at the same duty cycle, the lower the frequency of PWM, the bigger the the amplitudes of parasitic current, and the frequency of PWM is same as the frequency of parasitic current. And the conclusion is same as the theoretical analysis. When the PWM frequency is 4KHz, the frequency of parasitic current is also 4KHz which is much higher than the response frequency of valve, so the valve core is almost stationary. When the PWM frequency is 200Hz, there is noticeable vibration on the valve core, the amplitude is about 0.6%.

Let valve core in vibration state, then static friction will be replaced by sliding friction, which is an effective means to decrease the hysteresis. In order to study the effect on hysteresis made by parasitic current, we made comparative test between 4KHz and 200Hz.

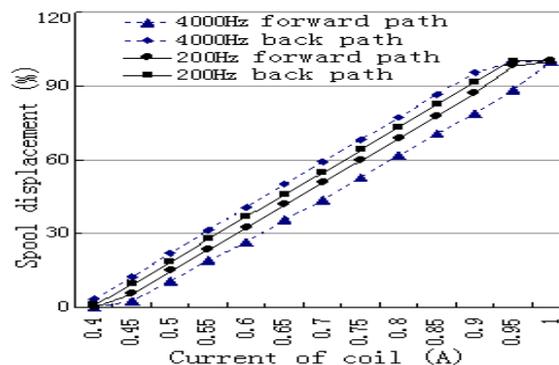


Figure 5. The Effect on Hysteresis Made by Parasitic Current

Figure 5 shows the the effect on hysteresis made by parasitic current. Generally, when the frequency of parasitic current is lower than 200Hz, it is effective to decrease the friction hysteresis, and when the frequency is lower than 2KHz, it is effective to decrease the

magnetic hysteresis [12]. After analysis, the hysteresis is about 12.03% when the PWM frequency is 4KHz, and 3.51% when the frequency is 200Hz. The experiment showed that suitable parasitic current has remarkable effect on decreasing the hysteresis.

5. Several Influencing Factors of Parasitic Dither

When in a low PWM frequency, parasitic dither (or say parasitic current) is a decisive factor of flutter of valve core. However, once the parameters of electromagnet and PWM frequency were determined, the amplitudes and frequency of parasitic dither were defined, furthermore, the amplitudes and frequency of parasitic dither can not be adjusted independently, all these are the great limitations to apply it to practical engineering.

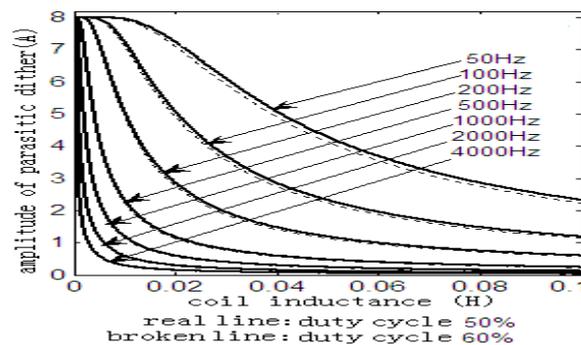


Figure 6. The Effecton on Hysteresis Made by Parasitic Current

Figure 6 showed the effections on the amplitude of parasitic dither made by PWM frequency, duty cycle and coil inductance (DC resistance is 6Ω). From theoretical point of view, matching parameters such as PWM frequency and coil inductance reasonably, suitable parasitic dither can be generated.

In this paper, the maximum current of the valve is about 1.5A, and the range of PWM duty ratio is from 54% to 70%, from Figure 6 we can see that the effecton on parasitic dither made by PWM duty ratio is almost negligible when the PWM duty ratio changing in a narrow range, so, the parasitic dither signal is stable.

6. The Principle of Superimposing Dithers by Frequency Moderation

Figure 7 shows the relationship between the average value of parasitic current and PWM. On the one hand, we can conclude that when at the same PWM frequency, the average value of parasitic current increases as the PWM duty increases, so, at present, the pulse width modulation method is widely used to superimpose dithers. On the other hand, when at the same PWM duty cycle, the higher the PWM frequency, the higher the average value of parasitic current.

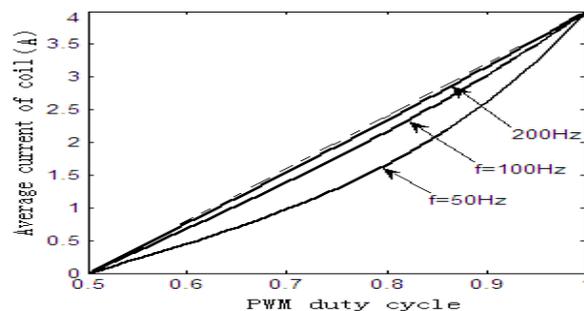


Figure 7. The Relationship between PWM Duty and Current of Coil

Actually, the change law of the current is complex, in this paper, we study the current of coil by experiment method. Figure 7 shows the relationship between the PWM frequency and the current of coil when the PWM duty cycle is 50%, 52%, 55%, 57% and 60% separately.

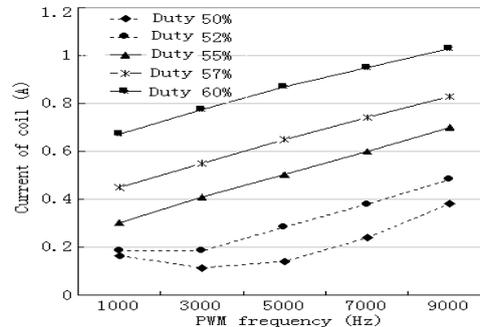


Figure 7. The Relationship between PWM Frequency and Current of Coil

The experiment showed that the current of coil increases as the PWM frequency increases with good linearity when the PWM duty cycle is more than 55%. So, when the PWM frequency waves around a fixed frequency, the current of coil waves too. In this way, the dithers can be superimposed to the valve coil, and the dithers and average current of coil can be adjusted separately by changing PWM frequency and PWM duty cycle, besides, the algorithm of superimposing dithers is simplified.

7. Experimental Verification

In order to observe obvious experimental phenomena, the central frequency is set to 6KHz in the programm, the amplitude is set to 4KHz, and PWM duty cycle is set to 57%. Besides there is an interrupt, which is triggered every time when a PWM period finished. In the interrupt service routine, the PWM frequency is increased or decreased on the base of the current frequency to make the PWM frequency change according to triangle-wave, in this way, the current of the coil will also change according to triangle-wave, as Figure 8 shows.

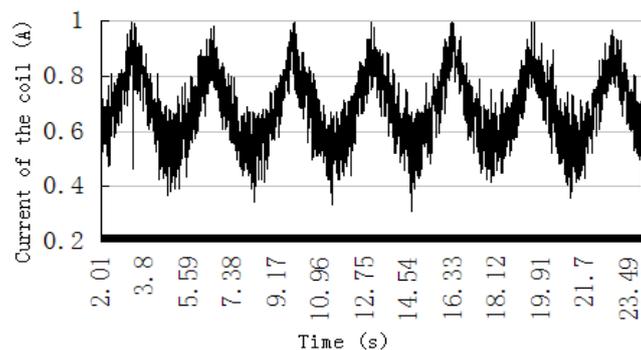


Figure 8. The Current of Coil

8. The Results of Superimposing Dithers by Frequency Moderation

Based on the practical object, the central frequency is set to 3 KHz in the program, the amplitude is set to 2 KHz, and PWM duty cycle changes between 54%-70%.

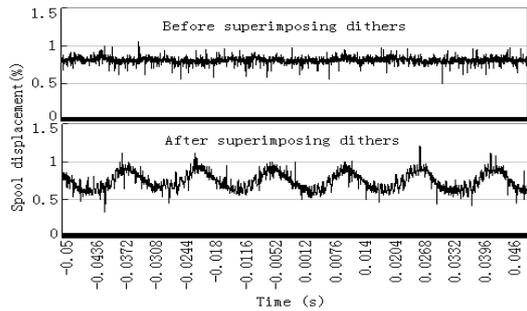


Figure 9. The Spool Displacement Pre-and Post Superimposing Dithers

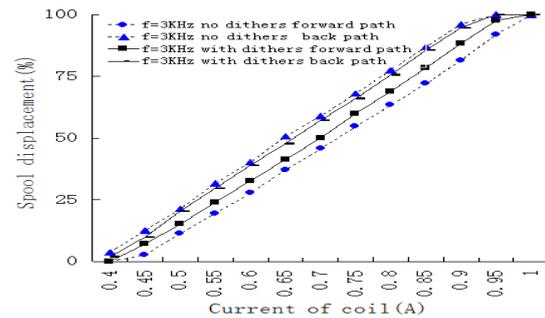


Figure 10. The Effects on Hysteresis Made by Dithers

Figure 9 shows that the spool displacement pre-and post superimposing dithers, there is obvious vibration on the valve core of which the frequency is 70Hz and the amplitude is about 0.4%.

Figure 10 shows the effects on hysteresis made by dithers, the broken line refer to the forward and back path without dithers, and the real line refer to the forward and back path with dithers, after analysis, the hysteresis is 12% before superimposing dithers and 4.97% after superimposing dithers.

9. Conclusion

(1) Aiming at the character of anti-unloading power driver circuit, this paper analyzed the parasitic dither which exists in $\pm 24V$ PWM control, and the algorithms for the dither is deduced.

(2) This paper studied the effects on parasitic dither and hysteresis made by PWM with different frequency, and several factors effecting parasitic dither were analyzed.

(3) In the experiments, we superimposed dithers to the valve coil successfully by frequency moderation, and in this way, the hysteresis is improved significantly.

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