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D flip-flop design by adiabatic technique for low power applications

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ABSTRACT

Indigital circuits, energy reduction is the most important parameter in the design of handy and battery-operated devices. Flip- flop is an important component in any digital system. By improving the performance of flip-flop, complete system performance is better. This paper addresses the design of D flip-flop using direct current diode-based positive feedback adiabatic logic (DC-DB PFAL) at various frequencies at 45nm technology node. Further, the layout for the proposed design is also presented. The performance analysis is carried out for delay, power dissipation, power delay product and transistor count. Circuit simulation is done by using cadence virtuoso tool at 10 MHz and 100 MHz frequencies. The results show an improvement in power dissipation of 18% with less transistors count compared to exiting designs in the literature.

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1. INTRODUCTION

As battery-powered devices become smaller, the size of the devices also shrinks. Low-power very large scale integration design has been progressively increasing due to speedy and inventive development [1]. Because of the rapid advancement of personal devices, high-performance digital signal processors and the internet of things, low power, fault tolerance, and high-performance devices are in greater demand [2], [3]. Alam *et al*. [4] have presented the low-power, small, and modular complementary metal -oxide semiconductor amplifier for modern radio frequency receivers, showing the improvement in power dissipation and gain range. Sulaiman [5] have presented multi-objective Pareto front and particle swarm optimization techniques to minimize energy consumption and delay in microprocessors.

The adiabatic technique is one of the innovative approaches for minimum power dissipation at the circuit logic level if the time constraint is not critical. The most optimum approach is adiabatic-logic, which stores energy in the capacitor rather than discharging it to the ground. Adiabatic is a thermodynamic term that describes a procedure in which energy is not shared with the environment, hence, there is no energy dissipation [6]. Chaudhary *et al.* [7] presented a low-power memory cell using the adiabatic technique. Sharma and Noor [8] designed a semi-adiabatic positive feedback adiabatic logic (PFAL) based dual-rail D flip-flop. A positive-edge flip-flop is implemented in a master-slave configuration. The primary inverter/buffer setup is utilized to regulate the operation of the D flip-flop after adding additional transistors. Sharma and Noor [9] implemented asynchronous reset capability in a complementary pass transistor logic based adiabatic gated (CPLAG) XOR gate. It may be made synchronous with the count of an extra transistor and the reference clock

signal. Ghatole and Gaikwad [10] designed a low-power flip-flop with an innovative resettable method based on signal feed-through adiabatic buffers. It has a variety of pulse-triggered flip-flop devices. The problem of a long discharge path is solved, and improved power and speed are obtained. Hu *et al.* [11] designed and implemented complementary pass-transistor logic in low-power adiabatic sequential circuits. Sharma and Noor [9] developed a different type of flip flop using the conventional technique and the efficient charge recovery logic adiabatic logic technique. Bhutada [12] designed a low-voltage flip-flop circuit and the power-gating using the complementary pass-transistor adiabatic logic (CPAL) approach. Kiran and Raju [13] have presented the realization of energy-efficient combinational and sequential circuits using different adiabatic techniques. Dhoble and Kale [14] presented the design of a positive edge triggered D flip-flop and it is increase the counter's speed in a phase-locked loop using VLSI technology. It consumes low power and provides high speed. Lin *et al.* [15] presented a low-voltage adiabatic flip-flop which is designed using the CPAL power-gating with DTCMOS (dual threshold complementary metal–oxide–semiconductor) approach. Sharma and Noor [16] designed modified PFAL adiabatic logic circuits with a reconfigurable CPLAG approach. Xin *et al.* [17] designed a 2-phase adiabatic CPAL flip-flop circuit and optimized the power dissipation promptly. Sundar [18] have presented an adiabatic logic method to demonstrate an ultra-low-power sequential logic circuit. Garg and Niranjan [19] presented the logic circuits designs like inverter, NAND, NOR, half adder, and positive edge triggered Dflip-flop using a new cascade adiabatic logic technique. Bharathi *et al.* [20] presented energy- efficient D flip-flop, half adder, and full adder circuit designs and implemented them using sub-threshold adiabatic logic with two-phase clocking.

Now days, many researches has been reported on the design of adders [20]-[24], subtractors [25], comparators [26]-[28], memory [29] and some other combinational and sequential circuits. The schematic and layout design of the presented circuit is unreported in the literature as of yet. This paper presents a design of a D flip-flop based on the DC-DB PFAL adiabatic approach. The proposed design layout is also drawn and discussed for the process feasibility.

The remaining part of this paper is structured as follows. The preliminaries are discussed in section 2. The design and implementation along with layout of D flip-flop are depicted in section 3. The results and discussion are included in section 4. Finally, this paper is concluded in section 5.

2. PRELIMINARIES

An adiabatic circuit is a part of low-power technology that employs reversible logic to save energy [30]. The term adiabatic is refers to thermodynamic process in which no energy is exchanged with the environment and hence no energy is lost in the form of energy consumption [31]. For energy usage in the adiabatic circuit, there are three rules [32], [33]:

i) If the drain and source terminals have a considerable voltage difference, the transistor must be turned off.
ii) While current flows over the transistor, it must be switch on.
iii) Never let current flow over a diode.

In place of a steady power source, an adiabatic logic uses the trapezoidal power clock. A 4-stage power supply clock is used in adiabatic logic, that contains ideal, evaluate, hold, and recover phases. In evaluation phase, supply voltage is increased from 0 V to Vdd, i.e. Supply voltage is going up. In hold phase, supply voltage is constant to Vdd and retaining the values for outputs. In recovery phase, energy is recovered, the supply voltage is decreasing from Vdd to 0 V and the power supply recovers the accumulated charge from the capacitors. In wait phase, supply voltage is 0 V.

3. DESIGN AND IMPLEMENTATION

In this section, the DC-DB PFAL adiabatic technique is used to design the proposed D flip-flop using cadence virtuoso tool at 45 nm node and at different frequencies of 10 MHz and 100 MHz. DC- DB PFAL adiabatic approach is the modified in modified positive feedback adiabatic logic (MPFAL) logic circuit. The proposed design provides nearly complete charge recovery, which has been previously impossible. Proposed design is implemented and analyzed in terms of latency, power dissipation and power delay product and results are compared with the existing adiabatic techniques and conventional technique.

3.1. DC-DB PFAL based D flip-flop

DC-DB PFAL D flip-flop circuit is depicted in Figure 1. MPFAL logic has been modified in this circuit. The proposed design provides nearly complete charge recovery, which has been previously impossible. High impedance path to the power clock is provided by the diode attached at the bottom of N-type metal-oxide-semiconductor (NMOS) tree and it acts as an active load. By reducing the rate of discharge of internal nodes of the logic circuit and it can controls the discharging path. The positive source of direct current voltage is

connected between the diode and the ground to further incorporate the advantage of level shifting technique in the proposed logic circuit. Level shifting technique reduces the gate to source voltage at the output transistors and thus reduces the leakage and gate current, in turn reduces the energy consumption. It is more effective than the other adiabatic logic techniques used earlier for reduction in power dissipation. Simulations are carried out at 10 MHz and 100 MHz frequencies, at 45 nm technology node and the results are obtained for power dissipations and delay. A comparative analysis for performance parameters is shown in Table 1.

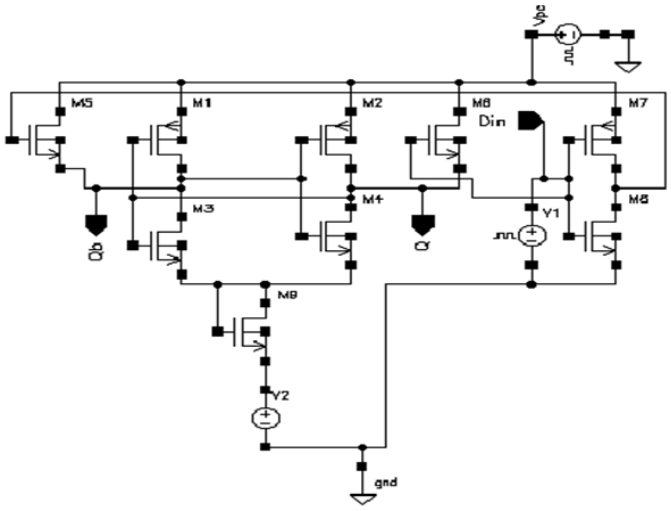

Figure 1. D flip-flop based on DC-DB PFAL

3.2. Layout design of proposed D flip-flop

Apart from schematic design, layout design is the most critical step in very large scale integration (VLSI) design flow. Here, the layout design of proposed D flip has been presented. The layout shown here is simulated on the virtuoso tool at 45 nm technology node with design rule check (DRC) and layout versus schematic (LVS) check. It is noteworthy to mention here that this is the first attempt to present the schematic and layout design of D flip-flop utilizing DC-DB PFAL adiabatic technique and thus, can give significant contribution in the low power VLSI domain. Figure 2 depicts the present circuit layout design.

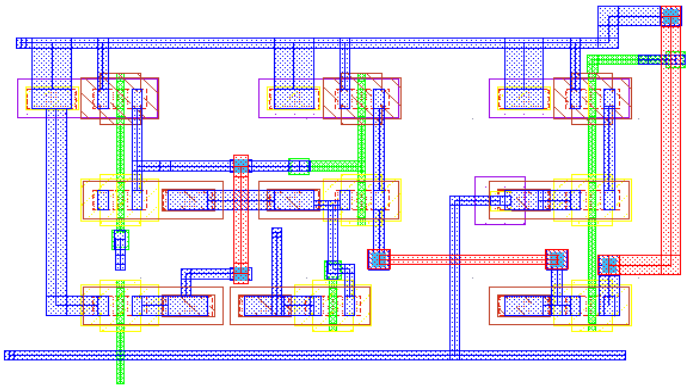

Figure 2. Proposed D flip-flop layout design

4. RESULTS AND DISCUSSION

This article presents the design of D flip- flop using DC-DB PFAL adiabatic approach. The diode at the bottom of the PFAL latch allows for easy control of the discharge path by lowering the discharge rate of the circuit's internal nodes, as well as level shifting. The leakage current of the output transistor and the gate to source voltage are reduced, because of the level shifting. The proposed circuit minimizes the power consumption.

For analysis, the cadence virtuoso tool is used to simulate the present circuit at 45 nm technology node. The D flip-flop circuit parameters like delay, energy consumption, transistor count, and power delay product are investigated. The power dissipation in D flip-flop is one of the most important metrics. When compared to the other existing adiabatic approaches and conventional technique, the energy consumption in proposed design using DC-DB PFAL is the smallest at 10MHz. A Comparative analysis of present circuit design with the existing designs at various frequencies is carried out in Table 1. In this table, at some places the '-' is marked, where the data is not available in the literature. The simulation waveform is depicted in Figure 3. Finally, in Figure 4, the graphs have been plotted, showing the comparison of transistors count for the existing designs with the present design.

The proposed circuit is simulated using 1 V trapezoidal power supply. In Figure 3, the output waveform of the present circuit is represented. In which the output (Q) waveform is obtained corresponding to input (D) and power clock (Vpc) combinations. It is found from the simulation waveform that the output swing is equal to the input swing. In other words, the, output logic level in proposed D flip-flop is nearly the same as that of input logic levels i.e, 0V for logic '0' and 1 V for logic '1'.

The power dissipation of the present circuit design is compared with the existing designs at different frequencies. It is found that the proposed circuit shows improvement in power dissipation by 33% and 18% respectively as compared to RCPLAG based D flip-flop circuit [16] and Sub-threshold adiabatic logic based D flip-flop [20]. In CMOS circuits chip density is the another parameter and it is calculated by the number of transistors. The transistor count of the presented design compared to the other existing techniques is illustrated in Figure 4, wherein 'P' instance for proposed design. It is observed that the present circuit uses fewer transistors compared to the standard adiabatic approaches. Moreover, latency is one of the important performance parameter when it comes to speed. In comparison to the certain designs, it shows improved performance in terms of latency as shown in Table 1.

Table 1. Comparative analysis of the existing designs with proposed D flip-flop

SI.No.	D flip-flop references	Delay (ps)	Power dissipation (mW)	Transistor count	Frequency (MHz)
1	CMOS [13]	72	0.798	18	-
2	CMOS [20]	-	0.0582	-	-
3	ECRL [13]	15	15.08	18	-
4	ECRL [16]	-	0.0591	-	-
5	PFAL [13]	15	4.83	18	-
6	PFAL [16]	-	0.0747	-	-
7	2PASCL [13]	17	17.98	20	-
8	Master-slave [7]	-	13.4	-	-
9	Sub-threshold adiabatic logic [20]	-	0.032	-	-
10	Reconfigurable complementary pass transistor adiabatic logic gated [16]	-	0.039	-	-
11	CMOS [19]	-	0.141	-	-
12	Adiabatic logic [19]	-	0.084	-	-
13	Two-phase CPAL [11]	-	-	20	100
14	Proposed adiabatic logic-2N/2N-2N2P [11]	-	-	24	100
15	CMOS TG [11]	-	-	16	100
16	Proposed design (100 MHz)	50.01	0.419	9	100
17	Proposed design (10 MHz)	30.0	0.026	9	10

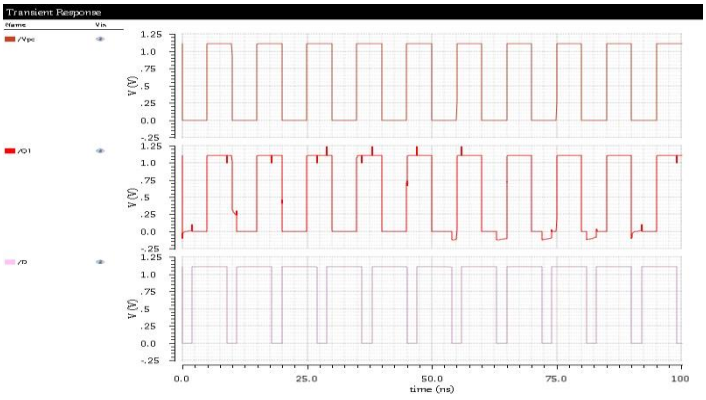

Figure 3. Output waveforms of the proposed circuit

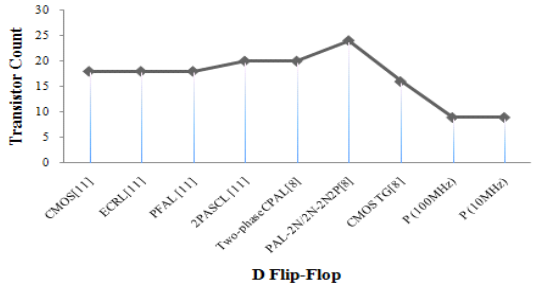

Figure 4. Transistor count of proposed design with existing designs

5. CONCLUSION

This paper presents the design of D flip-flop using DC-DB PFAL adiabatic technique. Proposed circuit is implemented on virtuoso tool at 45 nm technology node. Comprehensive analysis is carried out for the performance parameters like transistor count, power delay product, delay and energy consumption. The results are compared to the earlier existing designs with the present design. It is observed that the presented circuit design outperforms over the existing designs. Moreover, the layout design for the proposed DC-DB PFAL technique is also presented with DRC and LVS check to prove compatibility in the chip design. The proposed circuit consumes 26 µW power, which results in power reduction by 18% and transistors count by 43% compared to the available designs. The present circuit shows superior performance in terms of area and power dissipation at the cost of delay. The comprehensive investigation shows that the presented design can contribute significantly towards low power VLSI applications

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