Positive-sequence virtual-flux control of grid-connected converter during unsymmetrical voltage dips

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ABSTRACT

One of the major problems in direct power-controlled grid-connected voltage source converters is that during voltage dips, the converter current increases to compensate for the reduced grid voltage. The most common voltage dips are unsymmetrical, and they cause unbalance and distortion in the converter current. This paper introduces a new, simple but effective algorithm which limits the current in a direct power-controlled grid-connected voltage source converter during voltage dips. A positive-sequence virtual-flux based control scheme is employed and this makes the current balanced and sinusoidal during unsymmetrical voltage dips. The proposed control clearly demonstrates the performance which is illustrated through various simulations and experimental work. The current during unsymmetrical voltage dips is limited in magnitude and is balanced, with low distortion. The Implementation of this control scheme will enable voltage source converters to stay connected to the grid during voltage dips as required by most grid codes.

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1. INTRODUCTION

The grid-connected voltage source converter (VSC) has become widely used, mainly due to the increased use of distributed generation based on renewable energy; of which the most dominant are wind and solar photovoltaic (PV) systems. Grid-connected VSCs are also used as active filters, active front-end rectifiers, static synchronous compensators and VSC based high-voltage DC (HVDC) transmission systems. In all its applications, the grid-connected VSC is exposed to disturbances that may occur in the grid, such as voltage dips. Voltage dips are mainly caused by faults which could be symmetrical or unsymmetrical [1]-[3].

Due to changes in grid codes for many countries, made necessary by the increasing size and number of DG installations, VSCs for renewable energy DGs such as PV are required to remain connected to the grid during faults and provide grid support to maintain power system stability [4]. Therefore, the control system for the VSC should be designed to be able to control the VSC no only during stable operation, but also during faults and abnormal operating conditions [5].

The major problem with direct power controlled VSCs which is discussed in this paper is that during voltage dips, the current tends to increase to compensate for the reduction in voltage. The other problem is that during unsymmetrical faults, the presence of the negative-sequence components in the grid voltage and current leads to oscillations at twice the grid frequency in the active power, reactive power and DC link voltage [6], [7]. Therefore, one of the requirements for control of the VSC during faults is limiting the current

to a safe level to avoid tripping or possible damage to the semiconductor devices of the VSC. Another requirement is that during unsymmetrical faults, in addition to limiting the current, the VSC should be controlled to achieve balanced grid currents, which will reduce oscillations in the active power, reactive power and direct current (DC) link voltage.

A number of current limiting strategies have been proposed in literature such as [8]. Three different control schemes to achieve unit power factor, constant active power, or limited current, respectively, during unbalanced voltage dips are proposed in [9]. However, these strategies are implemented in the natural reference frame with Pi current controllers, making the control more complicated due to having to tune three different controllers, and the use of PI controllers to control sinusoidal currents leads to a steady state error [10]. Current limiting in the synchronous reference frame for a VSC HVDC scheme is presented in [11]. The proposed scheme limits the current during both symmetrical and unsymmetrical voltage dips. However, the current limiting depends on an outer loop frequency controller, which is not always available for grid-connected VSCs. In Reese *et al.* [12], a current limiting algorithm based on the German grid codes is applied to a direct power-controlled grid-connected VSC. The current limit is achieved by imposing the current limits defined by the German grid code, and then recalculating the active power and reactive power references based on the limited current. This requires transformation of the currents from the stationary reference frame to the synchronous reference frame (SRF), which is normally avoided in direct power control schemes, due to the increased computational burden on the controller.

During unbalanced voltage dips, the presence of negative-sequence components gives rise to oscillations in the active power and reactive power, and in the grid voltage angle detected by the phase-locked loop. Conventional current control schemes such as voltage-oriented control and direct power control would not be able to adequately control the current during unsymmetrical faults. A voltage oriented current control scheme suitable to control the VSC during unsymmetrical faults is the decoupled-double synchronous reference frame (DD-SRF) proposed in [13]. It consists of two synchronous reference frame current controllers, one rotating in the positive direction and one rotating in the negative direction. The main drawback of the DD-SRF controller is that it has four PI controllers and needs two separate synchronization angles, one for the positive-sequence and one for the negative-sequence in its implementation.

A number of control schemes based on proportional-resonant (PR) controllers such as the ones in [14], [15] have been proposed to give balanced phase currents, reduce oscillations in the active power, the reactive power or both during unsymmetrical faults. These are: instantaneous active-reactive control (IARC), average active-reactive control (AARC), positive-negative-sequence compensation (PNSC) and balanced positive-sequence control (BPSC). IARC gives constant active and reactive power, but the currents are highly distorted and unbalanced. AARC gives constant active power, while the reactive power has oscillations at twice the fundamental frequency and the currents are sinusoidal but unbalanced. PNSC gives constant reactive power, while the active power has oscillations at twice the fundamental frequency and sinusoidal but unbalanced currents. BPSC gives reduced oscillations in both active power and reactive power, while the currents are balanced and sinusoidal. In all these schemes, the current reference is calculated using the power and the voltage to meet a specific objective.

In this paper, a new current limiting algorithm for a grid-connected VSC is proposed. The VSC is controlled using direct power control with space vector modulation (DPC-SVM). Power estimation and synchronization is accomplished using the grid virtual-flux and the inverter current in the stationary reference frame. The VSC is connected to the grid through an LCL filter. Due to the current sensors being on the inverter side, the system is stable without using passive or active damping of the LCL filter resonance [16]. The error in the estimated reactive power resulting from the use of the inverter current is estimated and subtracted from the reactive power reference to achieve unit power factor operation [17].

The main contribution of the paper is the current limiting algorithm which limits the VSC current during symmetrical and unsymmetrical voltage dips to a safe level. The proposed current limiting algorithm is based on the limiting of the active and reactive power references, without recalculation of the currents, making it simple and easy to implement. To achieve balanced and sinusoidal grid currents during unsymmetrical voltage dips, the positive-sequence component of the grid virtual-flux is extracted and used for synchronization and power estimation.

2. SYSTEM DESCRIPTION

2.1. System Overview

The circuit diagram of the three-phase VSC considered in this paper is shown in Figure 1. The system consists of a two-level insulated-gate bipolar transistor (IGBT) voltage source converter connected to the grid through an LCL filter. The voltage is measured at the grid side of the filter while the current is measured at the inverter side to ensure system stability without the need for any active or passive damping [18]. This however, results in an error between the controlled reactive power and the reactive power at the

grid side, due to the reactive power output of the filter capacitor. To compensate for this error, a new simple compensation scheme which is described in more detail in the next sub-section is implemented. This compensation scheme does not use any additional current sensors such as capacitor current sensors [19]. To improve the quality of the output current even when the grid voltage is distorted, the measured grid voltage is used to estimate the grid virtual flux using cascaded low-pass filters as proposed in [18]. The grid virtual flux has a smoother trajectory than the grid voltage and ensures better synchronization and power estimation. The grid synchronization is achieved using a virtual flux phase-locked loop (VF-PLL). The VF-PLL has better performance than the voltage-based phase-locked loop (PLL) when the grid voltage is distorted without reducing its bandwidth which would lead to a reduced dynamic performance [20]. The instantaneous active and reactive powers are estimated using the grid virtual flux and the inverter current. The powers are controlled by PI controllers, and the PI controller outputs are converted to the stationary reference frame using the inverse Park transformation. Space vector modulation is used to obtain the pulse-width modulation (PWM) signals.



Figure 1. Grid-connected voltage source converter with LCL filter

2.2. Instantaneous power equations with unsymmetrical voltages

When the grid voltage is unbalanced due to, for instance, an unsymmetrical fault, the grid voltage vector can be written as the sum of a positive-sequence vector, and a negative-sequence vector as shown by:

$$\underline{v}_g = \underline{v}_g^{\ p} + \underline{v}_g^{\ n} \tag{1}$$

where $\frac{v_g}{v_g}^p$ is the positive-sequence voltage vector and \underline{v}_g^n is the negative-sequence voltage vector.

A similar expression can be written for the current injected to the grid, if it is unbalanced but has no harmonic distortion. This is given by:

$$\underline{i}_{L2} = \underline{i}_{L2}{}^{p} + \underline{i}_{L2}{}^{n} \tag{2}$$

where \underline{i}_{L2} is the grid current vector; \underline{i}_{L2}^{p} and \underline{i}_{L2}^{n} are its positive and negative-sequence component vectors respectively. There is no zero-sequence component because the investigated system is a three-wire system with no neutral conductor.

By applying the instantaneous power theory [21] and expressing the voltages and currents in terms of their orthogonal stationary reference frame components, the instantaneous active power and reactive power are shown to be composed of constant and oscillating components as:

$$p = P_o + P_c \cos(2\omega t) + P_s \sin(2\omega t)$$
(3)

$$q = Q_0 + Q_c \cos(2\omega t) + Q_s \sin(2\omega t) \tag{4}$$

where P_o and Q_o are the average values of the powers; P_c , P_s , Q_c and Q_s are the amplitudes of the oscillating components of the powers. Each of these power components can be expressed in terms of the voltage and currents components as [22].

$$P_{o} = \frac{3}{2} \left(v_{g\alpha}{}^{p} i_{L2\alpha}{}^{p} + v_{g\beta}{}^{p} i_{L2\beta}{}^{p} + v_{g\alpha}{}^{n} i_{L2\alpha}{}^{n} + v_{g\beta}{}^{n} i_{L2\beta}{}^{n} \right)$$
(5)

$$Q_{o} = \frac{3}{2} \left(v_{g\alpha}{}^{p} i_{L2\beta}{}^{p} - v_{g\beta}{}^{p} i_{L2\alpha}{}^{p} + v_{g\alpha}{}^{n} i_{L2\beta}{}^{n} - v_{g\beta}{}^{n} i_{L2\alpha}{}^{n} \right)$$
(6)

$$P_{c} = \frac{3}{2} \left(v_{g\alpha}^{\ n} i_{L2\alpha}^{\ p} + v_{g\beta}^{\ n} i_{L2\beta}^{\ p} + v_{g\alpha}^{\ p} i_{L2\alpha}^{\ n} + v_{g\beta}^{\ p} i_{L2\beta}^{\ n} \right)$$
(7)

$$Q_{c} = \frac{3}{2} \left(v_{g\alpha}^{\ n} i_{L2\beta}^{\ p} - v_{g\beta}^{\ n} i_{L2\alpha}^{\ p} + v_{g\alpha}^{\ p} i_{L2\beta}^{\ n} - v_{g\beta}^{\ p} i_{L2\alpha}^{\ n} \right)$$
(8)

$$P_{s} = \frac{3}{2} \left(v_{g\alpha}{}^{n} i_{L2\alpha}{}^{p} - v_{g\beta}{}^{n} i_{L2\beta}{}^{p} - v_{g\alpha}{}^{p} i_{L2\alpha}{}^{n} + v_{g\beta}{}^{p} i_{L2\beta}{}^{n} \right)$$
(9)

$$Q_{s} = \frac{3}{2} \left(-v_{g\alpha}{}^{n} i_{L2\beta}{}^{p} - v_{g\beta}{}^{n} i_{L2\alpha}{}^{p} + v_{g\alpha}{}^{p} i_{L2\beta}{}^{n} + v_{g\beta}{}^{p} i_{L2\alpha}{}^{n} \right)$$
(10)

The power controllers in the conventional DPC-SVM scheme are only able to control the average components of the power, while the oscillating components are not controlled. In addition, the synchronization angle will be distorted, due to the non-circular trajectory of the grid voltage vector. As a result, the inverter output current will be unbalanced and distorted.

2.3. Positive-sequence virtual-flux based instantaneous power estimation

To obtain balanced and sinusoidal grid currents, the negative-sequence components of the current have to be forced to zero. This can be achieved by using the positive-sequence voltage or virtual-flux for power estimation and grid synchronization. In this paper the virtual flux is used for power estimation and grid synchronization. Considering only the positive-sequence virtual-flux, the estimated instantaneous powers are given by (11), (12).

$$p = \frac{3}{2} \left(\psi_{g\alpha}{}^{p} i_{L1\beta} - \psi_{g\beta}{}^{p} i_{L1\alpha} \right) \tag{11}$$

$$q = \frac{3}{2} \left(\psi_{g\alpha}{}^{p} i_{L1\alpha} + \psi_{g\beta}{}^{p} i_{L1\beta} \right)$$
(12)

Since, the current is balanced the grid current will not have negative-sequence components. However, the grid voltage is unbalanced and has negative-sequence components. Therefore, the actual power at the grid side will have oscillation arising from the interaction between the balanced current and the unbalanced voltage. The oscillating power components are given by (13)-(16).

$$P_{c} = \frac{3}{2} \left(v_{g\alpha}^{\ n} i_{L2\alpha}^{\ p} + v_{g\beta}^{\ n} i_{L2\beta}^{\ p} \right) \tag{13}$$

$$Q_{c} = \frac{3}{2} \left(v_{g\alpha}^{\ n} i_{L2\beta}^{\ p} - v_{g\beta}^{\ n} i_{L2\alpha}^{\ p} \right) \tag{14}$$

$$P_{s} = \frac{3}{2} \left(v_{g\alpha}^{\ n} i_{L2\alpha}^{\ p} - v_{g\beta}^{\ n} i_{L2\beta}^{\ p} \right) \tag{15}$$

$$Q_{s} = \frac{3}{2} \left(-v_{g\alpha}{}^{n} i_{L2\beta}{}^{p} - v_{g\beta}{}^{n} i_{L2\alpha}{}^{p} \right)$$
(16)

Comparison of the magnitudes of the oscillating power components in (5)-(10) and those in (13)-(16) shows that the power oscillations are reduced by using the positive-sequence based control.

2.4. Positive-sequence virtual-flux estimation

In order to use the positive-sequence component of the virtual flux for power estimation and synchronization, it has to be extracted from virtual flux estimated from the unbalanced grid voltage. The positive-sequence components of the virtual flux are given by:

$$\psi_{g\alpha}{}^{p} = \frac{1}{2} \left(\psi_{g\alpha} + j \psi_{g\beta} \right) \tag{17}$$

$$\psi_{g\beta}{}^{p} = \frac{1}{2} \left(-j\psi_{g\alpha} + \psi_{g\beta} \right) \tag{18}$$

where j denotes a counterclockwise vector rotation of 90°.

The phase shift of 90° can be obtained using several different methods presented in literature. One of these is the delayed signal cancellation method [23], [24]. In this method the phase shift is achieved by delaying a signal for a quarter of the fundamental time period. Another method is based on cascaded low-pass filters which were introduced for sequence decomposition and virtual flux estimation in [18]. This method makes use of the cascaded filters' phase shift of 90° and attenuation of 0.5 at the fundamental grid frequency. The second method is adopted in this paper, because it does not require storage of a large number of samples to achieve the delay.

3. PROPOSED SOLUTION

The maximum allowable current of a voltage source converter is limited by the current carrying capability of its insulated-gate bipolar transistors. This in turn determines the maximum power capacity of the converter at nominal voltage. During normal operation, the converter can deliver rated power without exceeding its maximum current capacity because the grid voltage is normally within $\pm 10\%$ of its nominal value. During a voltage dip, the grid voltage becomes less than 90% of its nominal value and for the converter to deliver rated power; its current increases and this may lead to damage of the insulated-gate bipolar transistors. During unsymmetrical voltage dips, the problem is made worse by the unbalance in the voltages, which leads to unbalance and distortion in the current. To protect the VSC and limit the current to safe levels during voltage dips, a current limiting algorithm is proposed and implemented [25]. The derivation of the algorithm is explained in the steps below.

The per-unit magnitude of the voltage during a voltage dip is quantified by a factor k_1 defined as:

$$k_1 = \frac{|\underline{v}_g|}{|\underline{v}_g(ref)|} = \frac{|\underline{\psi}_g|}{|\underline{\psi}_g(ref)|}$$
(19)

where $|\underline{v}_g|$ and $|\underline{\psi}_g|$ are the magnitudes of the voltage and the virtual flux respectively; $|\underline{v}_{g(ref)}|$ and $|\underline{\psi}_{g(ref)}|$ are the nominal magnitudes of the voltage and the virtual flux respectively. During a voltage dip, the value of k_1 is less than 0.9 while during normal operation $k_1 \ge 0.9$.

The per-unit loading of the VSC is given by a factor k_2 defined as:

$$k_2 = \frac{p}{s} \tag{20}$$

where S is the nominal apparent power rating of the VSC.

The factor k_2 is needed to determine the capacity of the converter being used for active power. If k_2 is less than one, the remaining capacity of the converter can be used for reactive power support if needed. The reactive power is limited to the available capacity of the converter to avoid overloading it. The reactive power limit is based on the idea [26], where the reactive power provided by a grid-connected VSC is limited to the capacity not being used for active power.

If $k_2 = 1$ and $k_1 < 0.9$ the active power reference is reduced proportionally to the voltage dip and the new active power reference is given by:

$$p_{ref}' = k_1 p_{ref} \tag{21}$$

where p_{ref} is the active power reference after limiting.

Since the full capacity of the converter is being used for active power, the reactive power reference is set to zero. If $k_2 < 1$ and $k_1 \ge 0.9$, the active power reference limit is not applied, since the magnitude of the grid voltage is within its allowable limit. However, the converter is not fully loaded, and if needed, the remaining capacity can be used for reactive power. The capacity of the converter not being used for active power is given by:

$$q_a = \sqrt{S^2 - p_{ref}^2} \tag{22}$$

where q_a is the capacity of the converter available for reactive power. If $k_2 < 1$ and $k_1 < 0.9$, the active power reference is reduced as shown in (29). The capacity of the converter not being used for active power is given by (23).

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$$q_a = \sqrt{(k_1 S)^2 - (k_2 p_{ref}')^2}$$
(23)

The use of the current limiting algorithm described by (19) to (23) ensures that the converter is operated safely without exceeding its current rating during normal operation and more importantly during voltage dips. The flowchart of the current limiting algorithm is shown in Figure 2. The algorithm is implemented once in every sampling cycle.



Figure 2. Flowchart of current limiting algorithm

4. SIMULATION RESULTS AND DISCUSSION

The block diagram of the control scheme with positive-sequence virtual flux control and current limitation is shown in Figure 3. The grid-connected converter and its controller are simulated in MATLAB/Simulink, with the parameters given in Table 1. To allow for comparison of systems with different power and voltage levels, the per-unit system using the peak values of the phase voltage and the line current as base voltage and base current respectively, is used.

The system is investigated during a single-phase voltage dip of 50% in phase-a for different values of active power and reactive power. The results of the proposed positive-sequence virtual flux control with current limiting are presented and compared with the results of the conventional direct power control with space vector modulation (DPC-SVM).

The first case investigated is when the converter is delivering rated active power and zero reactive power to the grid. The results obtained during the voltage dip are shown in Figure 4. Figure 4(a) illustrates the conventional DPC-SVM control while Figure 4(b) describes the positive-sequence VF control with current limiting. In Figure 4(a) the current is distorted and the peak value of the currents in phase-b and phase-c exceed 1 pu. The average total harmonic distortion (THD) of the current is 19.8 % for all the phases. Both the active power and the reactive power have got double grid frequency oscillations whose peak-to-

peak value is 0.8 pu. In Figure 4(b), the current is balanced, and sinusoidal with an average THD of 2.58 % and its peak value is limited to 1 pu. There are still double grid frequency oscillations in the active power and the reactive power, but their peak-to-peak values are reduced to 0.35 pu and 0.65 pu respectively.



Figure 3. Block diagram of the proposed control scheme

Table 1. Parameters of simulation model

Parameter	Value
Rated power, P _n	100 kW
Grid voltage, V _L	415 V
Grid frequency, f	50 Hz
DC Voltage, V _{dc}	800 V
Inverter side inductance, L ₁	0.35 mH
Grid side inductance, L ₂	0.1 mH
Filter capacitor, C _f	90 µF
Sampling frequency, f _s	10 kHz
Switching frequency, f _{sw}	10 kHz
Base power, S _b	100 kVA
Base voltage, V _b	339 V
Base current, I _b	197 A

The second case investigated is when the converter is delivering rated reactive power, and zero active power. The results are shown in Figure 5, which are illustrated in Figure 5(a) for the conventional DPC-SVM and Figure 5(b) for the positive-sequence VF with current limiting. In Figure 5(a), the current is distorted with an average THD of 19 %, and unbalanced, although the peak value of the current in all the phase is around 1 pu. The peak-to-peak value of the oscillations in the active power and the reactive power are 0.77 pu and 0.43 pu respectively. In Figure 5(b), the current is balanced and sinusoidal with an average THD of 2.22 %, and its peak value is limited to 1 pu. The oscillations in the active power and the reactive power have peak-to-peak values of 0.4 pu and 0.2 pu respectively.

The third case investigated is when the converter is delivering 0.8 pu active power and 0.6 pu reactive power. The results are shown in Figure 6 which are illustrated within Figure 6(a) for the conventional DPC-SVM and Figure 6(b) for the positive-sequence VF with current limiting. In Figure 6(a), the currents are distorted with an average THD of 18.6 %, and unbalanced, with the current in phase-c having the highest peak value exceeding 1 pu. The peak-to-peak value of the oscillations in both the active power and the reactive power is 0.75 pu. In Figure 6(b), the current is balanced and sinusoidal with an average THD of 2.41 %, and its peak value is limited to 1 pu. The oscillations in the active power and the reactive power both have a reduced peak-to-peak values of 0.35 pu.



Figure 4. Simulation results with active power output, (a) conventional DPC-SVM and (b) positive-sequence VF with current limiting



Figure 5. Simulation results with reactive power output, (a) conventional DPC-SVM and (b) positivesequence VF with current limiting



Figure 6. Simulation results with active and reactive power output, (a) conventional DPC-SVM and (b) positive-sequence VF with current limiting

In all the above cases, significant reduction in the distortion and imbalance of the current has been achieved with positive-sequence virtual-flux control. The oscillations in the active power and the reactive power are also significantly reduced in magnitude. This is because the negative-sequence component of the current is eliminated, and the magnitude of the current is limited to its rated value in all the phases. This clearly shows that the proposed positive-sequence virtual-flux control is suitable for control of grid-connected converter during unsymmetrical voltage dips at different levels of active and reactive power.

5. CONCLUSION

In this paper the control of a direct power-controlled grid-connected voltage source converter during unsymmetrical voltage dips has been presented. The control focuses on limiting the current and injecting balanced and sinusoidal currents during unsymmetrical voltage dips. The proposed control uses the positive-sequence virtual-flux for power estimation and grid synchronization. To limit the current, a new current limiting algorithm has been proposed and implemented in simulations and experiments. The current limiting algorithm can work both for symmetrical and unsymmetrical voltage dips and has been demonstrated for the unsymmetrical voltage dip which is the more common and worse scenario. Simulation results show that the control objectives are achieved, and the VSC can ride through grid voltage disturbances without risk of damage to the semiconductor devices because the current is limited to the rated capacity of the converter.

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