A High Performance Sigma-Delta ADC for Audio Decoder Chip

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Abstract

This paper gives a high performance sigma delta Analog to Digital Converter (ADC) applied in computer audio decoder chip. In this design, a 3rd-order single-loop CIFF topology is chosen to achieve the high performance ADC. Its signal bandwidth is 20 KHz, sampling frequency is 10.24MHz and oversampling ratio is 256. Local feedback coefficient g_1 is used to reduce quantization noise. The non-linear model of modulator is given and the stability is analyzed. It is got that when quantizer gain is bigger than 0.322 the system is stable. According to simulation, Signal to Noise Ratio (SNR) is 123.1dB and Effective Number of Bits (ENOB) is 20.15bits. When input level is bigger than -3dBFs, the modulator is overload and becomes unstable. Then the integrator, quantizer and feed forward summation in ADC circuit are designed. Then the ADC is implemented in 0.6um CMOS process, and the test result shows that its performance is 99.28dB.

Keywords: Sigma Delta, Loop Stability, Audio Decoder

1. Introduction

In the field of high-fidelity audio, high performance Analog to Digital Converter (ADC) is greatly needed in computer audio decoder. To keep the audio signal fidelity, the precision of ADC should be as high as 16 bits and the signal bandwidth is in the range which is at least as big as 20KHz [1-3]. To traditional ADCs like double-integrating ADC, successive approximation ADC, and folding ADC, it is hard to achieve high precision. So sigma-delta ADC now is more widely used in computer audio decoder chip [4-7].

Sigma-delta ADC has many advantages: high precision, low power consumption, high density of integration, digital output and so on. But there are also many challenges in the design. First, in computer audio decoder chip, the precision should at least be bigger than 16bit. Second in sigma-delta architecture, when the order is bigger than two, the stability is a big problem in high order sigma delta ADC [8-9]. Last, the input signal would cause integrator or quantizer saturation and make the ADC overload [10-13]. In this paper, all these problems are investigated deeply.

In second section of this paper, the system design of the 3rd-order modulator system is given. Then the non-linear model and stability analysis are given in third section and simulation result is discussed. In fourth section the circuit of the ADC is designed in fourth section. In fifth section the ADC chip is tested. In last section a conclusion is presented.

2. System-level Analysis and Design

For sigma-delta ADC, there are two traditional structures: single loop structure and Multi-stage noise Shaping (MASH) structure. Each of these structures can be realized with one-bit quantizer or multi-bit quantizer. For single loop sigma delta modulator, it is not sensitive to mismatch of capacitances and charge leaking. In order to increase the precision high order is needed. But this would make the system conditional stable. MASH modulator is always stable. But mismatch of capacitances and charge leaking have big influence on MASH modulator. This

requires a very good manufacturing process. And MASH modulator has digital part, which would increase the complexity of the circuit. In this design, single loop structure is chose [14-15].
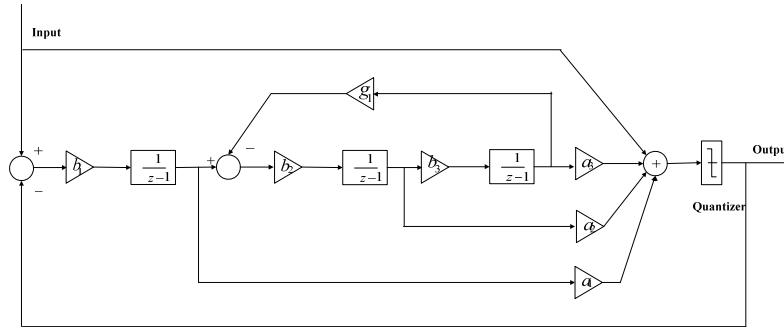

Figure 1. Block Diagram of 3rd-order ΣΔ ADC System

Single loop modulator has two main structures: Chain of Integrators with weighted FeedForward summation (CIFF structure) and Cascade of Integrators with distributed FeedBack (CIFB structure). CIFF structure is a wonderful structure to realize Butterworth filter and its signal transfer function is flat in signal bandwidth. In CIFB structure the input and output of integrators include signal and quantizer output, so the amplitude of integrators' input and output is very big. Little gains are required in CIFB structure. The gain in switch-capacitor circuit is realized by proportional capacitors. Little gains means big capacitors which would lead to more power consumption and bad output settle. CIFF structure has more advantages than CIFB structure [15-17]. So this paper also chooses the CIFF structure.

For sigma-delta ADC, the higher order and higher oversampling ratio achieve higher precision. In computer audio application, 16 bit precision is needed. So in this paper a third-order single loop CIFF structure modulator is designed. The signal bandwidth is 20KHz, oversampling ratio is 256, and the sampling clock is 10.24MHz. The third-order sigma-delta ADC topology is shown as Figure 1. There are three integrators, a one bit quantizer and gains.

In this modulator, the open loop transfer function $L_0(z)$ can be written as follow:

$$L_0(z) = -\frac{a_1 b_1}{(z-1)} - \frac{a_2 b_1 b_2 (z-1) + a_3 b_1 b_2 b_3}{(z-1)[(z-1)^2 + b_2 b_3 g_1]} \tag{1}$$

Where a_1, a_2, a_3, b_1, b_2 and b_3 are the proportional capacitances in circuit. The feedback transfer function $L_1(z)$ can be written as:

$$L_1(z) = 1 + \frac{a_1 b_1}{(z-1)} + \frac{a_2 b_1 b_2 (z-1) + a_3 b_1 b_2 b_3}{(z-1)[(z-1)^2 + b_2 b_3 g_1]} \tag{2}$$

From the open loop transfer function $L_0(z)$ and the feedback transfer function $L_1(z)$, the signal transfer function (STF) and quantizer noise transfer function (NTF) can be written as follows:

$$STF(z) = \frac{L_1(z)}{1 - L_0(z)} = 1 \tag{3}$$

$$NTF(z) = \frac{1}{1 - L_0(z)}$$
$$= \frac{(z-1)[(z-1)^2 + b_2 b_3 g_1]}{[(z-1) + a_1 b_1][(z-1)^2 + b_3 b_4 g_1] + a_2 b_1 b_2 (z-1) + a_3 b_1 b_2 b_3} \tag{4}$$

The STF is always equal to one which ensures no loss of signal. The NTF shows a high-pass filter characteristic to reduce quantization noise in bandwidth.
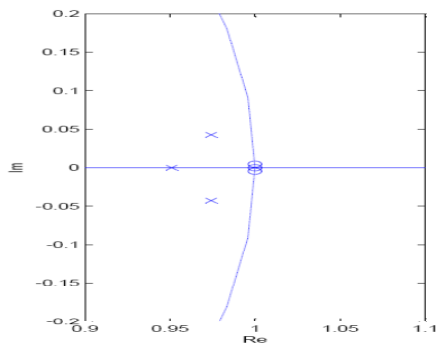

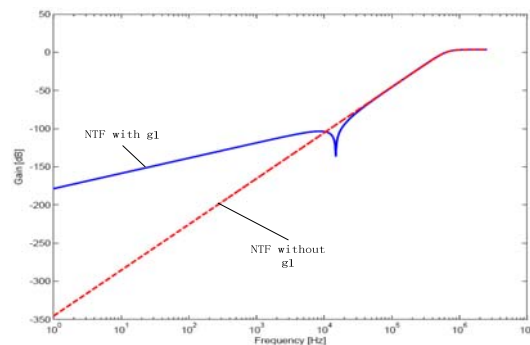Figure 2. Zeros and Poles of Third-order Butterworth Filter

Figure 3. NTF Transfer Characteristic with g_1 and without g_1

The next step for system design is to choose a high-pass filter transfer function for noise transfer function. The most commonly used filter transfer function is Butterworth filter, Chebyshev I filter and Chebyshev II filter. The Butterworth filter function has advantages like passband flatness, inhibition of excessive band gain and good stability. Therefore the Butterworth filter function is picked as the noise transfer function. Butterworth transfer function is shown as follow:

$$H(z) = \frac{(z-1)^n}{D(z)} \tag{5}$$

The poles and zeros of third-order Butterworth filter are shown as Figure 2. The zeros are all set around the real value one to suppress quantization noise in baseband. The poles are all set appropriately in unit circle to make the system stable. The Butterworth filter's poles and zeros correspond to poles and zeros of NTF. So the gain coefficients like a_1, a_2, a_3, b_1, b_2 and b_3 can be got from the zeros and poles as Table 1. To increase noise-shaping ability in signal baseband, the local feedback coefficient g_1 is added into last two integrators in modulator system. The local feedback g_1 spilt two zeros not slightly off real value one. This generates a minimum value for noise transfer function in signal baseband. The NTF transfer characteristic with g_1 and without g_1 are plotted in Figure 3. From the Figure 3, it is got that NTF with g_1 has better noise-shaping ability than NTF without g_1.

Table 1. Value of the Gain Coefficients

Gain	a1	a2	a3	b1	b2	b3	g1
Value	1.877	2.183	2.46	0.427	0.31	0.135	0.002

3. Stability Analysis

In traditional computer audio sigma-delta ADC system, it is always considered as a linear system. The quantizer in modulator has gain as big as one. However the modulator system is not a linear system. The quantizer has a gain k_q.

The nonlinear model of the third-order sigma-delta modulator system is described as Figure 4. In figure quantizer consists of gain k_q and quantization noise. The quantizer gain k_q is a variable changed with ADC input. So the whole modulator system is conditionally stable.

There is a range of k_q that make sure the system is stable. The nonlinear noise transfer function is:

$$NTF'(z) = \frac{1}{1 - k_q L_0(z)}$$

$$= \frac{(z-1)[(z-1)^2 + b_2 b_3 g_1]}{[(z-1) + k_q a_1 b_1][(z-1)^2 + b_2 b_3 g_1] + k_q a_2 b_1 b_2 (z-1) + k_q a_3 b_1 b_2 b_3} \tag{6}$$

Limit cycle is used to calculate the range of k_q. Based on Equation (6), the limit cycle of third-order signal-delta modulator is plotted in Figure 5. From the limit cycle result, it got that when the quantizer gain is bigger than 0.322 the system is stable.
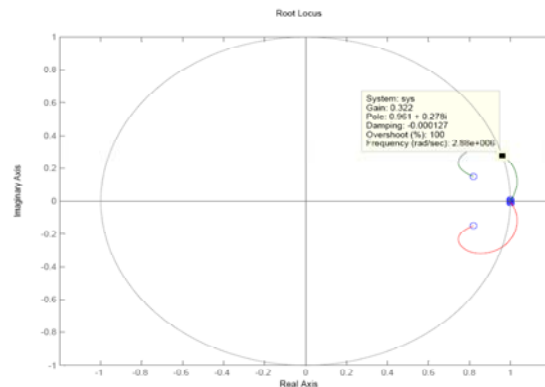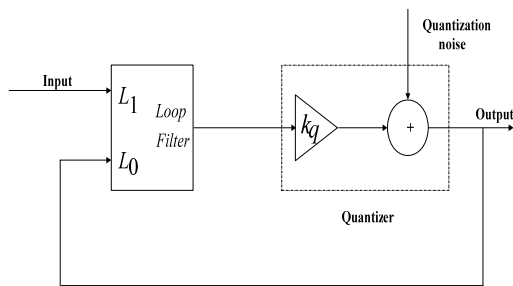

Figure 4. The Nonlinear Model of Sigma-delta System

Figure 5. Limit Cycle of Third-order Modulator

4. System Simulation.

The designed third-order sigma-delta modulator system is simulated by Simulink. In simulation the input signal is 100KHz sine wave, sampling frequency is 10.24MHz and signal bandwidth is 200KHz. The output Power Spectrum Density (PSD) is shown as Figure 6. The SNR is 123.1dB and ENOB is 20.15 bits. The performance satisfies the demand of computer ADC decoder.
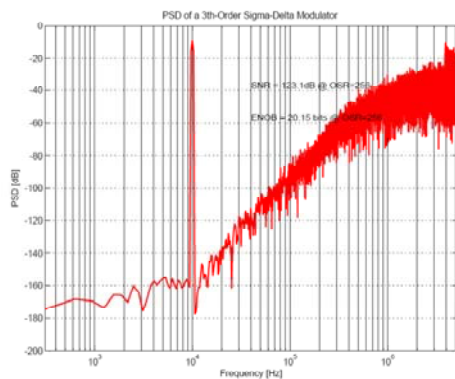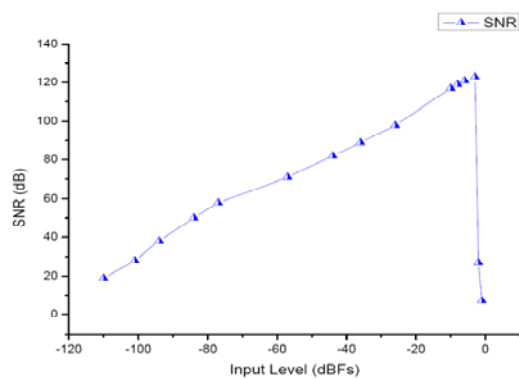

Figure 6. PSD of Modulator Output

Figure 7. Relation between SNR and Input Level

The relation between SNR and input level is described in Figure 7. When input level is smaller than -3dBFs, SNR is almost linear with input level. When input level is bigger than -3dBFs, the modulator is overload and becomes unstable.

5. Circuit Module in ADC
5.1. Integrator in ADC

The integrator used in this ADC is the same phase switch-capacitor integrator. Its work principle is: when $P1$ is high, the switch $S1, S3$ are turned on, $P2$ is low and the switch $S2, S4$ are turned off. In this time the input signal of integrator charges the sample capacitor $C1$. When $P1$ is low, the switch $S1, S3$ are turned off, $P2$ is high and the switch $S2, S4$ are turned on. In this time electric in $C1$ is transmitted into integrate capacitor $C2$.

According to conservation of charge, the amount of electric in sample capacitor $C1$ is equal to the amount of electric change in integrating capacitor $C2$. The equation can be written as follow:

$$[V_{out}(nT+T) - V_{out}(nT)]C_2 = V_{in}(nT)C_1 \tag{7}$$

Write the equation into Z-transform, it gets the transform function of switch-capacitor integrator:

$$I(z) = \frac{V_{out}(z)}{V_{in}(z)} = (\frac{C_1}{C_2})\frac{z^{-1}}{1-z^{-1}} = (\frac{C_1}{C_2})\frac{1}{z-1} \tag{8}$$

The capacitor ratio $C1/C2$ is used to realize the integrator gain b_1, b_2 and b_3. In this integrator clock $P1$ and $P2$ have delay clock $P1d$ and $P2d$ to turn off $S1$ and $S2$ advancely. This can prevent interference of switch charge injection to sample capacitor $C1$.
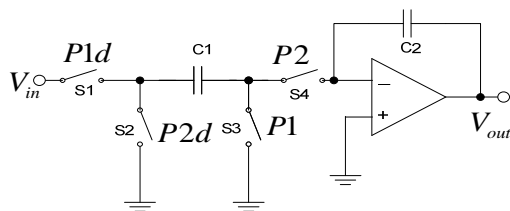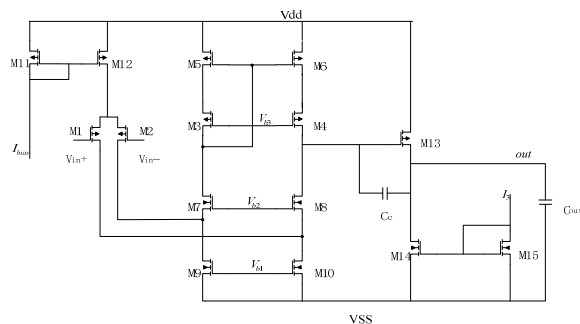

Figure 8. Same Phase Switch-capacitor Integrator

Figure 9. The Amplifier in Integrator

The amplifier used in this integrator is plotted in Figure 9. It is a folded cascode two-stage miller amplifer. M_1 and M_2 is the input mosfet and use the PMOS to decrease the 1/f noise. M_{12} and M_{11} constitute current mirror to supply the bias voltage for M_{12}. $M_5 \, 、 M_6 \, 、 M_9$ and M_{10} are current mosfet to supply current for first stage. $M_3 \, 、 M_4 \, 、 M_7$ and M_8 are cascode mosfet to increase gain of amplifier. Gate voltage of M_5 and M_6 are provided by source port of M_3 to increase the output swing of first stage. Miller capacitor C_c is used to compensate the first pole and second pole in amplifier to insure stability of amplifier. The second stage is made up by M_{13} and M_{14}. Though the second stage gain is low, it improves the amplifier output swing. C_{out} is the load capacitor in output.

The gain of this amplifier is :

$$A_v = g_{m1}(g_{m3}r_{o3}r_{o5}) \,\|\, (g_{m7}r_{o7}r_{o9})g_{m13}(r_{o13} \,\|\, r_{o14}) \tag{9}$$

Where g_{m1}, g_{m3}, g_{m7} and g_{m13} are the transconductance of M_1, M_3, M_7 and M_{13}. r_{o3}, r_{o5}, r_{o7}, r_{o9}, r_{o13} and r_{o14} are resistors bewteen source and drain of M_1, M_3, M_7, M_9, M_{13} and M_{14}.

Implemented in 0.6um CMOS process, the gain of amplifier is 81.2dB, unit gain bandwidth is 41.3MHz. When load capacitor is 10pF, the phase margin is 62.3°. The rising slew rate is 40.2V/us and the falling slew rate is -38.6V/us. The input swing is 0.1-3.8V and output swing is 0.1-4.7V.

5.2. Quantizer in ADC

The quantizer in this ADC is realized by a one-bit comparator. When input signal is higher than middle voltage, the output would be a high signal. When input signal is lower than middle voltage, the output would be a low signal. In ADC it requires quantizer to distinguish as low as minimum voltage, behave fast and ability to latch the result.
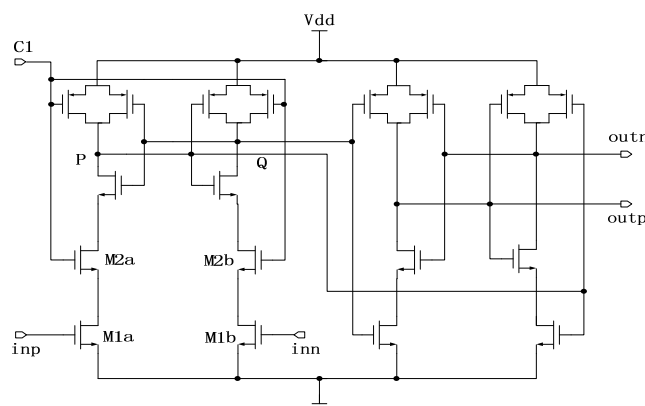

Figure 10. One-bit Quantizer Circuit

The circuit of quantizer is shown in Figure 10. It is a dynamic comparator with latch. When the clock control signal is low, the nodes P and Q are preset with supply voltage. When the clock control signal is high, presetted nodes P and Q discharge respectively through M_{1a} and M_{1b}. When the node voltage of the P and Q is lower than the threshhold voltage of the MOS transistor, the latter two inverters of the latch to change the value of the original the *outn* and *outp*, until it reaches the voltage value comparision. The result is latched in quantizer. The power consumption of the quantizer is very low and its comparision speed is very fast.

With the advancement in networking and multimedia technologies enables the distribution and sharing of multimedia content widely. In the meantime, piracy becomes increasingly rampant as the customers can easily duplicate and redistribute the received Although encryption can provide multimedia content once a piece of digital content is decrypted, the dishonest customer can redistribute it arbitrarily

6. Test and Discussion

The ADC is fabricated in 0.6um CMOS process. The power spectrum density of the ADC is obtained by the oscilloscope in Figure 11. The test result shows that the SNR of this ADC is 99.28dB and ENOB is 16.2bits. The test result is lower than simulation, because the electronic noise in circuit affects the performance of ADC. The single-end amplifier applied in this ADC result in non-linearity and this brings up the harmonic in signal bandwidth. So to increase the performance of ADC, it is adviced to use correlated double sample to decrease electronic noise and employ fully differential circuit to increase linearity to suppress harmonic.
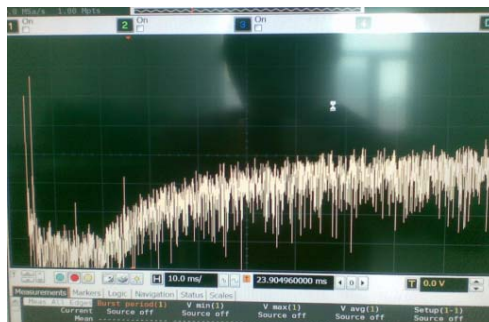
Figure 11. Test PSD of ADC

7. Conclusion

This paper presents design of high performance sigma-delta ADC applied in audio decoder chip. The CIFF third-order sigma-delta modulator system is analyzed. The Butterworth filter function is used to realize the NTF of modulator. Based on nonlinear model, it is got that when the quantizer is bigger than 0.322 the system is stable. Through Simulink simulation, the SNR of system is 123.1dB and ENOB is 20.15bits. The performance satisfies the demand of computer ADC decoder. From the output histograms of three integrators, it is gotten that the output ranges of three integrators satisfy the limit of integrators. And SNR is almost linear with input level. When input level is bigger than -3dBFs, the modulator is overload. The test result shows that the SNR of this ADC is 99.28dB and ENOB is 16.2bits. The single-end amplifier in this ADC brings up the harmonic in signal bandwidth.

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