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Single board re-spin for testing bridge transducer products

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ABSTRACT

Integrated circuit (IC) testing involves equipment and product interface board setup. Complex interfaces and obsolete components are some of the factors affecting the board functionality which results in manufacturing downtime. The legacy boards must be simplified so that it needs advanced tools for the lay-out and designing of test boards. This study proposes a solution for board functionality issues by re-spinning the legacy two-board interface into a single board interface. It converts the standard use of boards and standard contacting to single board interface (SBI) and plunge-to-board (PTB) contacting. As a result, the setup time is improved, minimizing board and system repair due to mismatch and contact issues. The board endorsement for contact issues were trimmed from 82 to 46 counts. Other board related issues are decreased by 60% based on the analysis of the correlation in the processes. Additionally, mismatches, which are system issues, are lessened which promotes fixtures maintainability.

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1. INTRODUCTION

In a test manufacturing floor, the testing of an integrated circuit (IC) involves set-up of equipment and product interface test board to perform the process [1]. The functionality of these boards from time to time fails, that is why repairs are required. The excessive setup time and repair made on test boards contribute to loss of revenue. An IC product manufacturer needs to control such events to deliver on time and gain excellent profitability. The factors affecting board functionality that results in manufacturing downtime are its complex interfaces and its components becoming obsolete. For these reasons, advanced tools for design and lay-out of test boards are used to simplify legacy boards. Component search tools can replace old components with one that is updated and has long life-spans.

In the test manufacturing floor, there are two types of device under test (DUT) [2], [3] contacting; (a) standard (STD) contacting, and (b) plunge-to-board (PTB) contacting. STD contacting is prone to worn-out of hyper-tack pins and contactor pins which also frequently undergoes rework of pins which can be translated to additional operations cost. Whereas in PTB contacting, setup is using surface-mounted contactor. These contactors have resistances that when not properly designed and monitored, can make an impact in the performance of the DUT [4]. It must not affect the DUT's performance as it establishes contacts for tests [5]-[8].

An ideal setup procedure starts from hand test to handler setup. The setup time depends on setup category; (a) Type1 setup (same fixtures used but new setup verifier (SUV) and test program which has 30 minutes of setup time, (b) Type2 setup (new board, new SUV and new program) has 60 to 90 minutes of

setup time, (c) Type3 setup (new handler, new board, new SUV and new program) has 90 to 180 minutes of setup time. For more efficient and fast setup, there must be optimization in the processes involved. These can be in the form of development of devices and or overhauling of processes.

There are two types of boards for testing the bridge transducer products: two-board combination interface test board, and single panel board. Bridge transducers are primarily used as sensing devices. Interfacing components to these bridges can be critical when small changes are amplified [9]–[12]. Therefore, careful test setup must be conducted. When the setup exceeds the allotted time and creates unplanned downtime, it is considered as hard-to-set up (HATSUP). The HATSUP devices are considered as sources of profit loss. Therefore, redesigning the old board is necessary. A HATSUP resolution may be done by re-spinning the lay-out to improve the setup time. Bridge transducer product is a HATSUP device. Its hand test verification to handler setup must be resolved by re-spinning the two-board interface into a single board interface.

This paper presents a solution on HATSUP bridge transducer product by re-spinning the two-board combination family board (FB) and DUT Board (DB) into an single board interface (SBI) to reciprocate the high setup and verification down time and board hits endorsement into revenue for this product. Specifically, the setup time and verification time is trimmed down by 50 percent. The schematic layout of family board and DUT board combination is re-spun into an SBI. The fabricated board is verified through an automated test equipment (ATE) for circuit bugs for board improvement [13]–[17].

2. METHOD

2.1. Re-spinning

Re-spinning is a process that simplifies and upgrades complicated and old designs of boards [18], [19]. Legacy Test Board handles the testing of the transducer bridge products. It is composed of two boards, the FB and a DUT Board. These boards are re-spun into an SBI which starts with the new hardware requisition form (NHR). In this setup, a software layout of schematic is used with updated components available in the company and commercially which are compliant with restrictions and standards.

Re-spin process takes several methodologies including schematic designing, PCB lay-out and design, debugging [20], and correlation of data [21]. In schematic designing, factors such as restriction of hazardous substance (RoHS) compliance, the tolerances of components, and phase out or component retirement are considered. In PCB lay-out and design, the transmission lines should match impedances to achieve maximum power transfer, always considering the critical component placement [22], [23].

The standard PCB and re-spin process schematic and lay-out flow is completely shown in Figure 1. The layout of schematic was performed using advanced tools for placing of updated list of components and allocation of resources. An electronic component search engine was used to check components commercially and internally available to be used for schematic layout. The libraries provide more options for specific parts description and application. This tool standardizes the design with its features, such as device footprint, voltage and wattage rating, package type, parts life span, and actual price on the market.

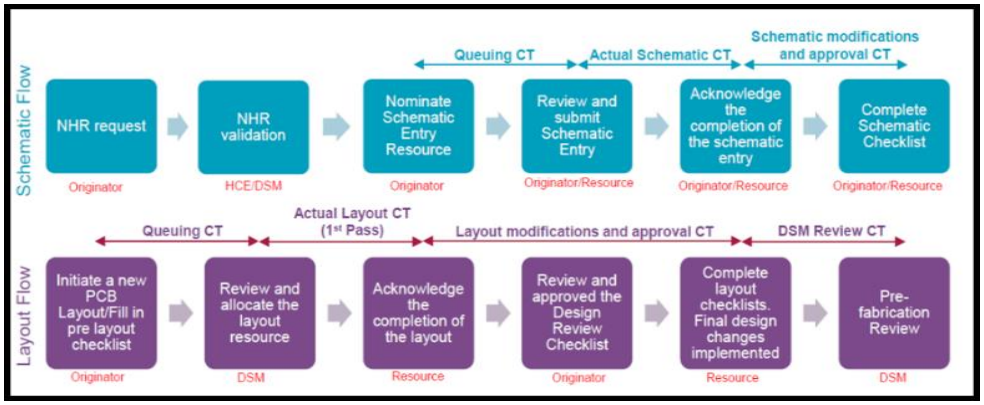


Figure 1. Schematic and layout flow

The block diagram for the basic design entry from schematic to physical board is presented in Figure 2. The schematic entry is created using the advanced layout tool. It will then proceed to packaging the design. It should have synchronized schematics in order to avoid errors in the layout process when

discrepancy happens. The schematics will be revised and updated when the layout is completed. The old schematics will be archived for future references.

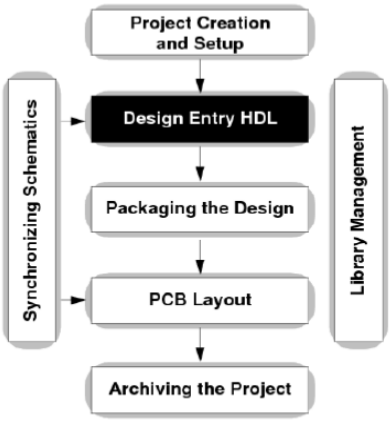


Figure 2. Design entry diagram

The schematic entry for PCB layout process starts from project creation using the Cadence Software and performs the netlist placement to re-spin the previous schematic with updated electronic components for parts list revision [24]. The design packaging window is where the bill of materials is generated to be automatically laid out and routed to the best placement of circuits to comply with the transmission line specifications as presented in Figure 3. The search filters provide specific library location of the parts description. This search engine is but limited to the components available in the company stack items, otherwise the items will be outsourced. The menu for search and filtering of components needed for the schematic entry.

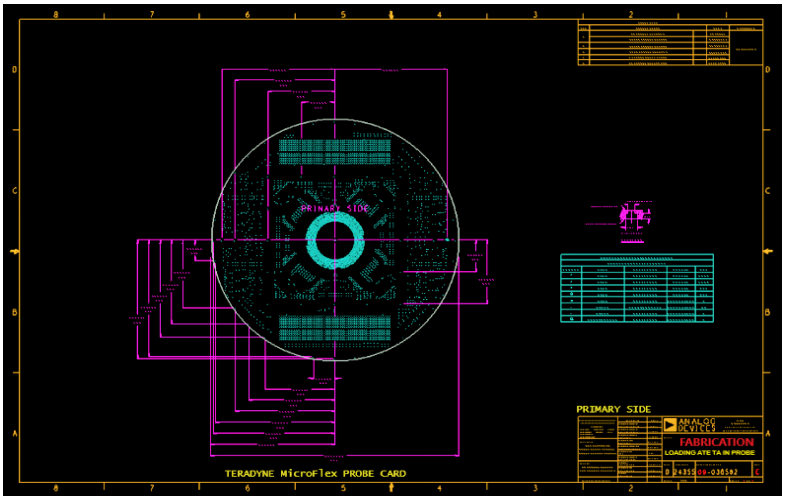


Figure 3. PCB layout

The fabrication of PCB layout will be executed when the schematic entry and pre-fabrication review has been approved, as shown in Figure 4. The PCB fabrication process needs to be outsourced since the process needs elaboration and involves comprehensive design, which has vital considerations on specifications of layout by the company and global standards. Some important processes have to be fully understood by the users in terms of the whole process, considerations in transmission lines setup, sensitivity on laying out, and design for manufacturability.

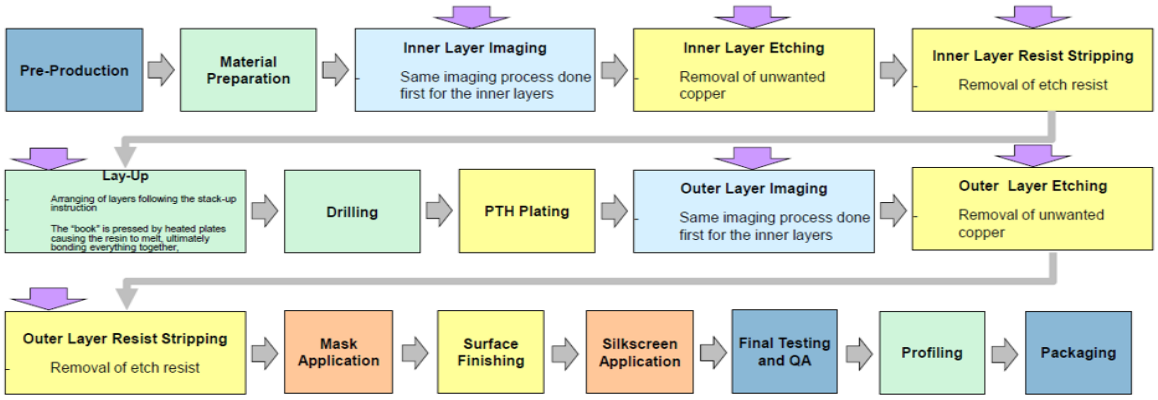


Figure 4. Test process of newly re-spin board

3. RESULTS AND DISCUSSION

3.1. Design fabrication and tests

The new board for bridge transducer product in single board fixture is shown in Figure 5. This new SBI has new sets of relays which replaces the obsolete relay components from the old board design. The 2 multiplexers (MUXs) IC13 and IC24 which are plastic lead chip carrier (PLCC) are replaced by small outline integrated circuit 300 mils (SOIC-300) to address the components obsolescence. The SBI will undergo debugging, as the first step to ensure correct voltage supplies, circuit connections, and responses of the new board program before it is subjected to the correlation process.

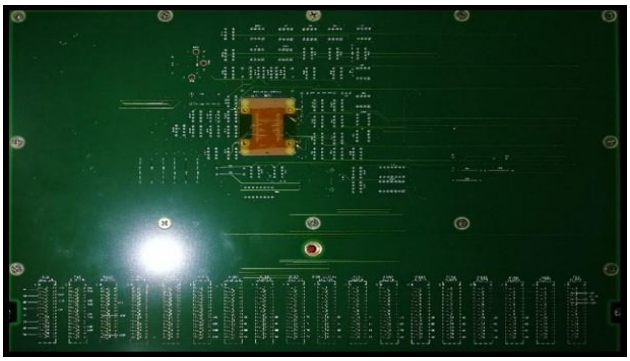


Figure 5. Finished single board interface

3.2. Device test results

When results passed, the new re-spin board is now ready for the correlations tests to check and further repair when needed. The correlation process compares all parameters of the Bridge Transducer product between the old and new board. Any shifting parameter is checked and verified for optimal design. CorL8 is the correlation tool used in this setup. A standard test data format (STDF) data tool shows the raw data, pareto chart of the top bin failure, and cumulative plots of tests [25]. This tool is also used for generating STDF files and performing statistical analysis on the population of tested devices. The mean and standard deviations can be computed using this tool. It can also be used to verify failures caused by setup fixtures and ATE systems. The new re-spin board is verified to pass the device test in the first stage Bin1 as shown in Figure 6. In this stage, the functionality of the re-spin board is verified.

The next stage is the correlation test between the device test of the old board and the new re-spin board. The mean shift and Sigma spread have been detected to fail during the correlation of Bin1. This failure in correlation is generally due to the difference between the old board's mean and SD as compared to the new re-spin board. These differences in mean and SD are not necessarily a fault but considered as an improvement. The debugging was conducted on a newly re-spin board specifically on IDDQ circuitry and the IDDQ pass on board calibration are shown in Figure 7. Its schematic comparison with notes on ground orientation are presented in Figure 8. Table 1 describes the common failures due to mean shift.

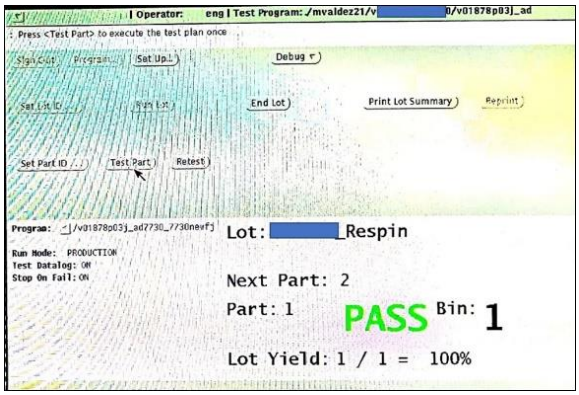


Figure 6. New re-spin board test

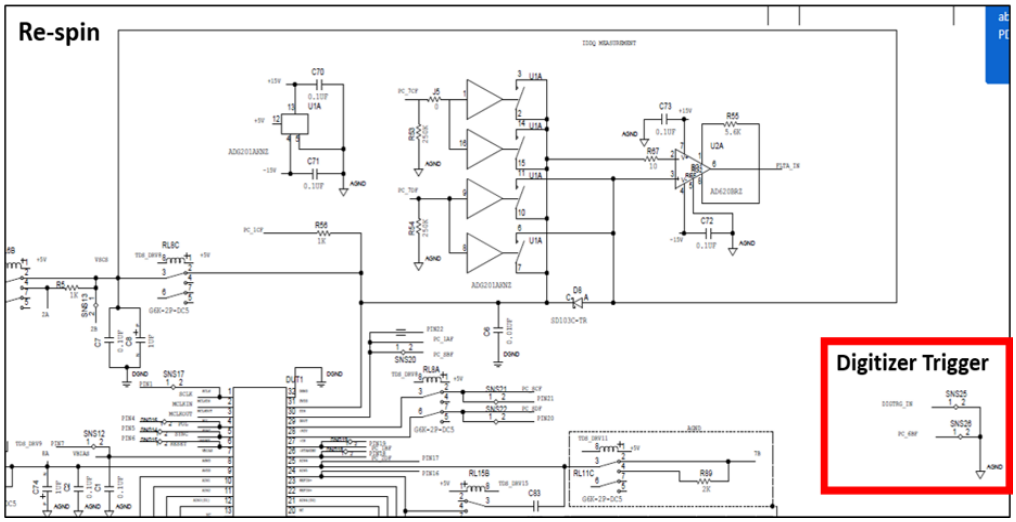


Figure 7. Re-spin with digitizer disconnected from the ground

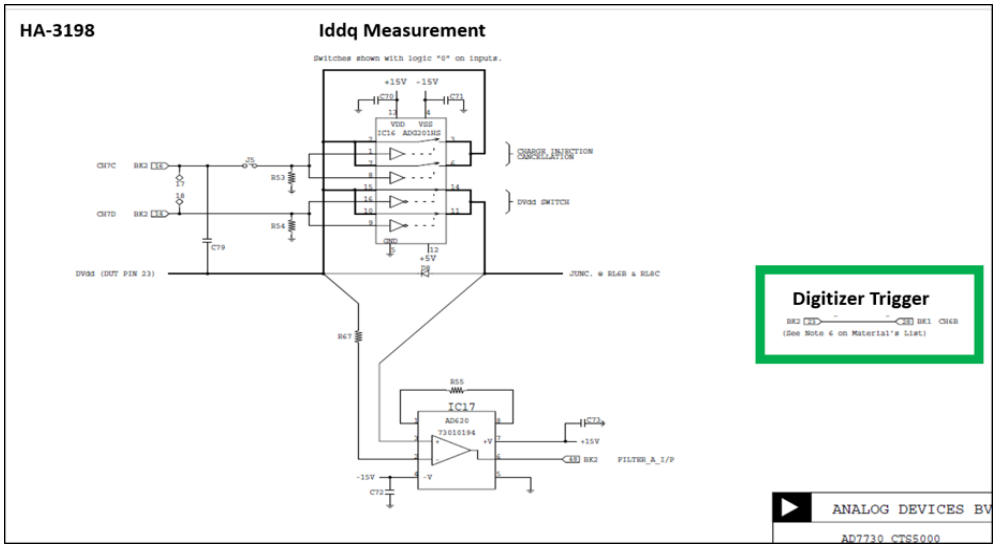


Figure 8. Iddq Measurement with direct connection of digitizer to a specified source and not ground

Table 1. Common failures due to mean shift described

Failures	Description
Leakage	Any voltage developed across this resistor would be directly due to input leakage.
SCLK	The digital vectors are repeatedly running whilst adjusting both vih and then vil on the SCLK input to establish the threshold points of each parameter.
IDDQ Test	Uses special circuits to enable the digital supply current to be measured during the digital vector pattern execution at every vector.
INL Test	Largely assumes that the part has no missing codes and therefore just takes a small number of conversion samples, typically 9, to assess the linearity of the input to output conversion.
DAC	The DAC is controlled via on-chip registers and is used to remove unwanted TARE values of up to ±80mV from the analogue input signal range.

There are 9 common failures due to mean shift with 5% tolerance listed in Table 2 and the graph is presented in Figure 9 (see Appendix). Figure 9(a) (see Appendix) presents the mean shift of 14.47% on the "D_jpSclk(Vt+-Vt-)" test parameter while the re-spin board going towards the upper limit of 0.78V. On the other hand, the "IDDQ Stby PowMax" test parameter has a mean shift of 9.76% as shown in Figure 9(b) (see Appendix), where the shift of the re-spin board is towards the upper limit of 90µW. Figure 9(c) (see Appendix) shows the "DAC525 chop zero difference" mean shift of 8.10% in which the re-spin board shifts towards the upper limit of 10µV. The mean shift of 20.72% on the "INL8bp SysCFS" test parameter is presented in Figure 9(d) (see Appendix) where the re-spin board is towards the upper limit of 500lsb. In Figure 9(e) (see Appendix), the shift of the re-spin board is towards the upper limit of 500lsb while Figure 9(f) (see Appendix) shows the mean shift is 9.02% on the "INL8bp NFS" test parameter. The shift of the re-spin board is towards the upper limit of 500lsb. Figure 9(g) (see Appendix) shows the mean shift of 27.50% on the "LkgAng Ain2- M result" test parameter. The Shift of the re-spin board is towards the upper limit of 40nA. Figure 9(h) (see Appendix) shows the mean shift of 17.6% on the "LkgAng Ain2+ M result" test parameter. The shift of the re-spin board is towards the upper limit of 40nA. Figure 9(i) (see Appendix) is the mean shift of 13.22% on the "LkgAng Ain2 Mo result" test parameter. The Shift of the re-spin board is towards the lower limit of -40nA. These data show the advantages of a re-spin board over the old one.

The common failures due to standard deviation shift at tolerance of 1.33% are presented in Table 3. The sigma spread result on the "IDDQ Stby PowMax" test parameter is 4.996 where the re-spin board is 3.696 higher than the allowable limit. The sigma spread result on the "INL8bp MaxPos" test parameter is 1.474 while the re-spin board is 0.174 higher than the allowable limit. The sigma spread result on the "IDDQ Delta" test parameter is 6.367 whlie the re-spin board is 5.067 higher than the allowable limit. These results show that re-spinning brings better results than the old setup.

Table 2. Nine common failures due to mean shift with 5% tolerance

Test parameter	Limit range	Mean shift	Percent shift over range (%)	Figure no.
D_ipSclk(Vt+-Vt-)	0.36	0.0521	14.47	9a
IDDQ StdBy PowMax	85	8.2981	9.76	9b
DAC525 chop zero difference	20	1.6218	8.10	9c
INL8bp SysCFS	1000	207.205	20.72	9d
INL8bp offset	1000	173.186	17.23	9e
INL8bp NFS	1000	90.21	9.02	9f
LkgAng Ain2- M	80	22.0025	27.50	9g
LkgAng Ain2+ M	80	14.08	17.60	9h
LkgAng Ain2 Mo result	60	7.9332	13.22	9i

Table 3. Three common failures due to standard deviation shift with 1.33% tolerance

Test parameter	OLD SD	NEW SD	Sigma spread criteria
IDDQ StdBy PowMax	0.134509	0.671973	4.996
INL8bp MaxPos error	0.137098	0.202098	1.474
IDDQ Delta	0.0251505	0.160133	6.367

3.3. Time study

One of the benefits of the project is to lessen setup time, verification and isolation time, and board repair time. Simulations are done on performing initial setup and hand test setup only. Given that boards coming from the hardware control room (HCR) are known to be good, ideal setup should pass easily. The hand test setup of the newly re-spin board takes not more than 10 minutes on installing hardware and loading of the test program. The device test passes bin1 thereafter, given that the re-spin board is a newly debugged board. For instance, the failing setup might be Board-related or tester-related, verification to another system

is needed to duplicate the failure to determine the root cause of failure. In this case, another 10 to 15 minutes will be added to the initial setup time.

The initial setup of old fixtures was conducted where the DUT board from the HCR is expected to be passing bin1. Installation of fixtures up to loading of the test program also takes 10 to 15 minutes. Even though the DUT board has come from HCR and is expected to pass bin1, it still needs to secure a passing family board (FB). On the first FB-DUT board combination, the setup failed on the AIN parameter, thus there is a need to verify another FB. Another 10 to 15 minutes is needed to install the spare FB, and unfortunately, the device test fails on open/short parameters. Therefore, verification of another FB is needed. This was passed after acquiring the fourth FB. In general, verification of FB requires 15 minutes, and during simulation, four FB were utilized which translates to one-hour verification and isolation time. Hence, board repair time is not yet considered.

The classic example for initial setup (hand test verification) is shown in Figure 10. It takes four FB prior making setup pass on hand test to identify the root cause of the failure during hand test verification. This is equivalent to a 60-minute verification time. Whereas upon using a re-spin board, it only takes 10 minutes to identify the root cause of the setup failure. The tester-to-tester verification was also conducted where it is easier to verify lone board rather than board combination. A reduction of 5-minute verification time was observed. In general, the verification time using re-spin board is 62.5% less than the verification of FB-DUT board combination.

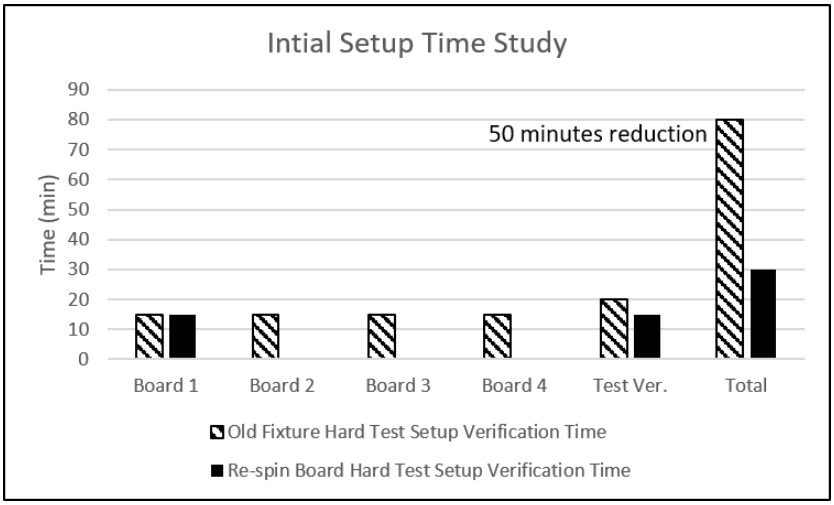
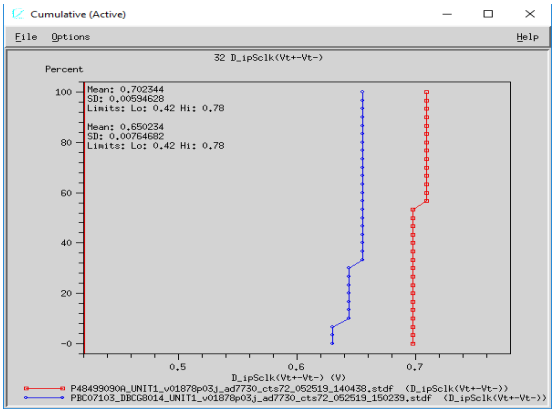


Figure 10. Initial setup time study (hand test verification)

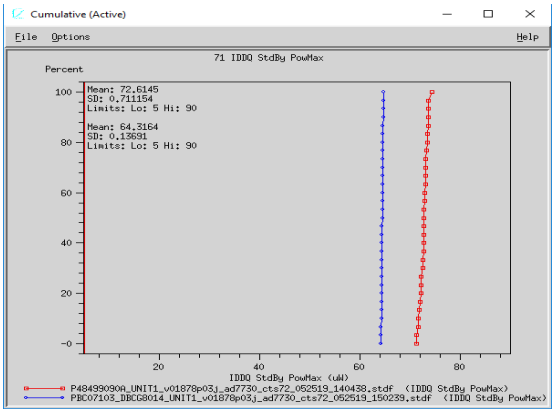
4. CONCLUSION

Through this setup, the surface mounted contactor fixed with four screws eliminates the replacement of damaged hyper tact pins. One of the factors on why there is HATSUP parts is because of the complexity of hardware of legacy design of boards and the obsolescence of its components. The specific part affected by this issue is the Bridge Transducer product. The Re-spin is conceptualized because of the bridge transducer product HATSUP. Through the re-spin process, the replacement time of the obsolete components is reduced compared to the former setup by replacing the two boards into a single board. A high passing rate for DUT check was achieved when the board calibration is passed. Correlation is done to pass bin1 on the re-spin board. It is not enough that the re-spin board will just pass bin1. For this reason, the integrity of the produced good units by the old board and the new board are compared to ensure that there will be no parameters that will lead to compromise the quality of tested units on newly re-spin board. The res-spin board takes advantage of applying it to the HATSUP part bridge transducer. Using the single board, SBI can reduce the setup time for isolation and/or verification by 50 minutes. Additionally, the less board endorsement due to FB-DUT board compatibility and due to contacting issues can be achieved because of the modeled dedicated board where the products and contacts have been converted to PTB type.

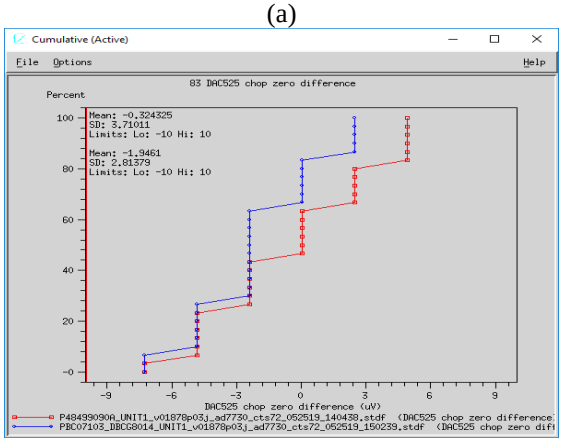
APPENDIX



(a)



(b)



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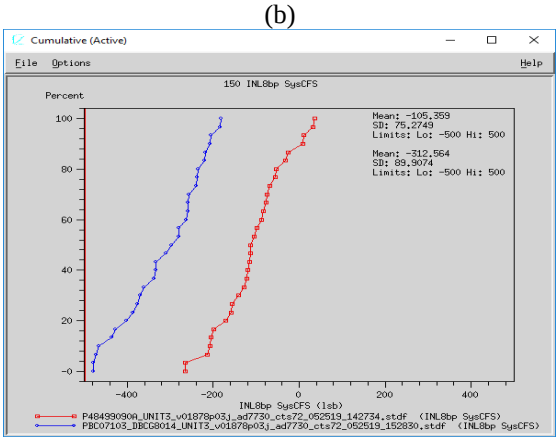

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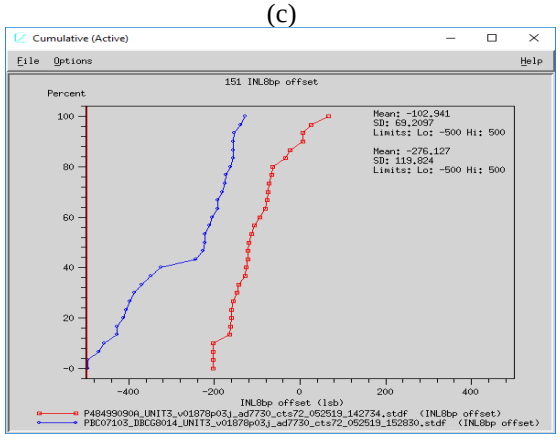

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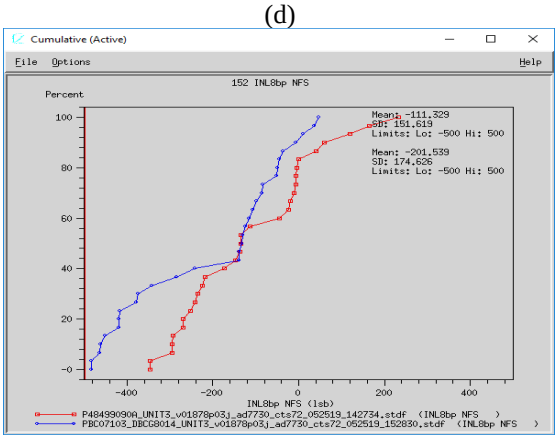

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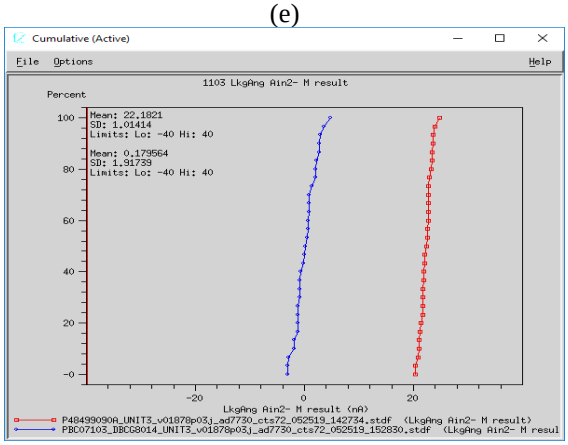

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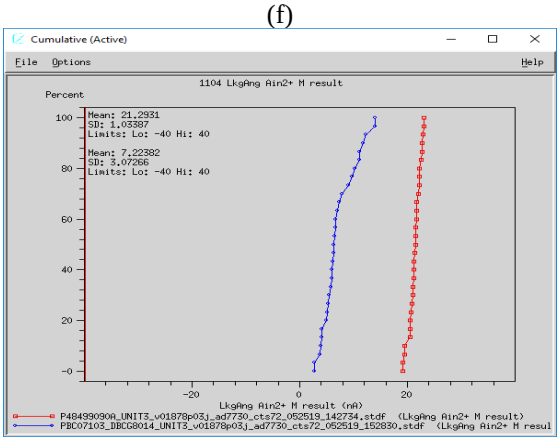

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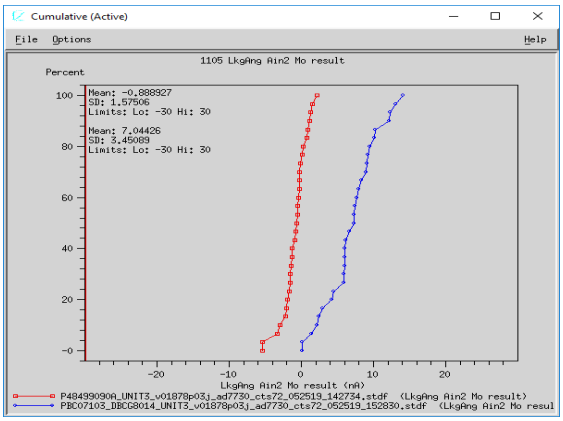

(i)

Figure 9. Nine common failures due to mean shift: (a) D_ipSclk(Vt+-Vt), (b) DAC525 chop zero difference, (c) INL8bp SysCFS, (d) INL8bp offset, (e) INL8bp NFS, (f) IDDQ Delta, (g) LkgAng Ain2- M result, (h) LkgAng Ain2+ M result, and (i) LkgAng Ain2 Mo result

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