Indonesian Journal of Electrical Engineering and Computer Science
Vol. 28, No. 2, November 2022, pp. 716~723
ISSN: 2502-4752, DOI: 10.11591/ijeecs.v28.i2.pp716-723

Fully synthesizable multi-gate dynamic voltage comparator for leakage reduction and low power application

Udara Yedukondalu[1], Vinod Arunachalam[2], Vasudha Vijayasri Bolisetty[3], Ravikumar Guru Samy[4]
[1]Department of Electronics and Communication Engineering, Sri Vasavi Engineering College, Andhra Pradesh, India
[2]Department of Electronics and Communication Engineering, Government College of Engineering, Tamilnadu, India
[3]Department of Electronics and Communication Engineering, Aditya College of Engineering and Technology, Andhra Pradesh, India
[4]Department of Electronics and Communication Engineering, M. P. Nachimuthu M. Jaganathan Engineering College, Tamilnadu, India

Article Info

Article history:

Received Feb 14, 2022
Revised Jul 18, 2022
Accepted Aug 11, 2022

Keywords:

Analog to digital converter
Fin field effect devices
Metal oxide
Offset noise
Voltage comparator

ABSTRACT

The paper presents the implementation of a standard cell multigate fully synthesizable rail-to-rail dynamic voltage comparator. The dynamic voltage comparator works on deep sub-threshold supply voltage VDD =0.3 V with common mode inputs. The common-mode input range is VDD/2 with minimum input offset voltage ranging between 8mV to 28mV. Thus the circuit is simulated at 180nm complementary metal-oxide semiconductor (CMOS) process. Hence the dynamic voltage comparator has measured and tabulated by corresponding output voltage, power dissipation. But the performance of CMOS device is not good when compared with fin field-effect transistor (FinFET) device. The leakage current is more in CMOS devices while in FinFET device due to the control of multi-Gates on the channel, the leakage current is reduced. This will improve the power consumption in the FinFET device when compared to CMOS devices. The comparator results shows that CMOS device is inferior when compared with FinFET device comparator. For the implementation of the comparator Spice model were used in this work. The software used in the project is synopsis Hspice.

Corresponding Author:

Udara Yedukondalu
Department of Electronics and Communication Engineering, Sri Vasavi Engineering College
West Godavari, Andhra Pradesh, India
Email: drykudara@gmail.com

1. INTRODUCTION

For data acquisition units, the high-speed analog-to-digital converters (ADCs) performance is based on the comparator's efficiency. Dynamic comparators or DC in high-speed ADCs should have low power consumption. Since speed is directly affecting the power, high-speed ADCs consume higher power than slower ADCs. In addition, the clocked regenerative comparators use flip-flop to have strong positive feedback which contributes to additional delay. The other issues or problems faced are due to noise, offset, random decision errors and white noise. In biomedical signal processing systems, a small amount of noise will affect the medical information. Thus, the noise input alters the delay in different clocked comparators. For low power analysis multigate devices can be used which reduces the leakage current during high-speed operation. The leakage current varies for the major operation of comparator namely reset phase and compare phase. Reset phase defines the start condition and the compare phase defines the output. The other issue is the delay. The conventional comparator faces delays due to the discharging of load capacitance and latch regeneration. The next problem is on the structure since rail-to-rail output swing is the main parameter to be considered. The double tail comparator performs in low voltage applications with reduction of kickback

noise when it leads to more power consumption. Thus, power consumption can be reduced by controlling the intermediate transistors on input sides. So as we look into the optimization of the circuit the delay is based on the speed and supply voltage by Vaijayanthi and Vivek [1]. The simulation when performed in 90nm CMOS technology the delay was less but leakage was more. B. Mashhadi and S. Moghaddam [2] analyzed the CMOS comparator delay and operation in small supply voltages. Chiwande and Akarte [3] designed a CMOS based double tail comparator for high-speed device and the effect of power and leakage current is observed. For delta sigma modulation, Pradhan and Bakshi [4] introduced a operational trans-conductance amplifier (OTA) based digital to analog approach combining features of switch capacitor-based return to zero (SCRZ) circuit in inverter-based dynamic latch comparator.

Hence the implementation is carried by 90nm technology with 1.2V supply voltage. Gawhare and Gaikwad [5] presented a new CMOS DC device with maximized speed and reduce power consumption. Gandhi and Devashrayee [6] designed differential double tail dynamic working in 0.9V supply but suffers from current driving capability. Li *et al.* [7] designed regenerative comparator in 0.13-μm CMOS with 1.8× voltage offset reduction. He *et al.* [8] anayzed dynamic comparator for the input range, operating characteristics, static and dynamic offset impacts on stability. The offset voltage expression for dynamic comparator implementation is validated in 40nm and 0.25-mum CMOS technology. An ultra low-voltage non-clocked voltage comparator in standard twin-well 130 nm CMOS is analyzed by Nagy *et al.* [9]. The operating temperature was -20-85 °C with the power supply voltage of 0.6 Chin *et al.* [10] designed a low power comparator working at high frequency with low supply voltage of 1V. This technique overcomes the kickback noise.

Thus, the implementation is done by rail-to-rail SAR ADC for biomedical application in 0.18 μm TSMC CMOS technology. Reduction of power in 65nm based CMOS preamplifier using adaptive power control is done by Lan *et al.* [11]. The simulation consumed 191.2 nW at 15 MHz and 0.8 V supply voltage for 12-bit ADC. Vemu *et al.* [12] discuss the sub threshold leakage of transistors to achieve architecture at 10 ns. Thus, the sub threshold voltage (Vt) leakage of transistors is rectified using the fast comparator in CMOS technology. Lotfi *et al.* [13] performed simulation of fully differential, high speed high swing comparator with operating voltage of 1V. The implemented device is in 0.25-mum CMOS process. The MOSFET based device is done for pipelined A/D converters with higher rail to rail swing. Thus, the result is taken using HSPICE simulations with various input ranges. Connecting a low gain amplifier connected to a latch circuit will improve the driving capability but suffers from high power consumption designed by Hussain *et al.* [14]. This technique also compares the inputs of amplifier during the evaluation period and the outputs are latched during the regeneration time. Chaudhari and Pawar [15] analysed the ADC and comparator performance for different inputs. Senthilkumar *et al.* [16] power and delay of dynamic comparator are cross-coupled inverters which are modified for fast operation and low power consumption. In Kumar *et al.* [17] new devices were designed in literature where the performance of FinFET is found exceptionally good. Guptha *et al.* [18] designed operational transconductance amplifier (OTA) Circuit. In literature several works are carried out for the design of comparators and noise removal [19]-[24].

Below 32 nm, Conventional MOSFET transistor face problems in short channel effects. Hence decreasing the width and length of MOS device will reduce the performance and higher average power consumption. The MOS transistor becomes bulk at the nano-scale due to the fabrication technology of FinFET. This technology compatible with single Gate MOS transistor. The MOSFET is replaced by FinFET due to the fact of fabrication process. The quasi-planner double gate (DG) transistors is the another type of FinFET transistor where the direction of the current is parallel and channel is perpendicular to it. The gate terminal is independently controlled to offer rich design space. The two corresponding electrically coupled gates suppress the short channel effects. In acquisition units, the data converters determine the system performances where the use of MOS logic circuits in VLSI chips ensures the same. But as the dynamic nature of MOS logic suffers from noise occurrence, the control if current may reduce the noise level. Common noises like ground noise, power noise, leakage noise, sharing noise, crosstalk noise, and substrate noise. The issues due to low voltage and noises in the earlier single gate transistor design can be eliminated using the double gate transistor due to the body or fin formed by the conducting channel wrapping by a thin silicon. The average power consumption is minimized under 32 nm technology in FinFET.

2. BACKGROUND METHODOLOGY

In medical and multi media applications data acquisition and event monitoring is done using high speed analog-to-digital converters (ADCs). The ADCs are build using dynamic voltage comparators (DVCs). The inputs of the comparator are from sensor units which are processed for an application may be based on internet of things (IoT). These devices consume low power with a ultra low power supply voltage of 0.6 V. Energy harvested systems cant able to accommodate these low voltage devices. Thus, the design is excluded in digital standard cell-based modules during integration. Some limitations are seen when digital

implementation of analog functions are performed. The fully synthesizable circuit is implemented by CMOS based digital standard cells. This circuit is completely performed under fully synthesizability and very low area. The major issue while performing the DVC is its very narrow common-mode input range (CMR). These limitations can be eliminated by proposed method.

2.1. Prior fully-synthesizable dynamic voltage comparator and limitations

The fully synthesizable DVC with NOR-based input stage. This method has the NAND3-DVC of an input stage comprising two NAND3 gates and an SR latch. The Figure 1 shows the fully synthesizable DVC.

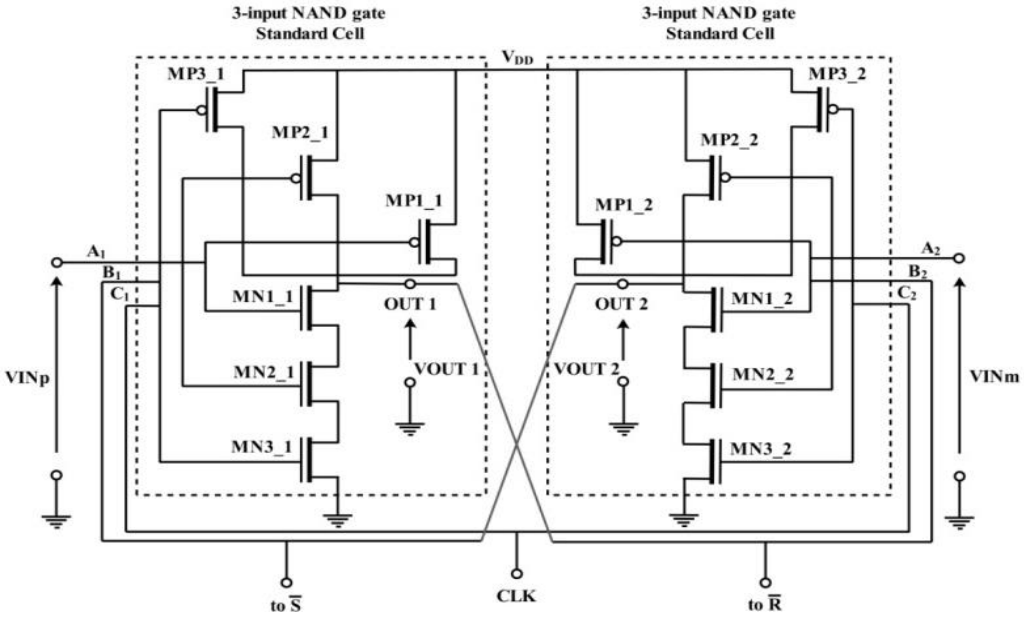

Figure 1. Fully synthesizable DVC

The DVC in Figure 2 during the low-to-high clock transition gets the digital output at the sampling phase. The NOR-based input stage is designed so that during the rising edge, the digital output is available. The polarity is set based on the logical switching and the analog input differential voltage. The driving capacity and logic levels may reduce due to the pulling down of OUT1 and OUT2 in the DVC. The countering of the current in the drains of the transistor MP1_1 and MP1_2 occurs due to the driving by the analog inputs. The voltage of the source-gate MP1_1 and MP1_2 is increased to reduce the common mode input voltage. The OUT1 and OUT2 falling transients are opposed by the current.

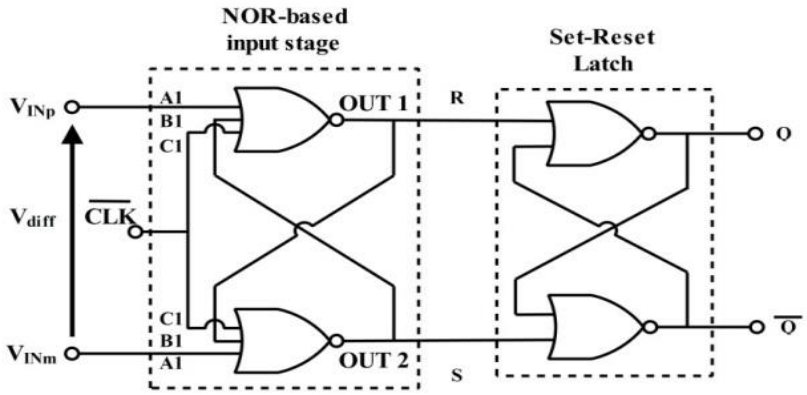

Figure 2. Fully synthesizable DVC with NOR-based input stage

3. PROPOSED FINFET BASED RAIL-TO-RAIL FULLY-SYNTHESIZABLE VOLTAGE COMPARATOR

The issues of CMR in synthesizable DVC is overcomed by proper design using FinFET as shown in Figure 3. The proposed design can work at larger range of input, low leakage and low supply voltage. The rail-to-rail DVC device in Figure 3(a) is redesigned by the NAND gates and NOR gates. The fully synthesizable FinFET DVC is shown in Figure 3(b). The dual circuit operation will lead to the similar way of operation as shown in rail-to-rail CMR. The common mode input voltage ranges between the ground and Vp. The value of Vp is equal to Vdd/2. Out of this range, the comparator output is less determined. The comparator fails to operate out of this range. Merging the NAND and NOR based input will enhance the performance, fully synthesizable and can operate at wider input voltage ranges.

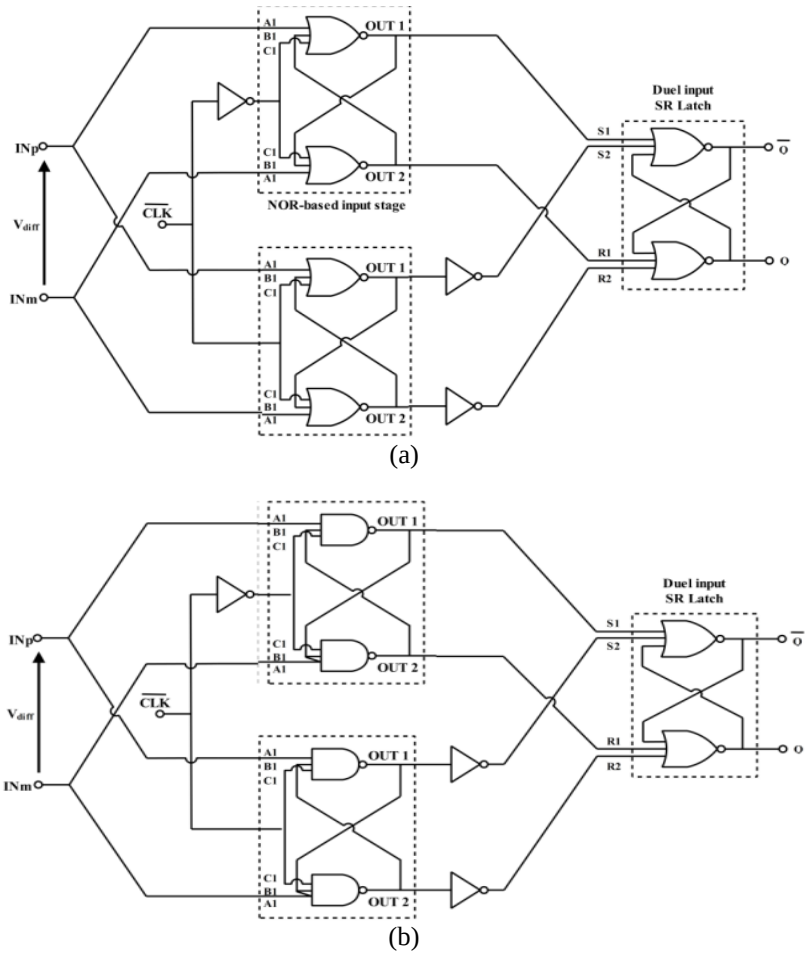

Figure 3. The issues of CMR in synthesizable DVC is overcomed by proper design using FinFET, (a) fully-synthesizable RRDVC of gate-level structure and (b) fully synthesizable structure of FinFET DVC with NAND3-based input stage (NAND3-DVC)

From the results, it has been found that CMOS device is inferior when compared with FinFET implementation of the comparator. SPICE model were used in this work and the software used in the project is Synopsis. The leakage current is more in CMOS devices while in FinFET. Due to the control of multi gates on the channel, the leakage current is reduced. This will improve the power consumption in the FinFET device when compared to CMOS devices. The Proposed comparator circuit implemented by FinFET is fully synthesizable. The pulling down of the output in the comparator is managed by using the FinFET devices. The device is implemented in low power mode. The Performance of the FinFET is similar with that of CMOS devices when connected in shorted gate mode, but the consumption of the power in the device can be reduced only if the device is working in low power mode. The Independent gate mode is preferable in certain applications. The Independent Gate mode needs multiple power supplies which is addition tradeoff.

3.1. FinFET based fully synthesizable DVC with NAND3

Fully synthesizable FinFET DVC with NAND3-based input stage (NAND3-DVC) dynamic voltage comparators implementation was done in ANALOG LTSPICE and synopsis HSPICE (Figure 3(b)). Predictive technology models were used for FinFET and CMOS devices [25]. The Key building blocks of the analog-to-digital converters can have wide range of supply voltage due to the maximum input voltage of the sensor. The reference voltage is chosen according to the sensor input by which the step size changes. The circuit is suitable for flash ADC due to the high speed operation in the range of 1GHz. The supply voltage varies between 0.6 V to 1.2V. The driving capability decreases if the supply voltage reduces. The leakage current also affects the driving strength of the circuit. Thus, the proposed design is custom fashion and digital standard cell-based module is created which forms the part of the ADC integration process. Some limitations are seen when speed above 5GHz is used. The power increases but with a minimum tradeoff. This circuit is completely performed under fully synthesizability and very low area. In FinFET the switching speed is better when compared to CMOS. Hence the common-mode input voltage is reduced by increasing the source-gate voltage of the pull up transistor block of the gates.

4. RESULTS AND DISCUSSION

The parameters of the NAND3-DVC, NOR3-DVC and RRDVC in different region are shown in Tables 1-3. By comparing the performance of the NAND, NOR and RRDVC, the NAND based DVC is very efficient. The proposed work basis of NAND logic is better in performance. The Tables 3 and 4 shows the performance of the proposed method. Figure 4 shows the simulation result of the designed circuit. The simulations results in Tables 1-3 were taken for different supply voltages, and it's been found that the output was at the maximum swing. The FinFET device provides the required swing and good input impedance. predictive technology model (PTM) files for CMOS and FinFET is used [25].

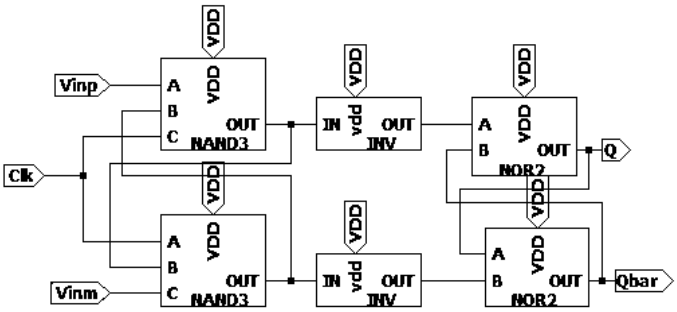

Figure 4. Simulation of fully synthesizable FinFET DVC with NAND3-based input stage (NAND3-DVC)

Table 1. Parameter analysis of NAND3-DVC in different region

S.No	Parameter	NAND3-DVC (Vdd= 0.3v)	NAND3-DVC (Vdd= 0.6v)	NAND3-DVC (Vdd= 0.9v)
1	V_Q	Vavg= 180.05mV	Vavg= 447.41mV	Vavg= 382.7mV
		Vrms=232.35mV	Vrms= 491.31mV	Vrms= 403.91mV
2	V_{Qbar}	Vavg= 119.89mV	Vavg= 140.25mV	Vavg= 438.64mV
		Vrms=189.57mV	Vrms= 239.62mV	Vrms= 465.38mV
3	At Q	P= 24.865pW	P= 129.32nW	P= 1.3268µW
		E= 248.65pJ	E= 1.2932µJ	E= 13.268µJ
4	At Q_{bar}	P= 11.983pW	P= 152.02nW	P= 1.5369µW
		E= 119.83pJ	E= 1.5202µJ	E= 15.369µJ

Table 2. Parameter analysis of NOR3-DVC in different region

S.No	Parameter	NOR3-DVC (Vdd= 0.3v)	NOR3-DVC (Vdd= 0.6v)	NOR3-DVC (Vdd= 0.9v)
1	V_Q	Vavg= 279.24mV	Vavg= 558.46mV	Vavg= 837.67mV
		Vrms= 282.29mV	Vrms= 564.57mV	Vrms= 846.84mV
2	V_{Qbar}	Vavg= 3.1368mV	Vavg= 6.2816mV	Vavg= 9.4318mV
		Vrms=6.9962mV	Vrms= 14.004mV	Vrms= 21.022mV
3	At Q	P= 10.266nW	P= 82.126nW	P= 277.18nW
		E= 102.66nJ	E= 821.26nJ	E= 2.7718µJ
4	At Q_{bar}	P=5.8393nW	P= 46.745nW	P= 157.84nW
		E= 58.393nJ	E= 467.45nJ	E= 1.5784µJ

Table 3. Parameter analysis of RRDVC in different region

S.No	Parameter	RRDVC (Vdd= 0.3v)	RRDVC (Vdd= 0.6v)	RRDVC (Vdd= 0.9v)
1	V_Q	Vavg= 118.57mV	Vavg= 201.86mV	Vavg= 343.13mV
		Vrms= 158.96mV	Vrms= 220.71mV	Vrms= 362.88mV
2	V_{Qbar}	Vavg= 137.28mV	Vavg= 245.15mV	Vavg= 353.13mV
		Vrms= 179.03mV	Vrms= 275.28mV	Vrms= 409.1mV
3	At Q	P= 23.911nW	P= 339.23nW	P= 1.1534µW
		E= 239.11nJ	E= 3.3923µJ	E= 11.534µJ
4	At Q_{bar}	P= 26.215nW	P= 384.98nW	P= 1.2748µW
		E= 262.15nJ	E= 3.8498µJ	E= 12.748µJ

Table 4. Parameter analysis of NAND3-DVC) in different region using FinFET

S.No	Parameter	NAND3-DVC (Vdd= 0.3v)	NAND3-DVC (Vdd= 0.6v)	NAND3-DVC (Vdd= 0.9v)
1	V_Q	Vavg= 299.98mV	Vavg= 599.96mV	Vavg= 539.96mV
		Vrms= 299.98mV	Vrms= 599.96mV	Vrms= 697.09mV
2	V_{Qbar}	Vavg= 13.225µV	Vavg= -3.7889µV	Vavg= 359.97mV
		Vrms= 202.52µV	Vrms= 129.06µV	Vrms= 569.17mV
3	At Q	P= -113.34nW	P= 111.26nW	P= -260.96nW
		E= -1.1334µJ	E= 1.1126µJ	E= -2.6096µJ
4	At Q_{bar}	P= -196.12pW	P= -98.992pW	P= 19.158nW
		E= -1.9612nJ	E= -989.92pJ	E= 191.58nJ

Figures 5-7 shows the comparison of parameters like power and energy for NAND-DVC, NOR-DVC and RRDVC in different region. The supply voltage is varied to observe the performance of the circuits. The simulations are performed as shown in Figure 8 and the results shows that the comparator has better output swing which is the most important parameter.

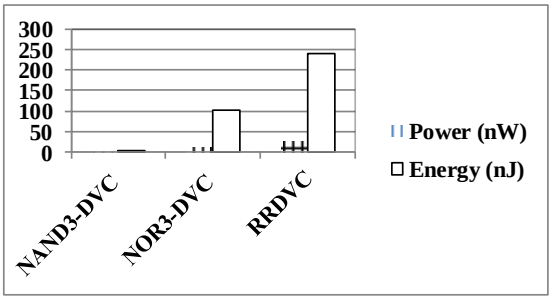

Figure 5. Power and energy comparison of NAND3-DVC, NOR-DVC and RRDVC in different region at Vdd=0.3v

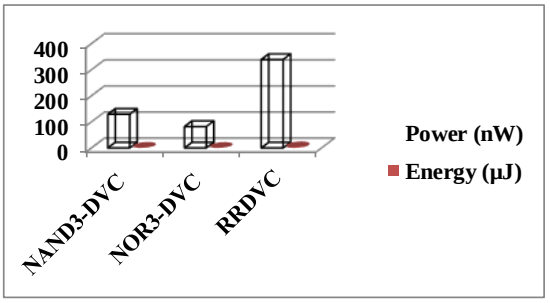

Figure 6. Power and energy comparison of NAND3-DVC, NOR-DVC and RRDVC in different region at Vdd=0.6v

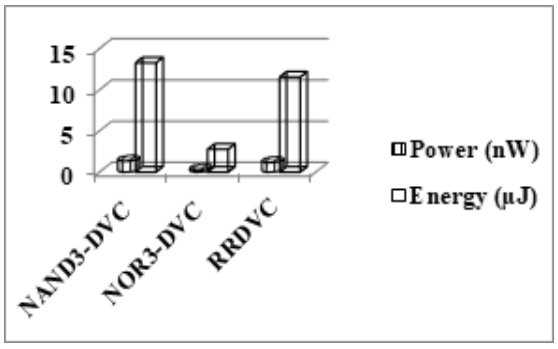

Figure 7. Power and energy comparison of NAND-DVC, NOR-DVC and RRDVC in different region at Vdd=0.9v

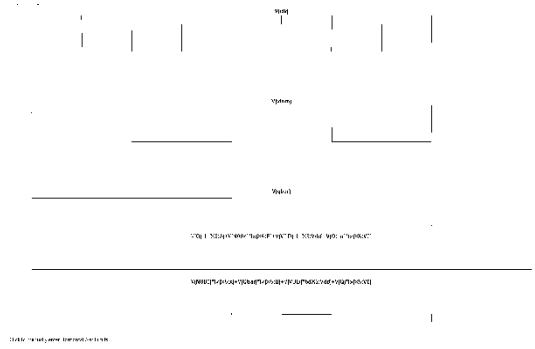

Figure 8. Simulation waveform of fully synthesizable DVC with NAND3-based input stage (NAND3-DVC) in sub-thershold region (Vdd= 0.9v) using FinFET

5. CONCLUSION

The design of comparator is more important for circuits when the input is a low amplitude signal. The ADCs use comparators at the input stage for the conversion process. The data convertors use circuits which are faster and consume less power. Such kind of design is addressed in this paper. A FinFET based fully synthesizable, rail-to-rail DVC is designed and implemented in this work. The rail-to-rail CMR for supply voltages down to 0.3 V is investigated for the CMOS and FinFET using PTM. But the performance of proposed design with FinFET device dominates in performance and the leakage current is reduced. The power consumption is improved. In future ADC SoC chip will be implemented using the proposed DVC.

REFERENCES

[1] M. Vaijayanthi and K. Vivek, "Analysis of dynamic comparators in ultra-low supply voltages for high speed ADCs," in *proc. International Innovations in Information, Embedded and Communication Systems (ICIIECS)*, 2015, pp. 1–6, doi: 10.1109/ICIIECS.2015.7193107.

[2] S. B. Mashhadi and M. S. Moghaddam, "Analysis and design of dynamic comparators in ultra-low supply voltages," in *proc* 2014 22nd *Iranian Conference on Electrical Engineering (ICEE)*, 2014, pp. 255-258.

[3] S. Chiwande and S. P. Akarte, "Performance analysis of low voltage, low power dynamic double tail comparator for data convertor application," in *proc 2016 World Conference on Futuristic Trends in Research and Innovation for Social Welfare (Startup Conclave)*, 2016, pp. 1-4, doi: 10.1109/STARTUP.2016.7583918.

[4] T. Pradhan and A. Bakshi, "Design of a low-voltage low power dynamic latch comparator for a 1.2-V 0.4-mW CT delta sigma modulator with 41-dBm SNDR," in *proc. 2017 International Conference on Trends in Electronics and Informatics (ICEI)*, 2017, pp. 815–820, doi: 10.1109/ICOEI.2017.8300817.

[5] S. B. Gawhare and A. Gaikwad, "Area and power efficient high speed voltage comparator," in *proc 2016 International Conference on Automatic Control and Dynamic Optimization Techniques (ICACDOT)*, 2016, pp. 198-201, doi: 10.1109/ICACDOT.2016.7877578.

[6] P. P. Gandhi and N. M. Devashrayee, "Differential double tail dynamic CMOS voltage comparator," in *proc. 2017 International Conference on Intelligent Communication and Computational Techniques (ICCT)*, 2017, pp. 8-11, doi: 10.1109/INTELCCT.2017.8324011.

[7] Y. Li, W. Mao, Z. Zhang, and Y. Lian, "An ultra-low voltage comparator with improved comparison time and reduced offset voltage," in *proc. 2014 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*, 2014, pp. 407-410, doi: 10.1109/APCCAS.2014.7032806.

[8] J. He, S. Zhan, D. Chen, and R. L. Geiger, "Analyses of static and dynamic random offset voltages in dynamic comparators," in *proc. IEEE Trans. on Circuits Systems I: Regular Papers*, vol. 56, no. 5, pp. 911-919, May 2009, doi: 10.1109/TCSI.2009.2015207.

[9] L. Nagy, D. Arbet, M. Kovac, M. Potocny, and V. Stopjakova, "Design and performance analysis of ultra-low voltage rail-to-rail comparator in 130 nm CMOS technology," in *proc 2018 IEEE 21st International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS)*, 2018, pp. 51-54, doi: 10.1109/DDECS.2018.00016.

[10] S. Chin, C. Hsieh, C. Chiu, and H. Tsai, "A new rail-to-rail comparator with adaptive power control for low power SAR ADCs in biomedical application," in proc. *2010 IEEE International Symposium on Circuits and Systems*, pp. 1575-1578, 2010, doi: 10.1109/ISCAS.2010.5537421.

[11] S. Lan, C. Yuan, Yvonne, Y. H. Lam, and L. Siek, "An ultra low-power rail-to-rail comparator for ADC designs," *in 2011 IEEE 54th International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2011, pp. 1-4, doi: 10.1109/MWSCAS.2011.6026511.

[12] S. R. Vemu, P. S. S. N. Mowlika, and S. Adinarayana, "An energy efficient and high speed double tail comparator using cadence EDA tools," in *proc. 2017 International Conference on Algorithms, Methodology, Models and Applications in Emerging Technologies (ICAMMAET)*, 2017, pp. 1-5, doi: 10.1109/ICAMMAET.2017.8186675.

[13] R. Lotfi, M. T. Sani, M. Y. Azizi, and O. Shoaei, "A 1-V MOSFET-only fully-differential dynamic comparator for use in low-voltage pipelined A/D converters," in *proc.* Signals, *Circuits and Systems, 2003. SCS 2003. International Symposium on*, vol. 2, pp. 377-380, 2003, doi: 10.1109/SCS.2003.1227068.

[14] S. Hussain, R. Kumar, and G. Trivedi, "Comparison and design of dynamic comparator in 180nm SCL technology for low power and high speed flash ADC," in *proc. 2017 IEEE International Symposium on Nanoelectronic and Information Systems (iNIS)*, pp. 139-144, 2017, doi: 10.1109/iNIS.2017.37.

[15] S. Chaudhari and M. Pawar, "Design of efficient double tail comparator for low power," in *proc. 2015 International Conference on Communications and Signal Processing (ICCSP)*, 2015, pp. 1782-1785, doi:10.1109/ICCSP.2015.7322829.

[16] V. M. Senthilkumar, S. Ravindrakumar, D. Nithya, and N. V. Kousik, "A vedic mathematics based processor core for discrete wavelet transform using FinFET and CNTFET technology for biomedical signal processing," *Microprocess Microsyst*, vol. 71, pp. 102875, 2019, doi: 10.1016/j.micpro.2019.102875.

[17] V. M. S. Kumar, C. Rathnakar, M. A. Guptha, and R. Selvaraj, "A hybrid full adder design using multigate devices based on XOR/XNOR logic," In *Intelligent System Design. Advances in Intelligent Systems and Computing*, pp. 229-236, 2021, doi: 10.1007/978-981-15-5400-123.

[18] M. A. Guptha, V. M. S. Kumar, T. H. Prasad, and R. Selvaraj, "Low power, less leakage operational transconductance amplifier (OTA) circuit using FinFET," In *Intelligent System Design. Advances in Intelligent Systems and Computing*, pp. 191-199, Springer, Singapore, 2021, doi: 10.1007/978-981-15-5400-1_19.

[19] Z. Zhu, Z. Qiu, Y. Shen, and Y. Yang, "A 2.67 fJ/c.-s. 27.8 kS/s 0.35 V 10-bit successive approximation register analogue-to-digital converter in 65 nm complementary metal oxide semiconductor," *IET Circuits Devices Syst.*, vol. 8, no. 6, pp. 427-434, 2014.

[20] Y. Xu, L. Belostotski, and J. W. Haslett, "A 65-nm CMOS 10-GS/s 4-bit background-calibrated noninterleaved flash ADC for radio astronomy," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 22, no. 11, pp. 2316-2325, 2014.

[21] Y. Nakajima, N. Kato, A. Sakaguchi, T. Ohkido, and T. Miki, "A 7-bit, 1.4 GS/s ADC with offset drift suppression techniques for one-time calibration," *IEEE Trans. Circuits Syst. I: Regul. Pap.*, vol. 60, no. 8, pp. 1979-1990, 2013.

[22] M. Nema and R. Thakur, "Design of low-offset voltage dynamic latched comparator," *IOSR J. Comput. Eng.* vol. 2, no. 4, pp. 585-590, 2012.
[23] J. Lu and J. Holleman, "A low power high precision comparator with time domain bulk tuned offset cancellation," *IEEE Trans. Circuits Syst. I: Regul. Pap*, vol. 60, no. 5, pp. 1158-1167, 2013.
[24] J. Gao, G. Li and Q. Li, "High-speed low-power common-mode insensitive dynamic comparator," *Electron. Lett*, vol. 51, no. 2, pp. 134-136, 2015.
[25] S. Sinha, G. Yeric, V. Chandra, B. Cline, and Y. Cao, "Exploring sub-20nm FinFET design with predictive technology models," In *Proc. 49th Annual Design Automation Conference (DAC '12)*, 2012, pp. 283-288, doi: 10.1145/2228360.2228414.

BIOGRAPHIES OF AUTHORS

Dr. Udara Yedukondalu was born in Karempudi, A.P, India, in 1977. He received B.Tech degree in Electronics and Communication Engineering from Nagarjuna University, Guntur, A.P, India, in 2001, M.Tech, degree in Instrumentation & Control Systems from University College of Engineering, JNTU Kakinada, A.P, India in 2007 and Ph.D. degree from the Acharya Nagarjuna University, Guntur, A.P, India in 2017. He is having 20 years of experience and published 25+ journals, five patents and also one copyright. He is currently working as an Associate Professor, Department of Electronics and Communication Engineering, Sri Vasavi Engineering College (A), Tadepalligudem-534101, A.P, India. His research main interest aims at VLSI design, Nano-electronics, Analog and Digital Integrated Circuits and Oscillators. He can be contacted at email: drykudara@gmail.com.

Vinod Arunachalam is Assistant Professor in the department of Electronics and Communication Engineering, Government College of Engineering, Dharmapuri. He holds Master of Engineering with specialization in VLSI DESIGN at Anna University of Technology Coimbatore. He is currently pursuing PhD in Anna University Chennai. His research areas are Biomedical image analysis, VLSI DESIGN and Image/Signal Processing. He is a member of ISTE. He published many paper in reputed journals. He can be contacted at email: vinodnash@gmail.com.

Dr. Vasudha Vijayasri Bolisetty was born in Eluru, A.P, India, in 1982. She received B. Tech degree in Electronics and Communication Engineering from JNTU, Hyderabad, A.P, India, in 2003, M.E, degree in Communication Systems from Andhra University, A.P, India in 2009 and Ph.D. degree from the JNTUK, Kakinada, A.P, India in 2020. She is having 19 years of experience and published 20+ journals and three patents. She is currently working as an Associate Professor, Department of Electronics and Communication Engineering, Aditya College of Engineering & Technology, Surampalem-533437, A.P, India. Her research main interest aims at Speech Processing, Signal Processing and Communications. She can be contacted at email: vasudha.tweety@gmail.com.

Dr. Ravikumar Guru Samy is Head of the Department of Electronics and Communication Engineering, M.P.Nachimuthu M. Jaganathan Engineering College, Chennimalai, Erode, Tamilnadu, India He awarded his Ph.D from Anna University, Chennai in the area of Medical Image Processing in the year 2019. His area of interest is Digital Image Processing, VLSI Design, Digital Signal Processing, Internet of Things and Computer Networks. He has more than thirty four years of experience in teaching and he has published papers in reputed International and National Journals. Area of interest VLSI, Image and signal processing. He can be contacted at email: ravikumarg66@gmail.com.