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A 1 V -21 dBm threshold voltage compensated rectifier for radio frequency energy harvesting

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ABSTRACT

Due to the limitations of battery life and capacity, power supply has been the bottleneck for scaling of a wireless sensor network in thousands or millions of nodes. Radio frequency energy harvester (RFEH) is a promising solution to power up sensors and wireless devices due to increasing accessibility of RF energy sources, better silicon integration of the harvester circuit and compatibility with wireless networks. One of the significant limitations of RF energy harvester is low power efficiency rectifier where the main function of the micropower rectifier is to convert radio frequency (RF) energy into direct current (DC) energy. To achieve higher power conversion energy (PCE), this paper presents a five-stage charge pump rectifier, with implementation of diode-connected metal-oxide-semiconductor (MOS) transistors and an auxiliary circuit to produce compensation voltage to the charge pump to achieve higher efficiency over a wide input range. This work is designed and implemented using 130 nm complementary metal-oxide-semiconductor (CMOS) technology and achieved a wide input power range of 15 dBm with efficiency higher than 20%; and at -21 dBm sensitivity for 1 V output is achieved while driving 1 MΩ load at 920 MHz.

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1. INTRODUCTION

The fast-growing use of radio-frequency identification (RFID) and wireless sensor networks (WSNs) brings a lot of demand to develop high-performance power supply generation for these types of applications [1], [2]. Also, due to the high usage of portable devices, availability of the electromagnetic field density is increasing, and it could provide an excellent energy source to radio frequency (RF) energy harvester. Radio frequency energy harvesting (RFEH) technique has more advantages compared to batteries, for example it has an unlimited lifetime, and it can operate at any time as long as a minimum RF power is available [3]-[5]. Additional benefits of the RFEH system is the possibility of combining it with solar energy harvesting or any other harvesting technologies [6], [7] to improve its power conversion energy (PCE) in the energy harvest system.

RF power transfer can be divided into two categories, near field which is also known as wireless power transfer (WPT), and far-field [8]. The near field works with higher power density at lower frequency [9] and; mostly used in wireless battery charging [10] and biomedical applications [8]. In far-field, the transmission distance is far and the power received by the antenna can be predicted using Friis transmission expression [11]. The general issues of the RFEH system are the limited power that can be received by a

rectenna [12] and low PCE at low input power [13], [14]. Apart from those, matching network losses [15] and reflection losses in the impedance matching network [16] also influence the overall PCE of a RFEH system. As the RF energy is not constant in the ambient due to distances, it is also crucial to design a RFEH system that can operate efficiently in a wide range of input power [17]. A micropower rectifier plays an important role in the RFEH system. The performance of the rectifier depends on the threshold voltage in the forward bias region and its leakage current in the reverse bias region [1], [18]. The implementation of RFEH system is characterized by sensitivity and power conversion efficiency (PCE) parameters that strongly dependent on leakage current and threshold voltage of the diode-connected transistors [17].

Dickson charge pumps are widely used in RF energy harvesting devices due to their coalition capabilities and compared to the Cockcroft-Walton rectifier, the Dickson rectifier has a relatively large storage capacity and higher power conversion energy (PCE) [19]. However, increasing the number of stages of this type of rectifier does not necessarily increase the output efficiency [20] and the performance of Dickson rectifiers is strongly dependent on the threshold voltage, V_{th} of the semiconductors [21]. Earlier researchers have proposed several solutions to improve its efficiency at low input power, by presenting different circuit techniques for example, Yaou *et al*. [18], the authors utilize transistors with zero threshold voltage while [22] uses the Schottky diodes to achieve a higher sensitivity value. However, the issue with these methods is the need to have a particular device specification to achieve the lowest threshold voltage, which raises the cost of the chip fabrication [1].

Modified charge pumps are another circuit design; that are widely used as RF rectifier [19] as it has high capability to enhance and rectify signal amplitudes by utilizing a stack of diode-connected transistors as rectifying devices. Several techniques have been proposed to achieve the high-efficiency rectifier by proposing new diode-connected configuration or varying the gate-source voltages known as compensation voltage which can be achieved by implementing an auxiliary circuit. For example, in Nakamoto *et al*. [23] and Li *et al*. [24], authors proposed passive auxiliary circuits to provide compensation voltage, however the main limitation of their design in multi-stage implementation, is the area consumption. This is due to large capacitance and resistance values are used, and it suffers from high parasitic capacitance and leakage current. On the other hand, in Papotto *et al*. [11] and Hameed and Moez [25], authors proposed active auxiliary circuits by connecting the gate terminals to the nodes in chain that produce higher overdrive voltage. However, these techniques suffer inversion loss and high leakage current during the reverse biased operation. Hameed and Moez [26] an adaptive connection is proposed to reduce the leakage current and inversion loss. The main degradation of these techniques is that the compensation voltage cannot be adjusted and highly depends on input power. As the gate terminals are connected to particular nodes of chain, therefore they are regularly failed to deliver a high PCE over a wide input power range.

In this paper, we propose RF rectifier using modified Dickson charge pump with an auxiliary circuit to provide threshold voltage compensation to the rectifier to deliver PCE higher than 20% over a wide input power range using 130 nm CMOS process. The paper is arranged as shown in; Section 2 details out the reverse bulk diode connection transistor to minimize the leakage current in the reverse bias region; Section 3, details out the optimization of compensation voltage and in section 4, explains the proposed rectifier structure; section 5, the experimental results, and the discussion and finally section 6, the conclusion of the design.

2. PROPOSED REVERSE DIODE CONNECTED TRANSISTORS

A diode connected p-channel metal-oxide semiconductor (PMOS) or n-channel metal-oxide semiconductor (NMOS) transistor is the central part of most CMOS rectifiers [14]. Figure 1 represents different types of diode connected transistor. Figure 1(a) demonstrates that by connecting the bulk to the source terminals and gate to the drain terminals, the transistor will act as a diode [1]. In this conventional diode, the voltage difference between the source and bulk is zero, $V_{SB} = 0$. According to (1), the threshold voltage V_{th} will be reduced to the intrinsic threshold voltage V_{tho}. However, (2) shows, reduction of V_{th} will increase the leakage current exponentially, which will drop the overall efficiency of the CMOS rectifier design. Direct implementation of conventional diode in rectifier circuit has shown good performance in the subthreshold and forward bias regions; however, its efficiency dramatically drops in the reverse bias region due to high leakage current [27].

$$V_{th} = V_{tho} + k_1\left(\sqrt{\varphi_s + V_{SB}} - \sqrt{\varphi_s}\right) + k_2 V_{SB} \quad (1)$$

Where φ_s is the surface potential, k_1 and k_2 are dependent on channel doping.

$$I_{leakage} \approx 2n\mu C_{ox}\left(\frac{W}{L}\right)\left(\frac{kT}{q}\right)^2 \exp\left(\frac{|V_{GS}|-V_{th}}{\frac{nkT}{q}}\right) \quad (2)$$

Where *k* is the Boltzmann constant, μ is the effective mobility, n is the subthreshold slope factor.

To increase efficiency of the rectifier, threshold voltage in forward-bias region and leakage current in reverse-bias region should be minimized in the rectifier [1]. This can be achieved by connecting the bulk to its drain terminals as shown in Figure 1(b). With this connection, when the proposed diode connected NMOS is in the forward operating region, then $V_S < V_B$ therefore $V_{SB} < 0$, according to (1) the V_{th} will be lower than the conventional diode. In reverse bias region, the $V_S > V_B$ therefore $V_{SB} > 0$, which increases the threshold voltage. As previously discussed in (2), higher V_{th} will reduce the leakage current. This diode connection will be used in the design of the rectifier in this paper.

(a) (b)

Figure 1. Diode connected transistor (a) conventional diode and (b) proposed diode connected

3. OPTIMIZATION OF THE COMPENSATION VOLTAGE

Compensation voltage is applied between the gate and source terminals of a transistor to reduce its threshold voltage and ultimately enhance the RFEH performance. Figure 2 shows a single-stage charge pump with an ideal direct current (DC) voltage source that acts as a compensation voltage. At low input power, the transistor will be in the subthreshold region [17] and the input power and output voltage can be expressed as in (3) and (4) [28].

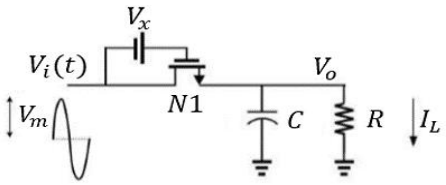


Figure 2. Single stage charge pump

$$V_O = nV_T \ln\left(\frac{\frac{J_0\left(\frac{V_m}{nV_T}\right)}{I_L}}{\left(C_{ox}\mu_{eff}(n-1)V_T^2 \exp\left(\frac{V_x-V_{th}}{nV_T}\right)\frac{W}{L}\right)}+1\right) \quad (3)$$

$$P_{in} = V_m\left(C_{ox}\mu_{eff}(n-1)V_T^2 \exp\left(\frac{V_x-V_{th}}{nV_T}\right)\frac{W}{L} + I_L\right)\left(\frac{J_1\left(\frac{V_m}{nV_T}\right)}{J_0\left(\frac{V_m}{nV_T}\right)}\right) \quad (4)$$

According to (3), by increasing the value of V_x for a fixed load, increment in the output voltage can be obtained however, in (4) it shown that it also increases the input power P_{in}.

$$PCE = \frac{\left(\frac{V_O^2}{R_L}\right)}{P_{in}} \quad (5)$$

Therefore, increasing the V_x value does not necessarily increase the PCE and it is essential to obtain the optimum value of V_x to achieve the peak PCE. This can be obtained by finding the root of ∂PCE/∂Vx=0 and thus the maximum compensation voltage can be expressed as (6) [17].

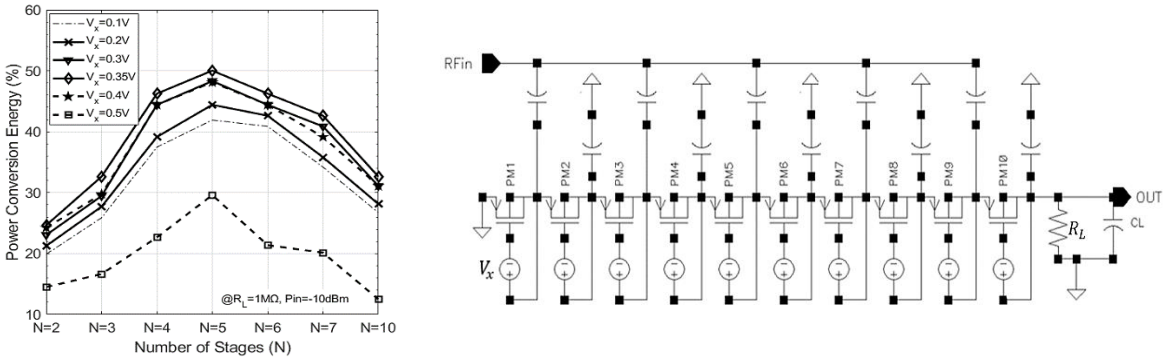
$$V_{x_{max}} = nV_T \ln\left(\frac{nV_T \exp\left(\frac{V_{th}}{nV_T}\right)}{C_{ox}\mu_{eff}(n-1)V_T^2 \exp\left(-\frac{V_{th}}{nV_T}\right)\frac{W}{L}R_L}\right) \quad (6)$$

According to (6) illustrates that the maximum compensation voltage is in the function of the output load R_L, transistor size *(W/L)*, and transistor characteristics such as V_{th}.

4. PROPOSED CHARGE PUMP RECTIFIER

The charge pump with optimal compensating voltage and the number of stages optimised is seen in Figure 3. Figure 3(a) shows the 5-stage charge pump with 10 constant DC sources, V_x as compensation voltage. PMOS diode connected transistor has lower leakage current compared to the NMOS therefore the PMOS charge pump is being used, with aid of ideal compensation for each PMOS, the relationship between the transistor sizing, optimal compensation voltage, and the number of stages to achieve a wide range of input power to gain the PCE above 20% will be investigated. Earlier, it is shown in (6) that the optimum compensation voltage is also dependent on the output load, R_L and in this work, the load is set to be 1 MΩ.

Figure 3(b) shows the comparison result of the PCE between charge pumps with different compensation voltage values and the number of stages where the P_{in} is set to -10 dBm and frequency at 920 MHz. The result shows that the 5-stage charge pump with ideal compensation voltage ranging from 0.3 V to 0.4 V achieves the highest efficiency among the other combinations. Figure 4 shows the compensating voltage and tranistors' size justification. Figure 4(a) also shows that the PCE varies non-linearly with the applied compensation voltage value where it can be seen that the PCE value dropped after achieving 0.35 V of V_x.



(a) (b)

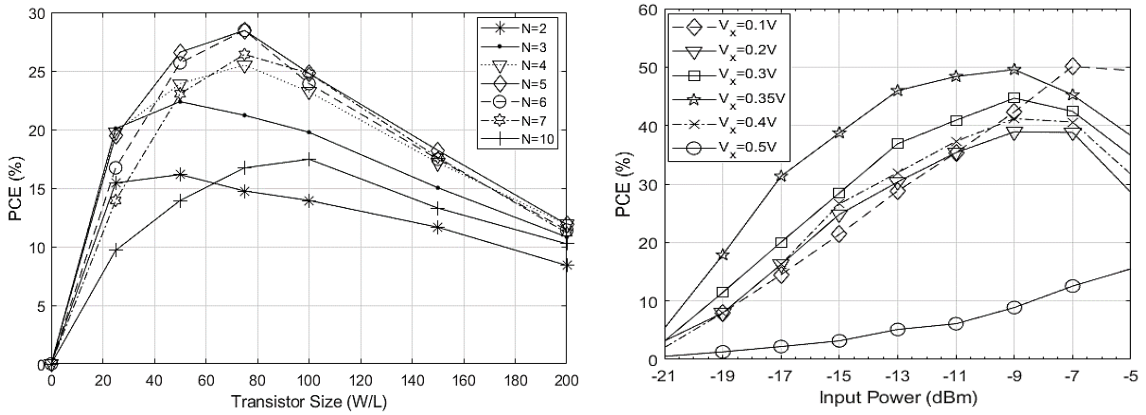
Figure 3. Charge pump (a) optimization of the number of stages and (b) schematic

Next, the transistor size and the number of stages are varied while the ideal compensation voltage is set to 0.35 V, input power to -15 dBm, and frequency at 920 MHz. Figure 4(b) shows that increasing the number of stages does not necessarily improve efficiency. The 5-stage charge pump with transistors' size of *W/L* of 78 shows the highest efficiency compared to the others. Next, an auxiliary circuit will be designed using the proposed diode-connected transistors and it will replace the ideal voltage source for the compensation voltage (V_x) from the previous section to obtain the approximate value of the compensation voltage without the needs for an external DC source. Figure 5 shows the proposed enhanced rectifier circuit where all the bulk terminals are connected to the drain terminals. Transistors M_1 to M_{10} and coupling capacitors C_1 to C_9 form the main charge pump chain. In order to reduce the ON resistance of the transistor, the V_{sg} of all PMOS in the charge pump are connected to the lower potential voltage than the drain voltage.

The lower potential voltage for every single gate in the main charge pump chain is generated by an auxiliary circuit which is a voltage divider circuit. The pack of diode-connected NMOS transistors N_{A1-7}, N_{B1-11}, N_{C1-11}, N_{D1-13} , N_{E1-13} , N_{F1-15} and N_{G1-15} which form the high impedance paths for the auxiliary circuits act as voltage dividers delivering the compensation voltage to the main chain

transistors' gates of M_{1-9}. Sizing of the PMOS, P_{0-6} are needed in order to achieve the optimized compensation voltage value, which is approximately about 0.3 to 0.4V that previously measured. The size of all NMOS in the high impedance tail should have the smallest width in order to reduce leakage current to the ground. For the gates of $M_2, M_4, M_6$and M_8, their drain terminals are connected to the drain terminals of $P_0, P_2, P_4\ and\ P_6$ respectively which is part of the auxiliary circuits that produce the compensation voltage value.

In order to suppress high-frequency noise at the gate of M_2, M_4, M_6 and M_8 the bypass capacitors of CB_{1-4} are connected to the gates respectively. The drain voltage of M_3, M_5 and M_7 which are alternating provide the compensation voltage to their gates. The DC levels of the discharge voltages M_3, M_5 and M_7 are transferred to lower potential voltages without reducing their alternating current (AC) coefficient by adjusting the small DC block capacitors CD_1 , CD_2 and CD_3, respectively which disable the AC components to charged DC drains of P_1, P_3 and P_5, respectively. The final stage of the proposed rectifier M_9 and M_{10} are uncompensated in order to reduce the leakage current, and the number of auxiliary transistors. As the input power is not sufficient to power up the auxiliary voltage divider in the first stage the first transistor is replaced by an NMOS, $M_1$and its gate terminal is linked to the higher potential voltage than the drain terminal that is connected to the ground. The drain terminal of the N_{A7} will provide the compensation voltage for M_1.



(a) (b)

Figure 4. Optimization of (a) the size of transistors and (b) the compensation voltage.

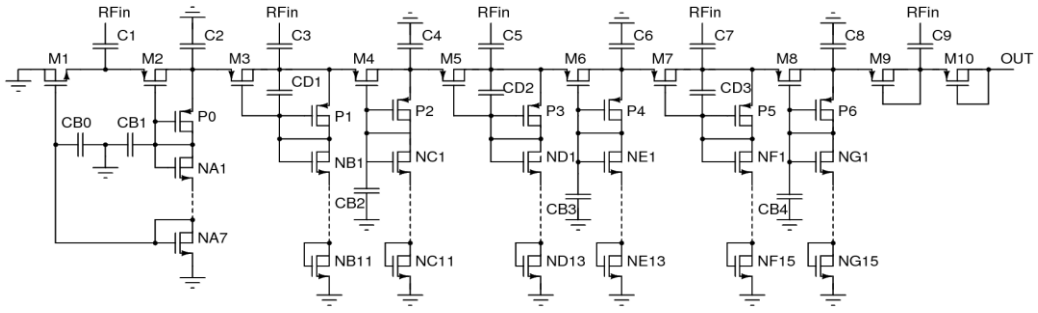
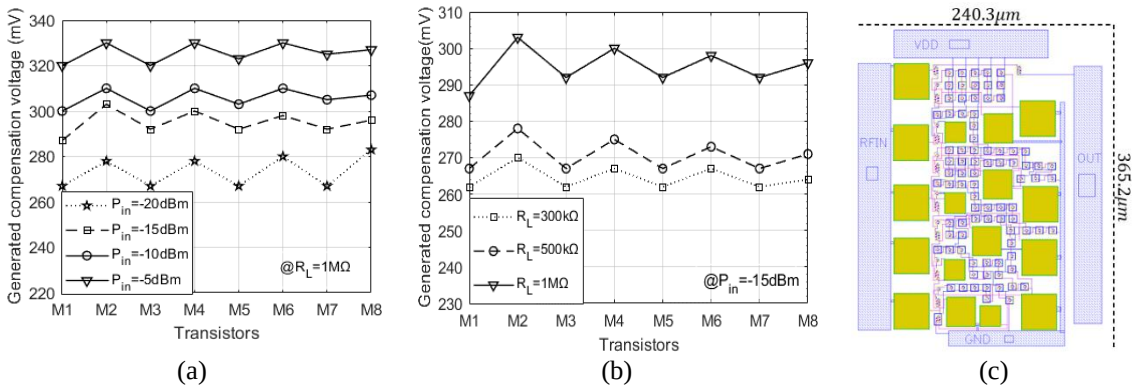


Figure 5. The proposed rectifier circuits

5. SIMULATION AND ANALYSIS OF THE PROPOSED RECTIFIER

This work is designed in standard $0.13\mu m$ CMOS technology with eight layers of metallization and simulated using Cadence. The simulation is performed by using a L-type matching network, at the frequency of 920 MHz. The transistor size of the main path, NMOS (M_1) and PMOS (M_{2-10}) are set to $8\ \mu m/0.13\ \mu m$ and $10\ \mu m/0.13\ \mu m$ respectively and the stack of diode-connected NMOS transistors N_{A1-G15} and voltage driver transistors PMOS (P_{0-6}) are set to $1\ \mu m/0.5\ \mu m$. The coupling capacitors C_{1-9} and bypass capacitors of CB_{1-4} and CD_{1-3} are set to 3pF, 2pF and 1pF, respectively.

Figure 6 depicts the design layout as well as the resulting compensation. Figures 6(a) shows the generated compensation voltage at each transistor in main path of charge pump when taking 1 MΩ load. The average generated compensation voltages at, -5 dBm, -10 dBm, -15 dBm, and -20 dBm input powers are 325.6 mV, 305.6 mV, 295 mV, and 273.4 mV. As the input power level increases from -20 to -5 dBm at 1 MΩ load, the compensation voltage barely varies by 52.2 mV. Figure 6(b) shows the generated compensation voltage for different loads while the input power is set to -15 dBm. The average generated compensation voltage for 1 MΩ, 500 kΩ, and 300 kΩ are 295 mV, 270.6 mV, and 264.5 mV. As the load raises from 300 kΩ to 1 MΩ at -15 dBm, the compensation voltage barely varies by 30.5 mV, which means that when the proposed rectifier is connected to a variety of loads or input power, a nearly consistent compensating voltage is created, which is almost in the optimum compensation voltage range (0.3 V to 0.4 V). Figure 6(c) shows the layout of the proposed rectifier with an area of 0.087 mm^2.



(a) (b) (c)

Figure 6. Generated compensation voltage (a) input powers, (b) loads, and (c) layout of proposed rectifier circuit

Simulation is carried out with input power ranging from -23 dBm to 0 dBm using three different loads, 1 $M\Omega$, 500 KΩ and 300 KΩ. During the simulation, the transistor breakdown voltage is monitored not to exceed 10 V and in order to avoid latch up from occurring especially at the final stages of the charge pump, the V_{sb} is monitored to be lower than 0.5 V, which is the threshold voltage, V_{th} of the transistor. Although the input power of 0 dBm is difficult to achieve in real application, circuit block to cap the maximum bulk voltage may need to be developed but it is not the focus of the current work.

Post-layout simulation results for the proposed rectifier are shown in Figure 7. The output voltage of the proposed rectifer is shown in Figure 7(a) for various loads. This work for 1 MΩ, 500 kΩ, and 300 kΩ loads is simulated up to -5 dBm, -2 dBm, and 0 dBm input power, respectively, to assure transistor and capacitor durability and voltage breakdown (10 V). The 1 V sensitivity of this work are -21 dBm, -18 dBm, and -16 dBm for 1 MΩ, 500 kΩ, and 300 kΩ loads, respectively.

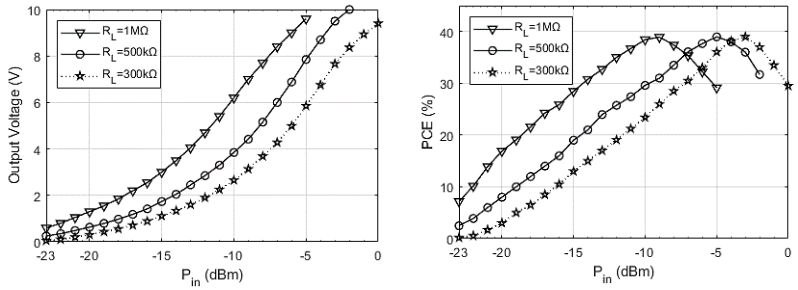
Figure 7(b) represents the efficiency of the proposed rectifier where the maximum efficiency of 39.9%, 38.97%, and 38.5% can be achieved at -9 dBm, -5 dBm, and -3 dBm for 1 $M\Omega$, 500 KΩ and 300 KΩ loads, respectively. In general, we can observe from the graph that using higher load will result in shifting the peak efficiency to the lower input power. The PCE with above 20% for 1 $M\Omega$, 500 KΩ, and 300 KΩ ranging about 15 dBm (-19 dBm to -5 dBm), 14 dBm (-15 dBm to -2 dBm), and 12 dBm (-11 dBm to 0 dBm) respectively. The efficiency of 1 $M\Omega$, 500 KΩ, and 300 KΩ at the sensitivity voltage level of 1 V are 13.9%, 13.5%, and 13%.

Table 1 reviews the performance comparison between the proposed rectifier and other works. The proposed rectifier has an efficiency of above 20% for a wide range of input power from −19 dBm to −5 dBm, higher than [17], [26], [29]-[33] for 1 $M\Omega$ load. In this design, optimum number of stages is used to achieve the highest PCE range and in [17], the author proposed 4 stages rectifier design, but the PCE above 20% range of input is just 8 dBm, which is half of this work's achievement. The area consumption of this work is 2.2, 16.6, and 2.9 times lower than [11], [26], and [30], respectively. Stoopman *et al.* [29] got around 2 dBm greater sensitivity than this work by employing extra needs such as differential antenna and triple nwell transistors. Peak efficacy in [33] is strongly correlated with output load, and as output load increases, peak efficacy decreases. However, this work provides a large PCE dynamic range exceeding 20% with a nearly consistent peak efficiency for diverse loads.

Table 1. Performance summary and comparison

	Frequency	Technology	No. of Stages	Area (mm^2)	Additional Requriments	Peak Efficiency	High PCE** (dBm)	Sensitivity 1 V (dBm)	Load
This work	920 MHz	130 nm	5	0.087	-	39.9% @ -9 dBm	15	-21	1 MΩ
						38.97% @ -5 dBm	14	-18	500 KΩ
						38.5% @ -3 dBm	12	-16	300 KΩ
TCSI, 2022 [33]	915 MHz	130 nm	10	0.029	-	34.5%* @ -19 dBm	7*	-22*	1 MΩ
						42.4% @ -16 dBm	8*	-20*	450 KΩ
						41.5%* @ -14 dBm	8*	-18*	300 KΩ
ISCAS, 2021 [31]	915 MHz	130 nm	6	0.064	Zero V_{th} Transistor	27.6% @ -30 dBm	5*	-17.5*	1 MΩ
2020 [32]	902 MHz	180 nm	2*	0.105	-	28.5% @ -17 dBm	7*	-20.2	1 MΩ
TCSI, 2020 [17]	896 MHz	130 nm	4	0.053	-	43% @ -11 dBm	8.5	-20.5	1 MΩ
JSSC, 2017 [30]	402 MHz	180 nm	3	1.44	Control Loop	31.9% @ -1 dBm	10	-12 @1MΩ	30 KΩ
TCSI, 2015 [26]	915 MHz	130 nm	12	0.25	-	32% @- 15 dBm	10.5	-20.5	1 MΩ
JSSC, 2014 [29]	868 MHz	90 nm	5	0.029	Differential antenna, Triple-Well	24% @ -21 dBm	8*	-23	1 MΩ
JSSC, 2011 [11]	915 MHz	90 nm	17	0.19	Triple-Well	11% @ -18.8 dBm	N.A	-17.5*	1 MΩ

* Estimated from the figure and ** PCE dynamic range above 20%.



(a) (b)

Figure 7. Post-layout simulation of proposed rectifier (a) output voltage and (b) PCE

6. CONCLUSION

A rectifier based on the modified Dickson charge pump with an auxiliary circuit to provide the compensation voltage has been successfully designed using 130 nm CMOS process. The RF rectifier can operate with high efficiency for input power range of 15 dBm without any additional requirements such as control loop and triple-well transistors. By implementing the proposed diode connected metal-oxide-semiconductor field-effect transistor (MOSFETs), the leakage current is reduced and hence improved its efficiency. The proposed rectifier obtained sensitivity of 1 V at -21 dBm for 1 MΩ load, which is the lowest input power to feed the output system. It also achieved 39.9% efficiency at -9 dBm and 15 dBm input power range with PCE above 20% for 1 MΩ load.

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