Adaptation of March-SS algorithm to word-oriented memory built-in self-test and repair

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ABSTRACT

The technology shrinkage and the increased demand for high storage memory devices in today's system on-chips (SoCs) has been the challenges to the designers not only in the design cycle but also to the test engineers in testing these memory devices against the permanent faults, intermittent and soft errors. Around 90% of the chip area in today's SoCs is being occupied by the embedded memories, and the cost for testing these memory devices contributes a major factor in the overall cost and the time to market. This paper proposes a strategy to develop a word-oriented March SS algorithm-basedmemory built-in self-test (MBIST), which is then applied for memory built-in self-test and repair (MBISTR) strategy. The implementation details for 1 KB of single-port static random-access memory (SRAM) depict that the modified March-SS algorithm based MBISTR-enabled SRAM facilitates self-test and self-repair of embedded memories with a marginal hardware overhead (<1%) in terms of look up tables and slice registers when compared to that of standard SRAM.

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1. INTRODUCTION

The system on-chip (SoC) architecture primarily consists of a processor core with single or many processing elements (cores) and embedded memories. The SoCs mainly consists of logic cores, memory partners, interconnects and I/O peripherals. According to the survey of the semiconductor industry association (SIA), embedded memories occupy more than 90% of the silicon area in modern day SoCs. The logic core components in SoCs are tested using logic built-in self-test (LBIST) strategies. i) The LBISTcan be classified into hardware-BIST. ii) software based self-test (SBST). The LBIST strategies are though capable of detecting manufacturing (permanent) faults, these techniques are not effective in handling transient faults which may occur when the system is deployed on the field. The Berger code based concurrent testing [1] is capable of detecting the transient faults.

The requirement for increased data storage (embedded memories) in today's complex SoCshas driven the designers to integrate millions of transistors on a silicon wafer by minimizing the device (transistor) size. The miniaturization in very large-scale integration (VLSI) technology has increased the parasitic effects and manufacturing defects that includebridges, opens, and shortsas well. The cross talks, process variation, parasitics, and short channel effects have introduced newer faults and fault models in high density semiconductor memories affecting the system behavior and performance.

The performance and reliability of SoCs depend hugely on the fault patterns and testing strategies for built-in memories. The high-density static random-access memorys (SRAMs)generally comprises of higher number of manufacturing defects per unit die-area which may result into lower yield as contrastto other glue logic. In addition, the cost of memory testing also increases with the increased memory density. With the availability of precise fault modeling and effective memory built-in self-test strategies, an improvement both in fault coverage and in the yield for embedded memories in today's SoCsis quite possible. This research work aims to develop an effective test methodology for self-testing and repairing of embedded memories in SoCs.

Fault modelingand test strategies for semiconductor memories, is the logical fault models are used to map or model the physical defects (opens, shorts, and bridges) in a circuit to logical faults. The classical fault models used for logic circuits and glue logic are not effective to model memory faults. The functional fault models are the best to model memory faults outlined in [2]–[4].

The effectiveness of a testmethodologyis measured using the metrics: fault coverage and test time. The VLSI test engineers have developed effective fault-diagnosis algorithms by targeting the memory fault models. These algorithms are aimed to improve the fault coverage and also to minimizethe test time. The test strategies for semiconductor memories are categorized into i) classical test methods and ii) march algorithm-based memory built-in self-test (MBIST) methods.

Classical test approaches, the classical test approaches for memory testing presented in the literature [4] suffer with low fault coverage and/or higher test time. March algorithms based MBIST techniques facilitate self-test memories without the need of external test hardware [5]–[10]. The March algorithms are more suitable for fault diagnosis and self-testing of regular 2-D memory architectures. March algorithms [11]–[14] performs March operations (memory write, and memory read operations) in a predefined sequence (ascending or descending order) of memory addressing. Each March operation could be: i) Write 0 (W0) into a memory cell. ii) Write 1(W1) into a memory cell. iii) Reading for '0' (R0) from the addressed memory cell. iv) Reading for '1' (R1) from the addressed memory cell in March algorithms, the following notations are used:

⇑ accessing the memory in an increasing order of its addresses (i.e., from 0 to 2^n-1)
⇓ accessing the memory in a decreasing order of its addresses (i.e., from 2^n-1 to 0)
⇕ accessing the memory in any order of its addresses

The commonly used March algorithms are summarized and compared in Table 1. These algorithms are compared with respect to the following parameters: the required number of March elements and March steps, test sequence, and the fault detection capability. As summarized in the Table 1, the March SS algorithm involves two consecutive Read operations during test sequencing and hence can additionally detect read destructive faults (RDFs) apart from the majority of other faults. This advantage has been the motive behind the selection of March SS algorithm this work though the test complexity (number of March elements and March steps) is higher when compared to other March algorithms.

Table 1. Comparison of various March algorithms

S. No	March Algorithm	No. of March elements	No. of March steps	Test Sequence	Fault Detection capability
1	MATS	4N	3	{⇕W0, ⇕ (R0, W1), ⇕R1}	SAFs, ADFs
2	MATS+	5N	3	{⇕W0, ⇑ (R0, W1), ⇓ (R1,W0)}	SAFs, ADFs
3	MATS++	6N	3	{⇕W0, ⇑ (R0, W1), ⇓ (R1,W0, R0)}	SAFs, ADFs, TFs, CFs
4	March A	15N	5	{⇕W0, ⇑ (R0,W1,W0,W1), ⇑ (R1,W0,W1), ⇓ ((R1,W0,W1, W0), ⇓ (R0,W1, W0)}	SAFs, ADFs, TFs
5	March B	17N	5	{⇕W0, ⇑ (R0,W1,R1,W0,R0,W1), ⇑(R1,W0,W1) ⇓((R1,W0,W1,W0), ⇓ (R0,W1,W0)}	SAFs, ADFs, TFs, CFs
6	March C	11N	7	{⇕W0, ⇑ (R0,W1), ⇑ (R1,W0), ⇕R0, ⇓ (R0,W1), ⇓ (R1,W0), ⇕R0 }	SAFs, ADFs, TFs, Some CFs
7	March X	6N	4	{⇕W0, ⇑ (R0,W1), ⇓ (R1,W0), ⇕R0 }	CFs
8	March Y	8N	4	{⇕W0, ⇑ (R0,W1, R1), ⇓ (R1,W0, R0), ⇕R0 }	SAFs, ADFs, TFs, CFs
9	March SR+	18N	6	{⇓W0, ⇑ (R0,R0,W1,R1,R1,W0,R0), ⇓R0, ⇑W1, ⇓ (R1,R1,W0,R0,R0,W1,R1), ⇑R1}	SAFs, ADFs, TFs, CFs
10	March SS	22N	6	{⇕W0, ⇑ (R0,R0,W0,R0,W1), ⇑ (R1,R1,W1,R1,W0), ⇓(R0,R0,W0,R0,W1) ⇓ (R1,R1,W1,R1,W0), ⇕R0}	SAFs, ADFs, TFs, CFs, RDFs

The March algorithms based MBIST techniques available in the literature are based on bit-access. As the size of memory increases, the number of March operations also increases thereby increasing the test time. The test time can be reduced if the March elements operate on memory words. This paper is focused on the adaptation of March SS algorithm for word-oriented embedded memories.

2. PROPOSED WORD-ORIENTED MARCH-SS ALGORITHM FOR MEMORY BUILT-IN SELF-TEST AND REPAIR

All the March algorithms found in the literature operate March operations on each memory cell (i.e. at bit-level) in ascending or descending or any order of memory addressing. This bit-wise access of meory cells during MBIST increases the number of March operations which results into enormous delayin test time for high density memories. In this work, the bit-oriented March SS algorithm has been modified into word-oriented (with word length of 8 bits) March SS algorithmso that the entire row (word) of the memory under test (MUT) can be accessed during March operation. The required test/reference patterns, denoted as W0, W1, W7, R0, R1, R7 that can detect all possible faults in the MUTare depicted in Table 2.

The test sequencing for the proposed word-oriented March SS algorithm is given in Table 3. During each memory read operation, the read out data from the MUT is compared with the reference pattern {Ri (i=0,1,2,… 7)} in the output response analyzer (ORA) module. The ORA module detects the presence of fault, if any in the addressed location. The modified word-oriented March SS algorithm has a test complexity of 82xN1 to complete the memory test, where N1 is the size of MUT in terms of the number of address locations.

SAFs, TFs, and ADFs which leads to the majority of the memory faults can be detected with two test patterns W0 and W1. The work presented in this paper focuses on the development of test architecture and analysis of simulation work for these two test patterns only. The number of word-level March operations for these two test patterns in the proposed modified word-oriented March SS algorithm is 22xN1.

Table 2. Test patterns for memory write andreference patterns for memory read operations

S.No.	Test Pattern	Notation	Reference Pattern	Notation	Targetted Faults
1	0 0 0 0 0 0 0 0	W0	0 0 0 0 0 0 0 0	R0	SAFs, ADFs, TFs
2	1 1 1 1 1 1 1 1	W1	1 1 1 1 1 1 1 1	R1	
3	0 0 0 0 1 1 1 1	W2	0 0 0 0 1 1 1 1	R2	CFs, NPSFs
4	1 1 1 1 0 0 0 0	W3	1 1 1 1 0 0 0 0	R3	
5	0 0 1 1 0 0 1 1	W4	0 0 1 1 0 0 1 1	R4	
6	1 1 0 0 1 1 0 0	W5	1 1 0 0 1 1 0 0	R5	
7	0 1 0 1 0 1 0 1	W6	0 1 0 1 0 1 0 1	R6	
8	1 0 1 0 1 0 1 0	W7	1 0 1 0 1 0 1 0	R7	

Table 3. Test sequence for the proposed word-oriented March SS algorithm

March Step	Test Sequence	March Step	March Sequence
1	$\Updownarrow$ W0	10	$\Downarrow$ (R0,R0,W0,R0,W1)
2	$\Uparrow$ (R0,R0,W0,R0,W1)	11	$\Downarrow$ (R1,R1,W1,R1,W2)
3	$\Uparrow$ (R1,R1,W1,R1,W2)	12	$\Downarrow$ (R2,R2,W2,R2,W3)
4	$\Uparrow$ (R2,R2,W2,R2,W3)	13	$\Downarrow$ (R3,R3,W3,R3,W4)
5	$\Uparrow$ (R3,R3,W3,R3,W4)	14	$\Downarrow$ (R4,R4,W4,R4,W5)
6	$\Uparrow$ (R4,R4,W4,R4,W5)	15	$\Downarrow$ (R5,R5,W5,R5,W6)
7	$\Uparrow$ (R5,R5,W5,R5,W6)	16	$\Downarrow$ (R6,R6,W6,R6,W7)
8	$\Uparrow$ (R6,R6,W6,R6,W7)	17	$\Downarrow$ (R7,R7,W7,R7,W0)
9	$\Uparrow$ (R7,R7,W7,R7,W0)	18	$\Updownarrow$ (R0)

2.1. Modified word-oriented March SS algorithm based MBIST architecture

A 1KB (1024x8 bit) single-port RAM (SPRAM) has been considered as MUT in this work. The MBIST architecture, depicted in Figure 1 consists of i) MUT, ii) a 2x1 Multiplexer (MUX), which selectsappropriate address, data, write and read control signals during the normal and test mode of operation, iii) test pattern generator (a REG file consisting of two registers holding 8-bit test patterns W0and W1), and iv) address sequencer (a 10-bit binary up-down counter). The entire operation of MBIST architecture is controlled by a MBIST controller which is a finite state machine (FSM). The MUT can be operatedeither in normal mode (TM=0) or in test mode (TM=1). For normal mode, the MUX selects the input/output functional data, memory address lines, memory write and memory read control signals so that normal functional operation (memory write and memory read) is carried out. During test mode of operation, the multiplexer selects the test patterns (W0 or W1from the REG file), memory address generated by address sequencer, and memory read/write control signals based on address sequencing.

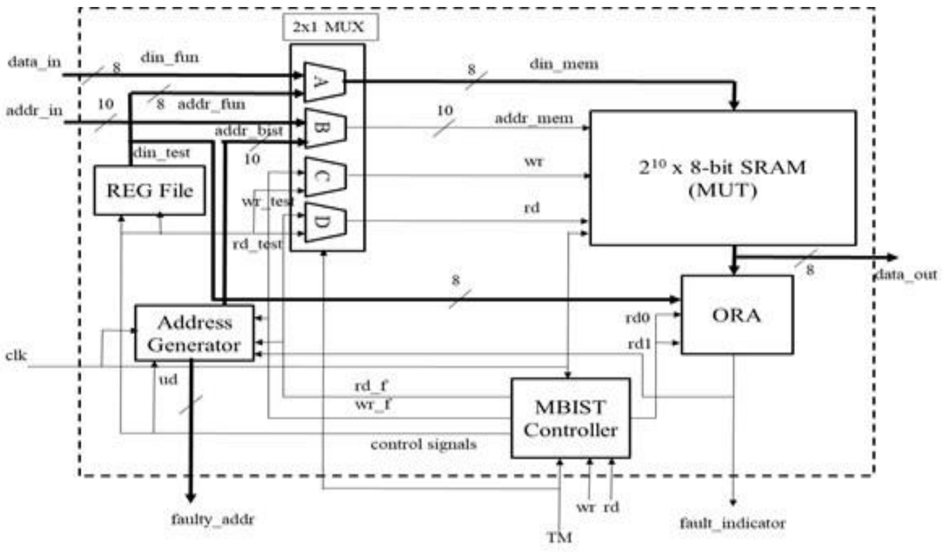


Figure 1. March SS based MBIST architecturefor word-oriented memory

2.2. Design of MBIST controller

The proposed MBIST controller whose FSM diagram is depicted in Figure 2 performs the following operations: i) It activates the up-down counter which generates the addresses for the MUT in a pre-defined sequence governed by March SS algorithm, ii) It asserts the memory write operation in the addressed memory location to write the selected test pattern (W0 or W1), and iii) It asserts the memory read operation from addressed memory location. After the memory read operation, the ORA module compares the read out data from the memory with the reference pattern to detect any faults in the addressed memory location.

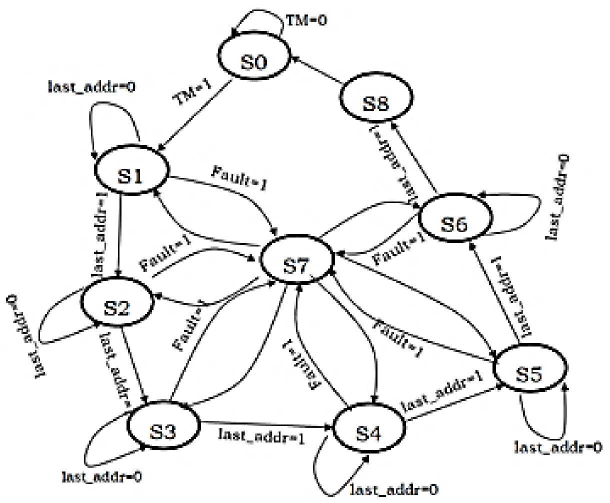


Figure 2. State diagram of the FSM based MBISTcontroller

2.3. Memory built-in self-test and repair (MBISTR) strategy

The memory built-in self-repair (MBISR) strategies found in the literatures [15]-[26] are capable of self-repairing the faulty embedded memory modules with additional hardware in terms of redundant memory array (additional rows and/or columns). The architecture of MBISTR strategy [27] proposed in this work is depicted in Figure 3. The architecture consists of two main modules; i) MBIST-enabled SRAM, and ii) a self-repair unit, which primarily consists of redundant memory array (RMA). In the test mode of operation, the faulty locations in MUT are stored in a faulty address memory (FAM) array addressed through FM_addr generated using fault-map (FM) address generator which is a mod-16 counter incremented every time a faulty location in MUT is detected. These faulty addresses are mapped to the RMA i.e., the multiplexer selects output data from the RMA to retrieve fault-free data.The size of FAM and RMA is the key for hardware overhead in the MBISTR architecture. Considering the hardware overhead in MBISTR architecture, a FAM of size 2^4x 10 is chosen which is capable of storing a maximum of sixteen 10-bit faulty addresses of MUT. All the 16 faulty addresses of MUT can be mapped with 2^4x8 RMA. At the end of memory test, the MUT will return to functional mode with FAM consisting of all the faulty addresses from RMA.

The FSM diagram for the MBISTR controller which controls all the operation of MBISTR architecture is depicted in Figure 4. At ‘S0’state, the input address to the memory is checked in FAM using the fault-map unit (FMU). When a match is found, the FMU asserts addr_matched signal to 1 indicating the addressed location in the primary memory is faulty. The MBISR controller then goes to the state ‘S1’, wherein, the subsequent memory (write or read) operations to these faulty addresses are switched into the RMA by asserting wr_rma or rd_rma signals and then the controller then enters into ‘S2’ state. At the end of memory access cycle, the controller returns to ‘S0’state.

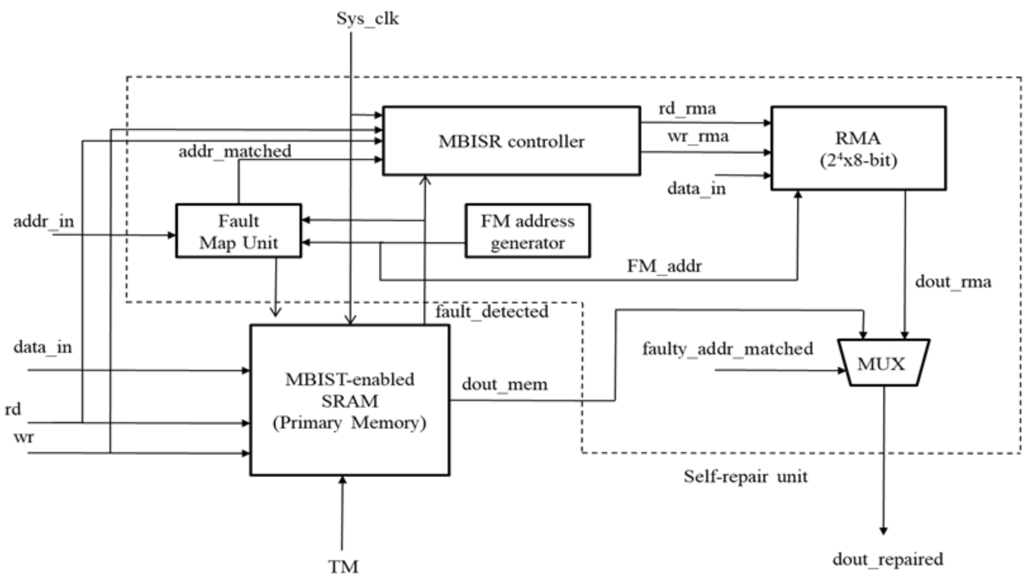
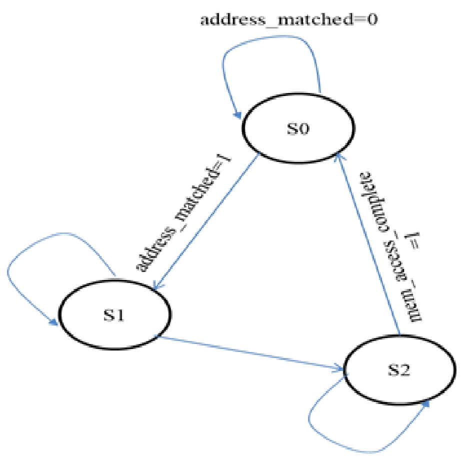


Figure 3. Proposed architecture of MBISTR



State	Activity	Description
S0	Initialization	Checks the input address with the entries in FAM until **address_matched** is asserted by FMU. The controller moves to state S1 when it is asserted.
S1	Self-repair	Access fault-mapped address from RMA by asserting **wr_rma** and **rd_rma** signals. Issues **FM_addr** to RMA.
S2	Repair done	The controller returns back to S0 state when the memory access is completed.

Figure 4. Typical state diagram for FSM based MBISR controller

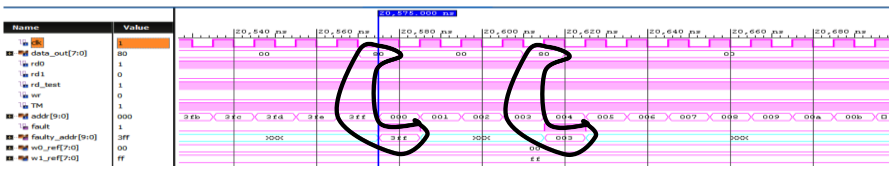
3. RESULTS AND DISCUSSION

The simulation in this work has been carried out in Xilinx Vivado 2017.4 environment using Verilog HDL. Xilinx SynthesisTools has been used to synthesize the proposed March-SS algorithm for word-oriented MBIST and MBISTR. The effectiveness of this method is presented and discussed in the following sub-sections.

3.1. Simulation results and implementation details of MBIST

During test mode of operation, the 2x1 MUXat the input side of the MUT selects the memory address from the address generator. It also selects the test patterns from REG fileandmemorywrite and memory read control signals as per the test sequencing defined by the proposed word-oriented March SS algorithm. The functional simulation for the proposed 1 KB MBIST controller is carried out at 100 KHzclock frequency. The proposed methodology has a test complexity (number of memory operations)of 322*N1 which results into a simulation delay of 225.50 ms.

The fault simulationin this work is carried out by injecting stuck-at-1 (SA1)faults at the most significant bit (MSB) position of memory locations 3FFH and 003H. These two faults are detected during the test mode of MUT when R0 operationis carried outwhen the MBIST controller is in the state ‘S2’. When these faults are injected, the read outdata for R0 operation following W0 operation will be 80H instead of 00H. The faulty locations (faulty_addr[9:0]) are stored for possible self-repair activity, discussed in the next section. The detection of memory faults at address locations 3FFH and 003Hhas been depicted in the simulation outcome shown in Figure 5.



Fault injected: S@1 fault at most significant bit (MSB) position of address locations 4’h3FF and 4’h003.
Inputs
TM=1 (**MBIST operation)**
rd_test=1, rd0=1 (**Memory read operation – R0)**
data_out: 4’h80 (Output of read data from memory to the input of ORA)
Outputs

Figure 5. Illustration of fault detection using word-oriented March SS algorithm based MBIST technique

The 1 KB single-port RAM with MBIST capability is implemented on 7-series Zynq Field programmable gate arrays (FPGA) (Xc7z020clg484-1). The hardware utilization for 1KB SPRAM without and with MBIST hardware is compared and presented in Table 4. The results obtained in the experiment show that ainsignificant (less than 3%) hardware overhead (in terms of LUTs and slice registers) enables self-testing.

3.2. Simulation results and implementation details of MBISTR

The synthesizable register transfer level (RTL) code for MBISTR is written using verilog hardware description language (HDL) and implemented in 7-series Zynq FPGA(Xc7z020clg484-1). After the memory self-test and fault mapping process, the MUT turns into normal (functional) mode of operation. The design implementation of the proposed word-oriented March SS algorithm based MBISTR and its functional verification has been demonstrated in this section. The hardware overhead in terms of self-repair unit introduces the faulttolerance in the SRAM.

In this work, to illustrate the fault simulation capability of the proposed MBISTR architecture, a SA1 fault is inserted at MSB position of memory location addressed at 000H, 003Hand 3FFH. In the presence of this fault, the data read out from these addresses’ values will be 80Hagainsta test pattern of 00H written. The faulty addresses are stored in FAM as depicted in Figure 6. The self-repairing ability of the proposed architectureof MBISTR is demonstrated through the simulation outcome shown in Figure 7. The presence of SA1 fault at MSB position of address location (003H) has caused an erroneous read out data from memory to be data_out=D5H whenaninput data (data_in=55H) is written at this address. The correct data (Dout_repaired=55H) has been retrieved from the RMA. The hardware utilization for a single-port RAM (SPRAM), MBIST-enabled SPRAM, and MBISTR-enabled SPRAM is summarized in Table 4, which shows that the MBISTR-enabled SPRAM though requires a marginal (less than 1%) hardware overhead (LUTs and slice registers), introduces the fault-tolerance in the memory.

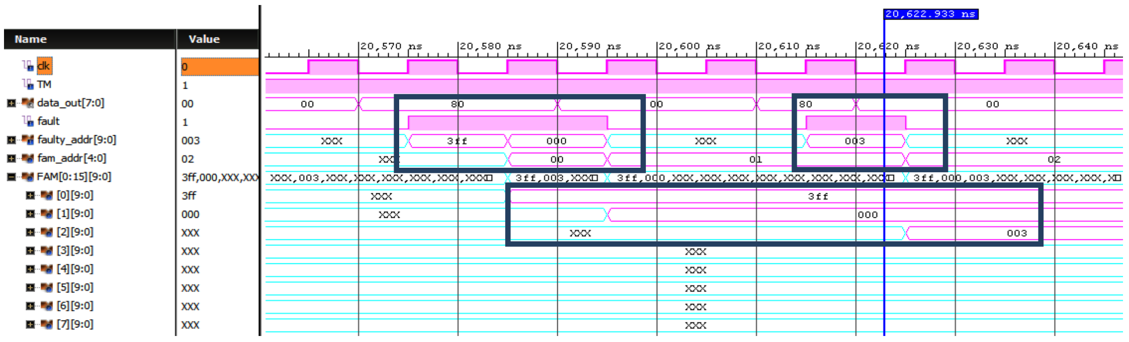


Figure 6. Simulation outcome demonstrating fault detection and fault-mapping

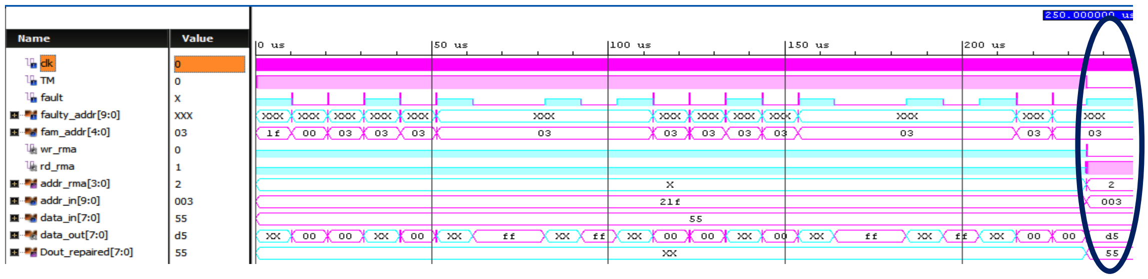


Figure 7. Simulation result of MBISTR for fault detection and self-repair

Table 4. Summery of hardware utilization of 1KB standard SPRAM, MBIST and MBISTR

S. No	Resource	Available	Standard SPRAM		MBIST-enabled SPRAM		MBISTR-enabled SPRAM	
			Utilization	%	Utilization	%	Utilization	%
1	Slice LUTs	17600	3516	19.98	3684	20.93	3715	21.07
2	Slice Registers	35200	8197	23.29	8256	23.45	8281	23.52
3	IOs	102	29	28.43	41	42.16	45	44.18
4	F7 Muxes	8800	1052	12.36	1052	12.36	1052	12.36
5	F8 Muxes	4400	472	12.36	472	12.36	472	12.36

4. CONCLUSION

This paper discusses a Memory Built-In Self-Test and Repair methodology based on a word-oriented March SS algorithmwhich is derived from the original bit-oriented March SS algorithm. The modified word-oriented March SS algorithm requires 22 word-level March operations to detect majority of memory faults i.e., SAFs, ADFs. The test complexity of the proposed architecture has been 22xN1 (=22,528) word-level operations for 1 KB (2^{10}x8) SPRAM, as compared to 22xN1x8 (=1,80,224) bit-level operations. The hardware utilization of MBISTR methodology requires a hardware overhead (LUTs and slice registers) of ~1% as compared to that of MBIST-enabled SRAM. This marginal hardware overhead has introduced a fault-tolerance in the embedded memories improving the reliability.

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