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A Power-Gating Scheme for MOS Current Mode Logic Circuits

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Abstract

MOS Current-Mode Logic (MCML) is widely used for high-speed circuits. However, the MCML circuits have large static power consumptions due to their constant operation currents. This paper presents a power-gating scheme for MCML circuits to reduce their static power dissipations in sleep mode. The PMOS transistors for linear load resistors of MCML circuits are used for power-gating switches. A power-gating control circuit consisting of NMOS and PMOS transistors is added for switching power-gating switches under the control of the sleep signal. The structure and operation of the proposed power-gating scheme are presented. In order to verify the correctness of the proposed power-gating scheme, several basic cells and a full-adder based on MCML circuits are realized. All the circuits are simulated with HSPICE at SMIC 130nm technology. The simulation results show that the power dissipations of the MCML circuits can be greatly reduced by shutting down their idle logic blocks.

Keywords*: MOS current-mode computing, low-power electronics, power-gating technique*

1. Introduction

As CMOS process technology scales, a single chip becomes more and more complex [1]. The demand for more processing results in large power dissipations [2]. With the increasing demand for battery-operated mobile platforms like portable computers, laptops, cellular phones, wireless sensors and biomedical applications that require ultra-low energy dissipations, energy-efficient designs have become more and more important for nanometer CMOS circuits [3]. In nanometer CMOS digital circuits, power dissipation consists mostly of dynamic and static components. The total power consumption can be expressed as [4]

$$E_{\text{total}} = C_{\text{L}} V_{\text{DD}}{}^{2} + V_{\text{DD}} I_{\text{leakage}} T \quad (1)$$

where C_L is load capacitance, V_{DD} is source voltage, T is operation cycle, and $I_{leakage}$ is leakage current, respectively. In (1), the first and second terms are dynamic and leakage dissipations, respectively.

Before the CMOS technology is scaled into deep sub-micro processes, the dynamic energy loss dominated total power dissipations, while leakage power dissipation was little, and often neglected [5]. Continued technology scaling reduces area and delay of the CMOS circuits at the expense of degradation in leakage power dissipation [6]. The leakage dissipation caused by leakage currents is becoming an important factor in low-power computer hardware [6]. Based on this change, we should pay more attention to the leakage dissipations. In CMOS circuits, an effective method for reducing leakage power is power-gating techniques [5]. Since not every cell works all the time in the circuits, the source voltage can be cut down when they are in sleep mode to reduce their energy losses by using power-gating techniques.

In MOS Current-Mode Logic (MCML) circuit, source voltage V_{DD} represents logic 1, while V_{DD}-ΔV (ΔV represents output voltage swing) means logic 0. Obviously, its swing is much little than conventional CMOS, and thus the MCML circuits can operate over a higher speed [7]-[9]. Therefore, MCML is widely used for high-speed applications such as high-speed processors and Gbps multiplexers for optical transceivers [10]. Another interesting advantage of this

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technique is that their speed and power consumption can be simply adjusted by altering the bias current of the gates without the need for resizing the devices [11].

However, MCML has large static power losses due to its constant operation current. Recently, the low power MCML designs have obtained quite some attentions. P. Heydari and G. Caruso presented the methodologies for the low-power design of MCML-based buffer chain and ring oscillators, respectively [12, [13]. Mohab H. Anis et al. proposed the multi-threshold MCML (MTMCML) technology that allows the reduction of the minimum supply voltage of the two-level MCML circuits, thus to lower the power dissipations of MCML circuits [14].

In order to attain both high-speed and energy-efficient designs, reducing static dissipations of the MCML circuits is demanded. In this work, we present a power-gating scheme for MCML circuits to reduce their static power dissipations in sleep mode. This paper is organized as follow. In section 2, conventional MCML circuits are reviewed. In section 3, a power-gating scheme for MCML circuits is introduced for the MCML circuits. The structure and operation of the proposed power-gating scheme are described also in section 3. In section 4, we compared the power dissipations of several basic cells and full-adders based on the conventional MCML without power-gating and the proposed power-gating MCML by using HSPICE simulations. Finally, our work of this paper is summarized in the last section.

2. MCML Circuits

The basic MCML inverter/buffer and its bias circuit are shown in Figure 1. The MCML inverter/buffer is composed of three main parts: the load transistors P1 and P2, the full differential pull down network (PDN) switch consisting of the NMOS transistors N1 and N2, and the current source transistor Ns. The load transistors are designed to operate at a linear region with the help of the control voltage V_{rfp} produced by the bias circuit, which also controls the output logic swings [7]. The pull-down network (NMOS transistors N1 and N2) are used to perform logic operation. The NMOS Ns is used to provide the constant current source, which is mirrored from the current source in the bias circuit.

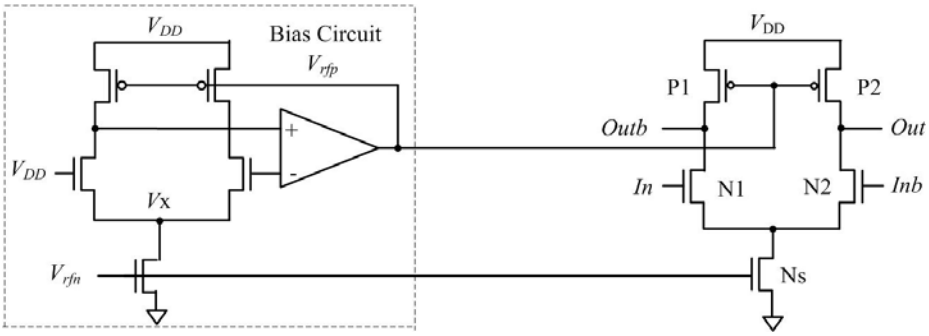

Figure 1. MCML inverter/buffer and its bias circuit

In the MCML circuits, the two signals V_{rfp} and V_{rfn} are generated from the bias circuit to ensure the proper operating for output voltage swings and to provide the constant bias current. This construction decide that the high and low levels of the output voltages are $V_{OH} = V_{DD}$ and $V_{OL} = V_{DD} – I_B R_D$, respectively, where R_D is the PMOS load resistance, and I_B is the bias circuit. The logic swing $\Delta V = V_{OH} – V_{OL} = I_B R_D$.

MCML is a type of differential logic with differential input logic tree. Therefore, the design of the MCML PDN is similar to other differential logic styles such as DCVSL and DSL. The complex logic functions can be realized by replacing N1 and N2 with NMOS logic trees. The MCML basic gates such as AND2/NAND2, OR2/NOR2, XOR2/XOR2 are shown in Figure 2.

The formula of 1-bit Full adder can be expressed as

$$Co = AB + BCi + ACi \quad (2)$$

$$S = ABCi + \overline{Co}(A + B + Ci) \quad (3)$$

where *A*, *B*, *Ci* are input signals, *Co* is the carry output, and *S* is the sum of *A*, *B*, and *Ci*. From (2) and (3), 1 bit Full adder based on MCML can be constructed by four PMOS transistors and twenty-eight NMOS transistors, as shown in Figure 3, where Figure 3 (a) is the sum circuit, and Figure 3(b) is the carry circuit.

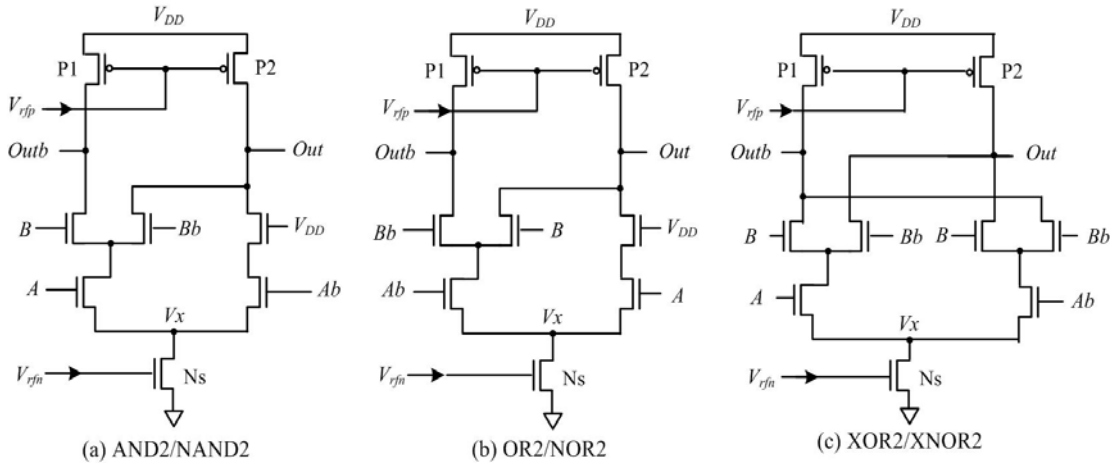

Figure 2. Basic gates based on MCML

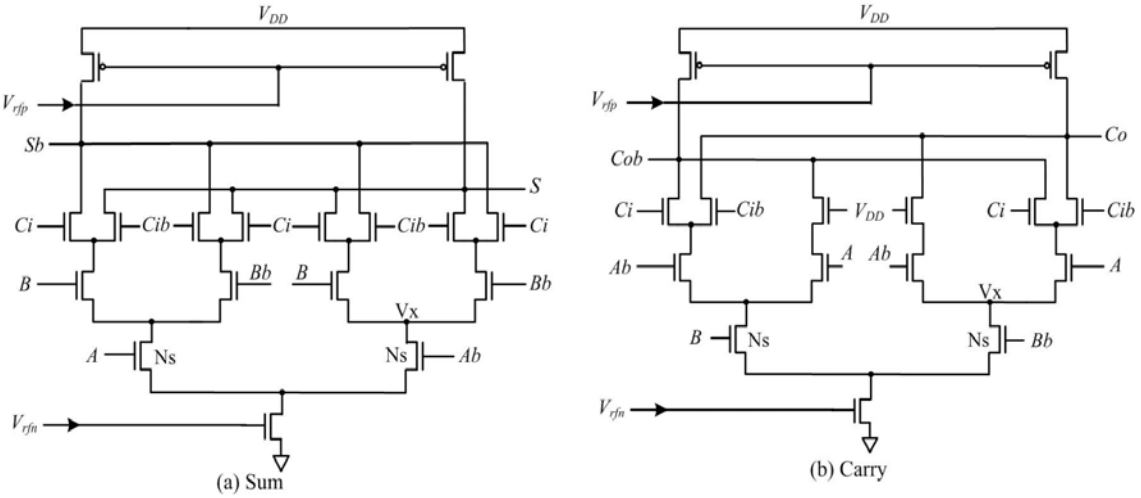

Figure 3. 1-bit Full adder based on MCML

As is known to all, the power consumption of MCML can be expressed as

$$P = V_{DD} I_B \quad (4)$$

Easily, energy consumption can be expressed as

$$E = V_{DD} I_B T \quad (5)$$

where *T* is the operation time of the circuits.

From (5), a direct solution for reducing energy consumption is scaling down supply voltage, since the total energy is reduced linearly as supply voltage decreasing. On the other hand, to ensure the performance of circuits, standard source voltage must be provided when the cells are in active mode. However, not every cell works all the time. This behavior leads to needless waste of energy.

3. Power-Gating Scheme for MCML Circuits

Static CMOS circuits don't exist any direct path between the power supply and ground under steady-state operating conditions. The absence of current flow (ignoring leakage currents) means that the circuits don't consume any static power. However, in the typical MCML circuits, energy dissipation occurs even for constant input signals, because their constant operation current are always from the power supply to flow into ground, so that the energy are wasted.

In conventional CMOS circuits, disabling the power supply for the inactive portions of the circuits is a useful approach for power dissipation reduction [5]. Similarly, idle MCML logic blocks can be also shut down by using power-gating.

Since the structure, operation, and signal waveforms of the MCML circuits are different from the conventional CMOS circuits, power-gating scheme and switches should also be different. There are kinds of ways to realize power-gating MCML circuits. In this work, the power-gating for MCML circuits is realized by cutting off the passage from power voltage to ground, as shown in Figure 4.

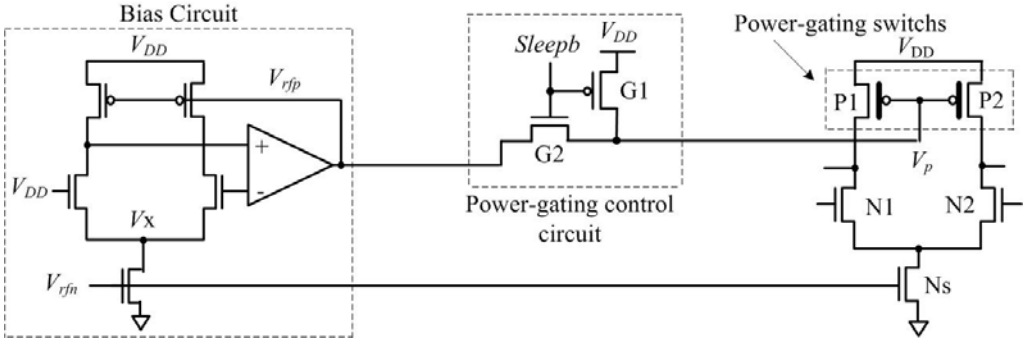

Figure 4. Power-gating scheme for MCML circuits

The power-gating for the basic MCML gates can also realized such as AND2/NAND2, OR2/NOR2, XOR2/XNOR2, as shown Figure 5.

In the power-gating MCML circuits, an extra input signal *sleepb* is added to control V_{rfp}. As is shown in Figure 4 and Figure 5, The PMOS transistors (P1 and P2) used for linear load resistors of MCML circuits are used for power-gating switches. A power-gating control circuit consisting of NMOS transistor (G2) and PMOS transistor (G1) is added for switching power-gating switches under the control of the signal *sleepb* (active control signal).

The simulated waveforms of the power-gating MCML (Figure 4) are shown in Figure 6. The power-gated MCML circuits works in two modes under the control of *sleepb* (active control signal). Its operation is explained as follows.

When *sleepb* is high, the circuit works in active mode. The PMOS transistor G1 is off and the NMOS transistor G2 is turn on, and thus $V_p = V_{rfp}$, so that the power-gating switches (P1 and P2) act as normal linear load transistors. Therefore, the MCML circuits operate in active mode.

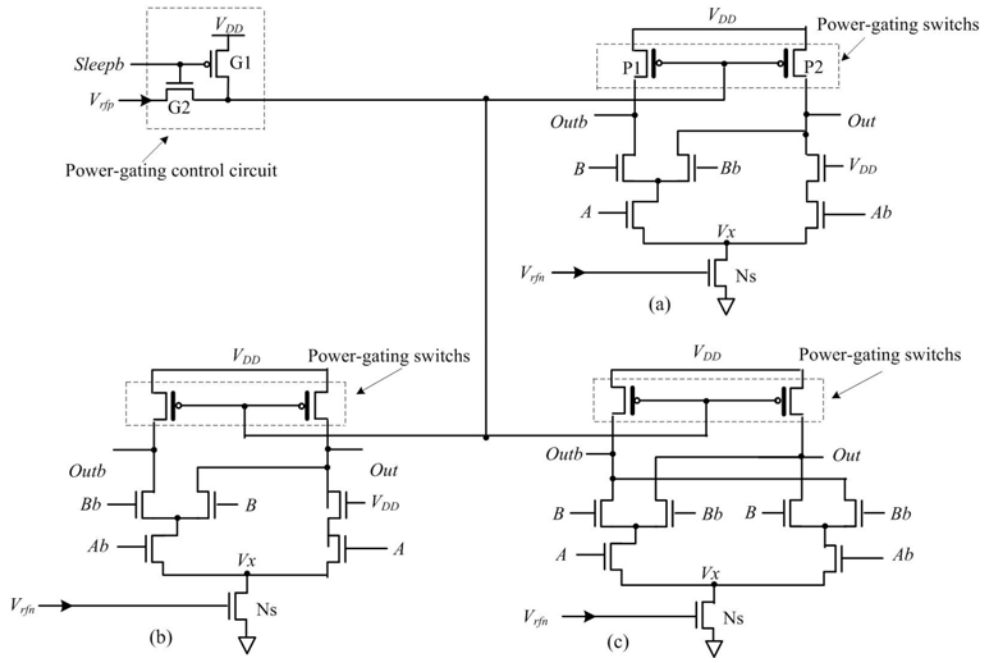

Figure 5. Power-gating MCML gates. (a) AND2/NAND2, (b) OR2/NOR2, and (c) XOR2/XNOR2

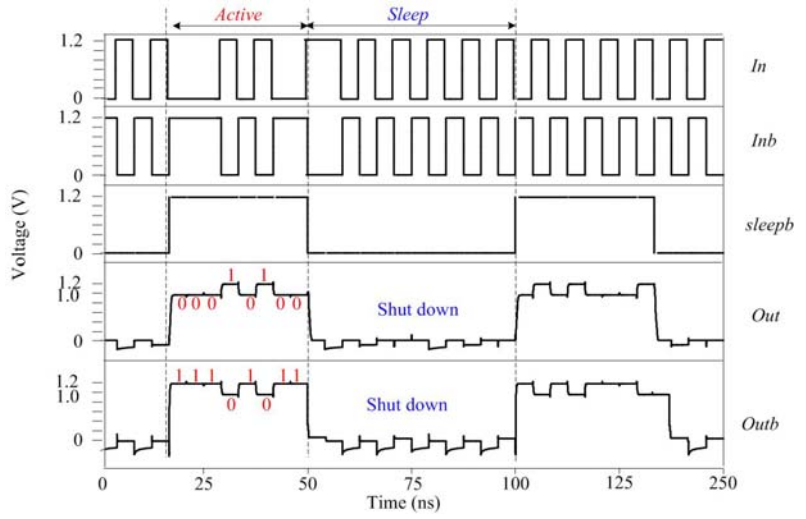

Figure 6. Simulated waveforms for the power-gating MCML inverter/buffer

When *sleepb* is low, the circuit works in sleep mode. The PMOS transistor G1 is turn on and the NMOS transistor G2 is off, and thus $V_p = V_{DD}$, so that the power-gating switches (P1 and P2) are shut off. Therefore, the current passage of the MCML circuits from power voltage to ground is cut off . the MCML circuits operate in active mode.

In normal MCML circuits, the load transistors P1 and P2 use standard threshold voltage. In this work, high threshold PMOS transistors are used as power-gating switches to reduce static power dissipations of the power-gated MCMML circuits in sleep mode.

The sub-threshold current of MOS transistors I_{sub} occurs due to minority carrier move by diffusion along the surface below the channel, when the gate voltage is below the threshold voltage. It is the dominant contributor to the total leakage current at nanometer CMOS process. I_{sub} can be expressed as

$$I_{sub} = \frac{W}{L}\mu V_T^2 C_{sth} \exp\left(\frac{V_{GS} - V_{th} + \eta V_{DS}}{nV_T}\right) \times \left(1 - \exp\left(\frac{-V_{DS}}{V_T}\right)\right) \quad (6)$$

where W and L denote transistor width and length, μ denotes carrier mobility, $V_T = kT/q$ (≈26mV) is thermal voltage at temperature T, $C_{sth} = C_{dep} + C_{it}$ denotes the summation of depletion region capacitance and interface trap capacitance both per unit area of the MOS gate, V_{GS} and V_{DS} are gate-source voltage and drain-source voltage, V_{th} is threshold voltage, η is drain-induced barrier lowering (DIBL) coefficient and $n = 1 + C_{sth} / C_{ox}$ is slope shape factor, where C_{ox} is gate input capacitance per unit area of the MOS gate.

From (6), the sub-threshold leakage current increases exponentially with threshold voltage (V_{th}). For a typical technology with a sub-threshold slope of 100mV/decade, each 100mv reduction in V_{th} will cause an order of magnitude increase in leakage currents. Therefore, increasing the threshold voltage can reduce leakage dissipations.

4. Results and Discussions

In order to verify the correctness of proposed power-gating scheme, simulations must be made. The power-gating realization for the both power-gated MCML block and MCML block without power-gating is shown in Figure 7.

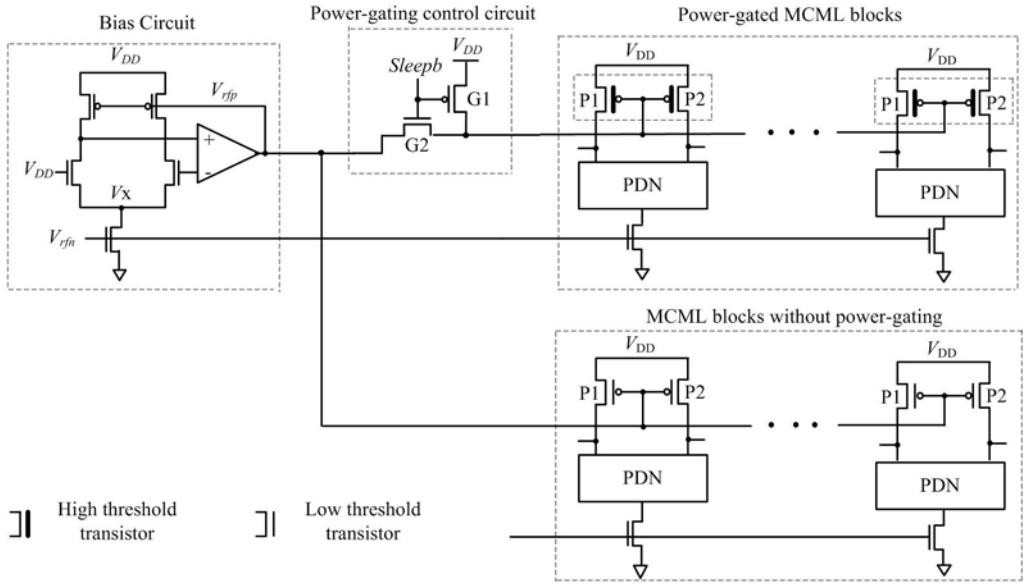

Figure 7. The power-gating realization for both MCML block without power-gating and power-gated MCML block

HSPICE simulations have been carried out. All circuits are simulated at SMIC 130nm technology. Simulation waveforms of the AND2/NAND2 and 1-bit full adder based on power-gating MCML are shown in Figure 8 (a) and (b), respectively.

As is shown in Figure 8, the power-gated MCML circuits have proper logic functions when *sleepb* is high. On the other hand, the *Out* and *Outb* are nearly 0 when *sleepb* is 0, since the power-gated MCML blocks are shut down by using the power-gating.

Power dissipations of the basic gates and 1-bit full adders between the power-gating MCML and convention MCML without power-gating have been compared in Figure 9 for a 50% activity.

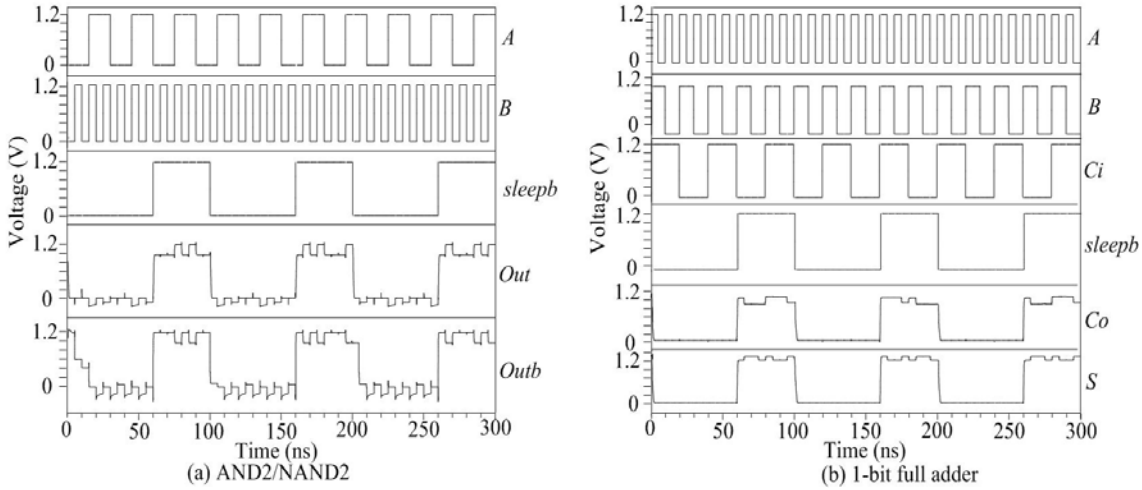

Figure 8. Simulation waveforms of the AND2/NAND2 and 1-bit full adder based on power-gating MCML

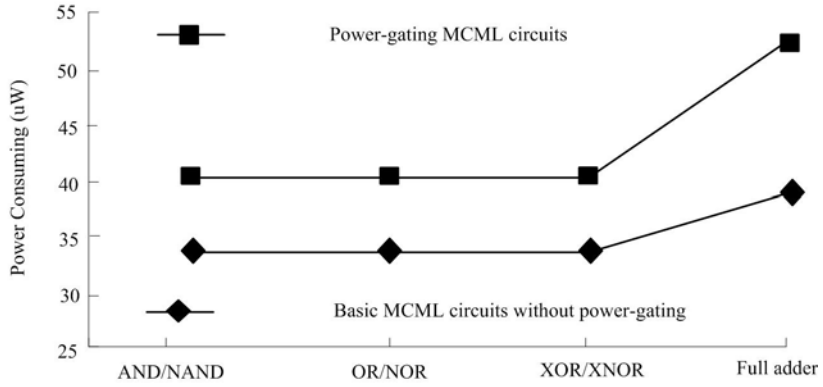

Figure 9. Power dissipation comparisons of the basic gates and 1-bit full adder between the power-gating MCML and convention MCML without power-gating

The power dissipation of power-gating MCML basic gates AND2/NAND2, OR2/NOR2, XOR2/XNOR2, and 1 bit full adder is 33.7uW, 33.7uW, 33.7uW and 39uW, respectively, while the power consumption of conventional MCML ones without power-gating are shown as 40.4uW, 40.4uW, 40.4uW and 52.7uW, respectively. The power-gating MCML basic gates can save about 16.6% energy, and power-gating 1 bit Full adder can save 26% compared with the conventional MCML one without power-gating.

The power dissipations of the 1-bit full adder based on the power-gating MCML have also been compared with the ones based on static CMOS and basic MCML without power-gating, as shown in Figure 10 (a). The working activity is 40%.

As the active ratio α is lowered, more energy savings can be achieved. Figure 10 (b) shows the power dissipations of the power-gated AND2/NAND2 and 1 bit full adder with various active ratio α.

As shown in Figure 10 (a), the power dissipation of the MCML circuits is independent of operating frequency. Moreover, the power dissipation of the power-gated MCML 1-bit-full-adder has an adventage over the static CMOS circuit when operating frequency is higher than 800MHz.

As shown in Figure 10 (b), the proposed power-gating MCML circuits can save more energy as the active ratio α is lowered.

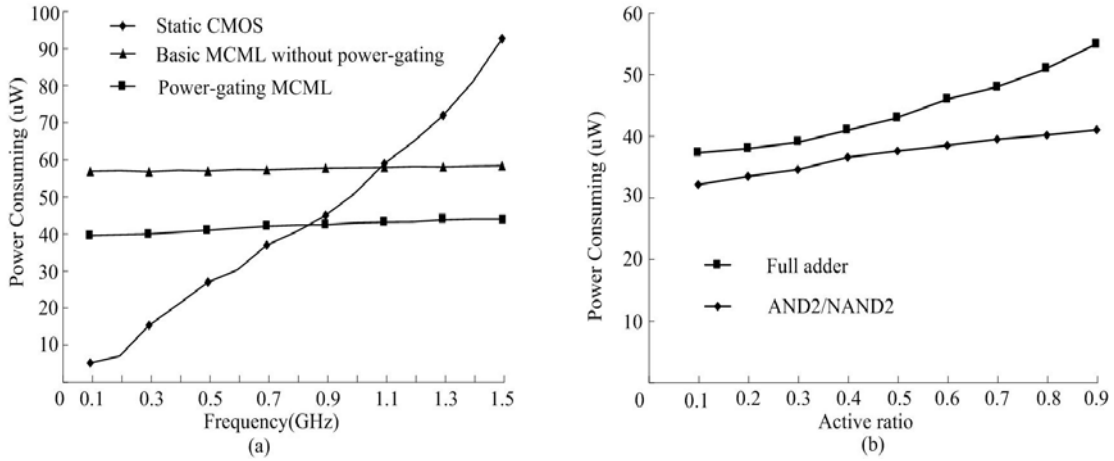

Figure 10. (a) Power consuming comparisons among the 1-bit full adders based on the power-gating MCML, static CMOS, and basic MCML without power-gating, and (b) Power dissipation of power-gating circuits with various active ratio

5. Conclusion

The circuits designed with the MCML techniques can operate over a higher speed than conventional CMOS. However, MOS Current-Mode Logic (MCML) has large static power consumption due to its constant operation current. With the increasing demand for battery-operated mobile platforms like portable computers, laptops, cellular phones, wireless sensors and biomedical applications that require ultra-low energy dissipations, energy-efficient designs have become more and more important for nanometer CMOS circuits.

In order to get both high-speed and energy-efficient designs, a power-gating scheme for MCML circuits has been proposed to reduce their static power dissipations in sleep mode. The PMOS transistors with high threshold for linear load resistors of MCML circuits are used for power-gating switches. The structure and operation of the proposed power-gating scheme are also presented. The simulation results show that the power dissipations of the MCML circuits with the proposed power-gating techniques can be greatly reduced by shutting down their idle logic blocks.

Acknowledgments

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