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Efficient carry select 16-bit square root adder with complementary metal-oxide semiconductor implementation

Pavitha Uppinakere sathyanarayan[1], Mamtha Mohan[1], Sandeep Kakde[2], Annam Karhik[3]
[1]Department of Electronics and Communication, M. S. Ramaiah Institute of Technology, Bengaluru, India
[2]Department of Electronics Engineering, Yeshwantrao Chavan College of Engineering, Nagpur, India
[3]Institute of Aeronautical Engineering, Dundigal, Hyderabad, India

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ABSTRACT

The adder is the maximum usually used mathematics block in programs inclusive of central processing unit (CPU) and virtual sign processing. As a result, it is important to expand a space-saving, low-strength, high-overall performance adder circuit. The hassle is diagnosed to layout mathematics sub structures with minimized strength dissipation, low area, and minimal time postpone of common-sense circuits. In conventional carry select adder (CSA), the time required to generate the sum output is less than other basic adder circuits but the principal difficulty is the location because the variety of transistors used to put in force the CSA circuit is fairly more. So, the area increases because of which the overall power consumption of the circuit will be more. If it's far viable to lessen the variety of transistors used withinside the structure of CSA adder, then, the strength intake of the circuit may be decreased or even the reaction time will improve. By lowering the area of the adder circuit, the suggested solution intends to reduce power consumption and latency.

Corresponding Author:

Pavitha Uppinakere sathyanarayan
Department of Electronics and Communication Engineering
M. S. Ramaiah Institute of Technology
MSRIT Post, Bengaluru 560054, India
Email: alihas@upm.edu.my

1. INTRODUCTION

The logical arithmetic unit is a very important subsystem within any numerical system. The layout of excessive pace and coffee strength Very large-scale integration (VLSI) architectures must be effective. Arithmetic processing units, which can be optimised for overall performance parameters together with pace and power consumption [1], [2]. Adders are key components of general use microprocessors and digital signal processors. Accordingly, optimal design of the adder units improves the overall performance of the system. The amount of space available is a critical consideration in the design of adders [3]. The enormous carry propagation delay [4] observed in traditional adder circuits, such as ripple carry adder and carries save adder, is the major speed constraint of adders. The fundamental benefit of carry select adder (CSA) is that it has shorter propagation delays. The format of high-tempo and low-power VLSI architectures goals inexperienced arithmetic processing units [5], which is probably optimized for the general overall performance parameters, namely, tempo and power consumption. Adders are the crucial aspect components in famous reason microprocessors and digital signal processors. They additionally locate use in lots of different capabilities which includes subtraction, multiplication and division. As a result, the optimum design of the adder units improves the overall performance of the system. Furthermore, for the packages consisting of the Reduced instruction set computer (RISC) processor design, wherein unmarried cycle execution of

commands is the important thing degree of overall performance of the circuits, use of a green adder circuit turns into necessary, to realise green gadget overall performance [6].

The main system construct is 16-bit modified adder circuit. The fundamental benefit of CSA is that it has shorter propagation delays. The targeted parameters are area, delay and power consumption. The modified CSA is improved by reducing the number of transistors used to implement the adder. To achieve the improvement, the binary excess converter (BEC) block of the modified CSA is replaced with improved BEC architecture. The improved BEC uses 3 transistor (3T) AND gate logic.

The main contribution of the paper is as shown in: i) Reduction in area, delay and power consumption, ii) The location is an important element that is to be taken into consideration withinside the layout of adders, iii) The principal pace predicament of adders arises from the massive bring propagation put off encountered withinside the traditional adder circuits, inclusive of ripple bring adder and bring shop adder. The principal benefit of CSA is its decreased propagation put off characteristics, and iv) The modified CSA is improved by reducing the number of transistors used to implement the adder.

The implementation of a 16-bit modified adder circuit is done in Cadence Virtuoso and simulated with Spectre 180 nm complementary metal oxide semiconductor (CMOS) technology with 1.8 V. The outcomes could be as compared with traditional CSA with admire to propagation delay, strength consumption, and transistor count. First the overall CSA adder architecture is divided into five stages with different input bits for each stage. The adder modified from the conventional one, which is proposed in the reference paper is implemented stage by stage. The basic blocks required for implementing each stage like root cause analysis (RCA), BEC and multiplexer (MUX) are generated using individual gates like XOR, and AND, which are made using transmission gates in Virtuoso Schematic Editor and each of their cell blocks are generated for further instantiation. After implementing and generating the modified adder, the improvement is made to the design and then the improved design is simulated. The functionality of both modified and improved are checked for similarity and the parameters like area, power and delay are compare to check for improvements.

The BEC block of the modified CSA is replaced with improved BEC architecture, which consists of 3T AND gate logic. The logic of the 3T AND gates is based on PMOS and NMOS pass transistors (PTL). The main benefit of employing this AND gate design is that it reduces the number of transistors, resulting in a smaller space.

2. RELATED WORK

The carry select adder (CSA) is one of the fastest adders available, and it's employed in many data-processing processors to execute quick arithmetic operations. It is obvious from the CSA's structure that there is room to reduce the CSA's area and power consumption. One of the maximum vital regions of studies in VLSI device layout is the development of area and strength green high-pace information course good judgment systems [7], [8]. The objective of the paper is to realize an efficient adder unit using novel architectural design. The paper improves upon the conventional carry select adder by replacing the ripple carry adder blocks with binary to excess-1 converter (BEC) blocks. Transmission gate (TG) is used to implement the adder logic. The use of TG and BEC reduce the number of transistors used and power dissipation.

In the main research field of VLSI system design [9], [10], the area and power reduction of the data path logic system play a major role. Fast additions and multiplications [11], [12] have continually been a essential requirement for excessive overall performance processors and systems. The sum of every bit role of the simple adder is sequentially generated and carried over to the following role. The circuit architecture is simple and space efficient. Therefore, each full adder can only start operating until the previous carry signal is ready, which slows down the calculation. CSLA [13], [14] is used in many computing systems to mitigate the problem of carry propagation delay and generate sums. The sum of each bit position of the basic adder is sequentially generated and carried over to the next position. There are many types of adder designs, each with its own strengths and weaknesses. The square root carry selective adder [15], [16] is constructed via way of means of compensating for delays because of the 2 convey chains and the block multiplexer sign from the preceding stage.

A ripple-carry adder [17], [18] and a multiplexer are usually used in a carry-select adder. When using a carry-select adder to add two n-bit values, two adders (and hence two ripple-carry adders) are used to do the calculation twice, once with the assumption that the carry-in will be zero and once with the assumption that it will be one. Following the calculation of the two outcomes [19 [20], the proper sum as well as the correct carry-out are picked using the multiplexer once the correct carry-in is known. Ripple carry adders [21], [22] have the maximum compact design, however they perform at a sluggish pace. The carry look ahead adder, on the alternative hand, has a quicker pace however takes up greater space. CLSA [23]

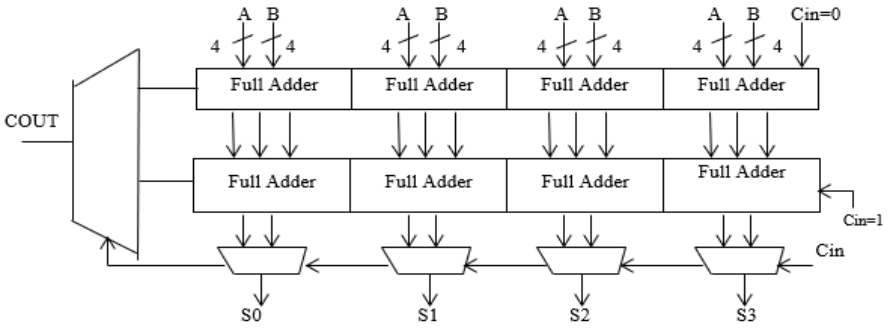
overcomes each the issue that the ripple carry adder and the carry look ahead adder cause. Rather than using dual ripple carry adders, a carry select adder may be built the use of a ripple-carry adder and an add-one circuit. Several adder structures [24] were proposed primarily based totally at the area, delay, and energy intake requirements. In analog design [25], the main parameters which are considered for the designs are area and power.

3. PROPOSED METHODOLOGY AND IMPLEMENTATION OF SYSTEM BLOCKS

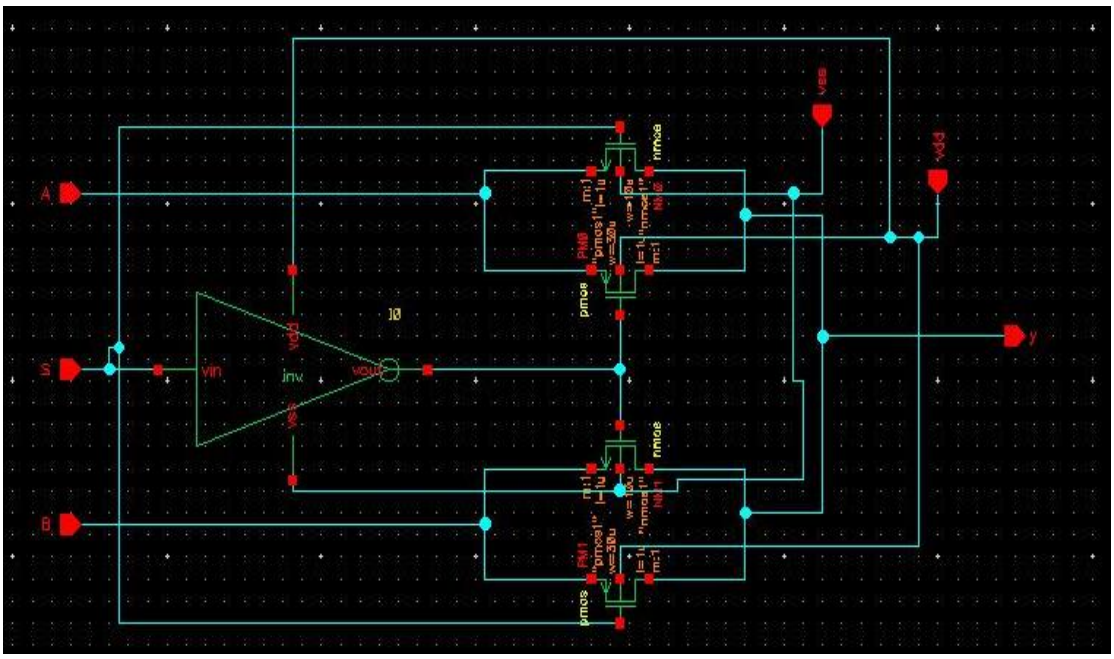
A ripple-carry adder and a multiplexer are usually used in a carry-select adder. When using a carry-select adder to add two n-bit values, two adders are used to do the calculation twice, once with the assumption that the carry-in will be zero and once with the assumption that it will be one. Figure 1 shows the main building blocks, for square root carry-select adder (SQRT CSA) which consists of multiplexer, exclusive OR (XOR) gate, half adder and full adder as shown in Figure 1(a).

3.1. Multiplexer

The 2:1 multiplexer (MUX) implemented using transmission gate (TG) that is used in the paper is proven withinside the Figure 1(b). A multiplexer is a circuit that combines two or more input lines with a single output line. In a simplest way, a multiplexer is a circuit with numerous inputs and a single output. The binary data is collected from the input lines and sent to the output line. One of these data inputs will be connected to the output based on the values of the selection lines.



(a)



(b)

Figure 1. Top level block diagram, (a) carry select adder block diagram and (b) 2:1 MUX using transmission gates

3.2. XOR gate

The XOR gate is implemented using transmission gate architecture as shown in Figure 2. It uses a total of 8 transistors, 2 transmission gates and 2 inverters. An XOR cell is created with two inputs, one output, supply and ground pins, which will be connected in the larger circuits.

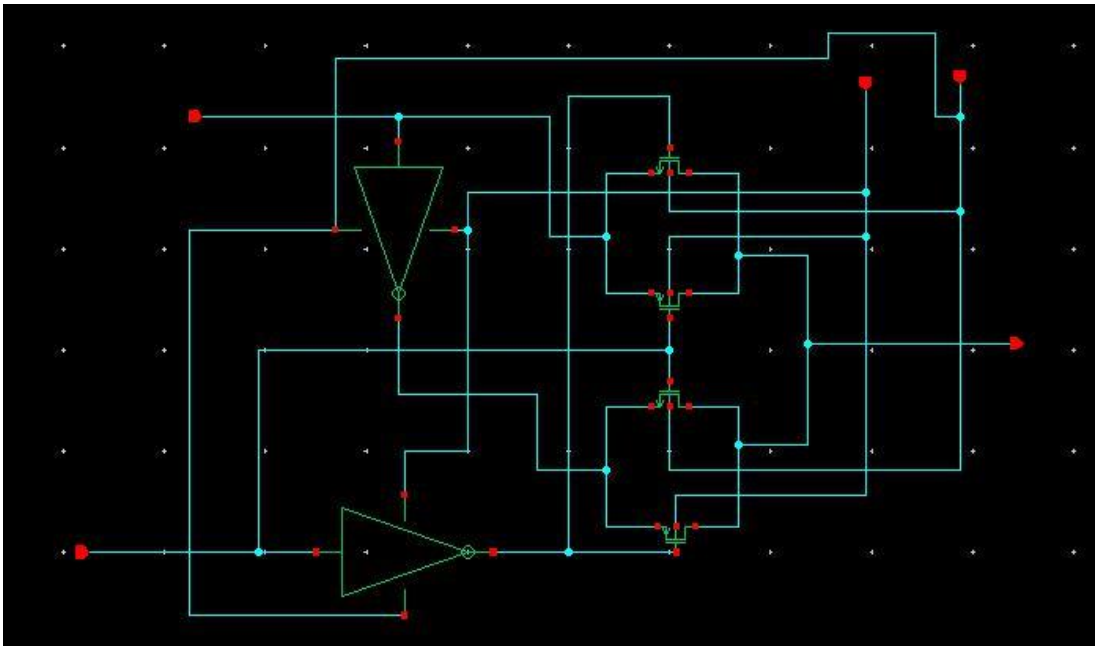


Figure 2. XOR gate using transmission gates

3.3. Half adder

A combination circuit known as a half adder is used to add two bits. The augend and addend bits are the input variables, whereas the sum and carry bits are the output variables. The half adder block is as shown in Figure 3 which is required in the design of CSA adder is implemented using transmission gates, using the XOR gates and AND gates which are as implemented using transmission gates as shown in previous blocks.

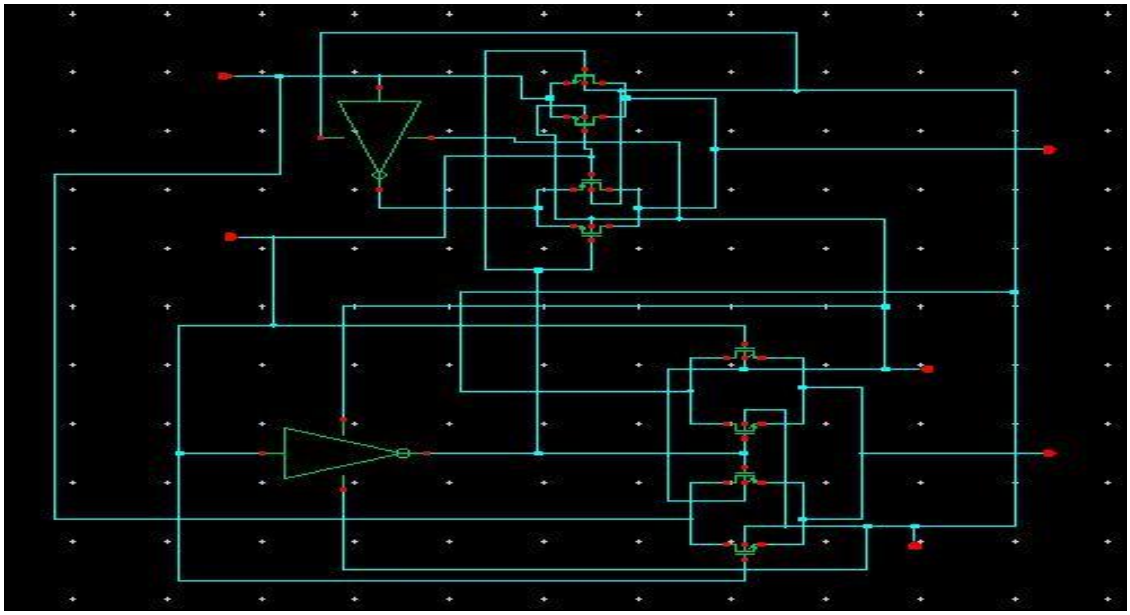


Figure 3. Half adder

3.4. Full adder

The full adder is an adder that takes three inputs and outputs two results. Figure 4 shows 1-bit full adder and it is also implemented using transmission gates just like the half adder design. The first two inputs are A and B, with the third being a Cin input. The Boolean expressions for outputs of 1-bit full adder are given as:

Sum=(A XOR B) XOR Cin
Carry=A * B+Cin *A + Cin * B

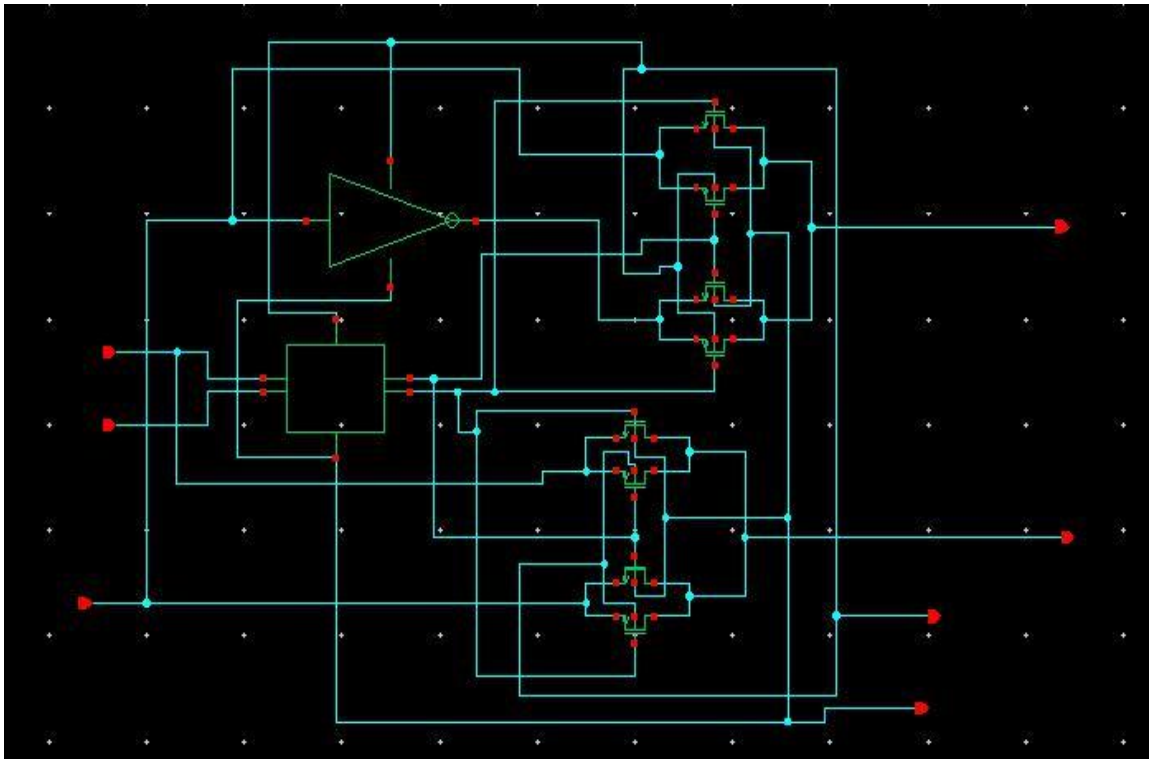


Figure 4. Full adder

3.5. Binary to excess 1 converter (BEC)

Figure 5 shows a 3-bit BEC. For stages with more bits, the same BEC architecture is changed to the required number of bits. The Boolean expressions of the 4-bit BEC is indexed as (observe the practical symbols ~ NOT, and AND, ^ XOR). BEC block is implemented by instantiating the XOR, Inverter and AND gate blocks generated before as per the BEC architecture discussed previously.

X0=~B0
X1=B0^B1
X2=B2^(B0 and B1)
X3=B3^(B0 and B1 and B2)

3.6. 6:3 Multiplexer

Figure 6 shows block diagram of 6:3 MUX and it is implemented using individual 2:1 MUX blocks which was generated before. Similarly, based on different inputs of different stages, the inputs of the MUX are changed. All the circuit level schematics are verified for functional simulations.

3.7. Stage 1

The first stage of the CSA adder has 2bit inputs as per the block diagram discussed before. There is no need for a multiplexer so it is made by cascading two 1bit full adders. The carry out generated by this stage is given as carry in for the next stage (stage 2).

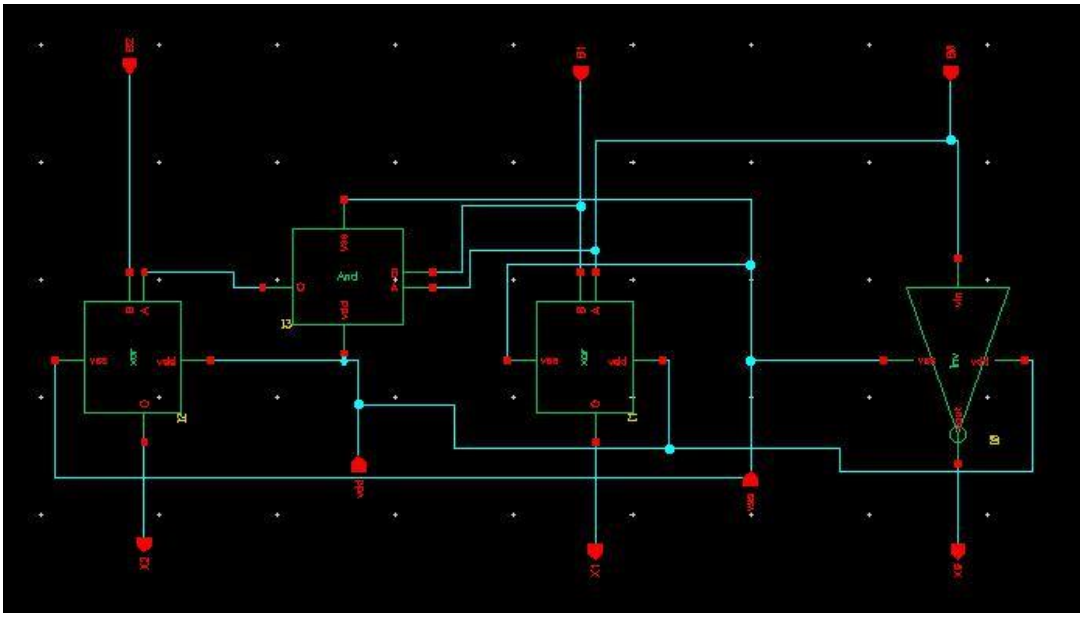


Figure 5. Binary to excess converter

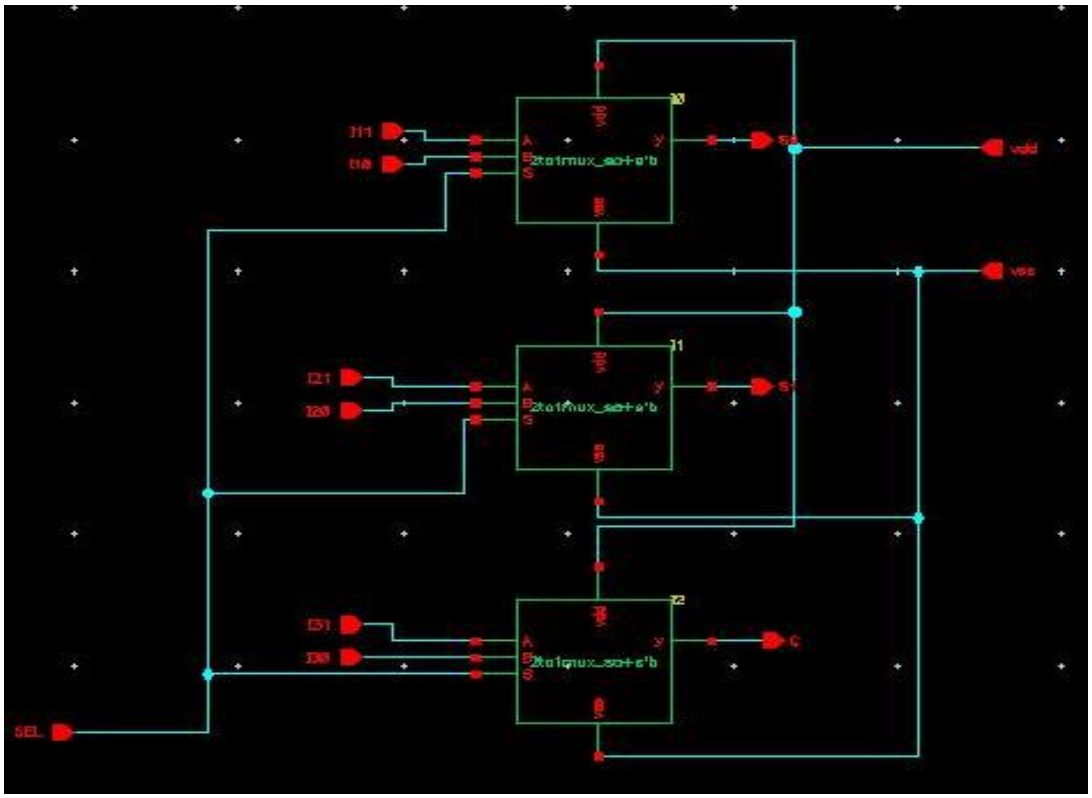


Figure 6. 6:3 MUX

3.8. Stage 2

The 3:2 RCA block with carry in as 1 has been replaced by a BEC block with input 3 bits for the enhanced architecture of the SQRT CSA adder. Figure 7 shows Stage 1 of SQRT CSA and the modified stage is implemented in Virtuoso schematics is show in Figure 8. The modification reduces the number of transistors used for implementing the functionality of adding one to the output of the 3:2 RCA block for carry in of zero. The 6:3 MUX remains the same but, now instead of selecting between the outputs of two 3:2 RCA

blocks, it selects either the output of 3:2 RCA (Cin=0) if carry in of the Stage 2 is '0' or output of the 3bit BEC, if the carry of the stage is '1'.

Other stages of the CSA adder are modified same as that of stage 2, which is a 2-bit stage. For Stage 3 (3-bit inputs), a 4-bit BEC replaces the 4-bit RCA with carry in 1 and so on for other stages The combined 16-bit SQRT CSA is implemented using the individual stages generated before as shown in Figure 9.

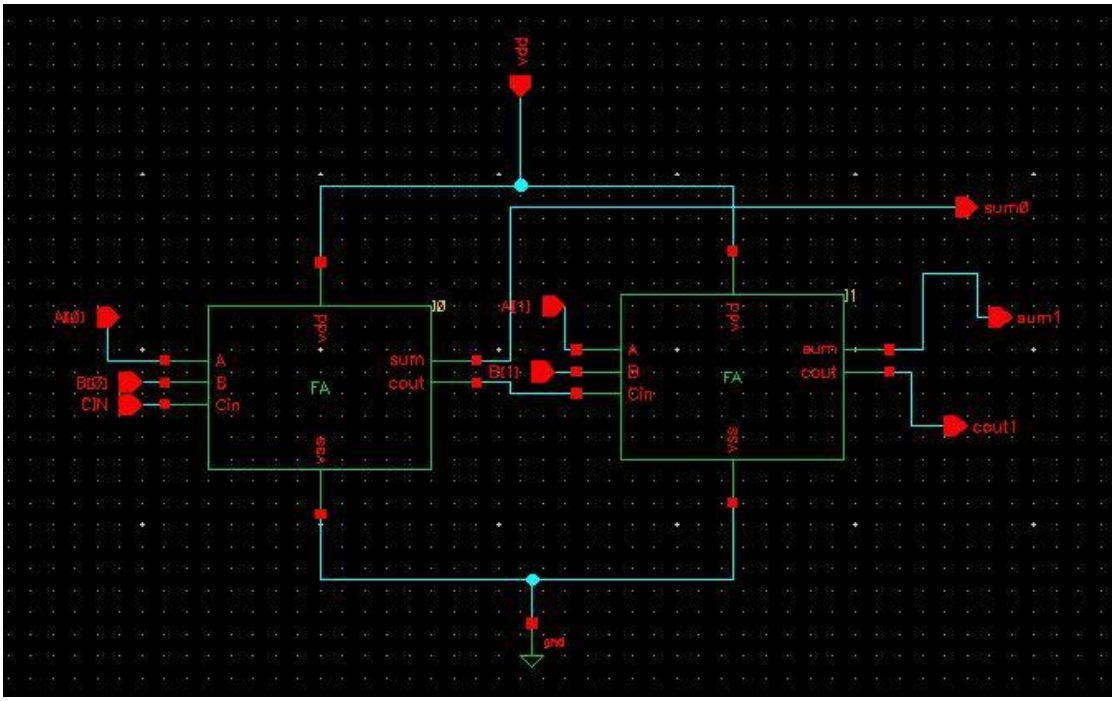


Figure 7. Stage 1 of SQRT CSA

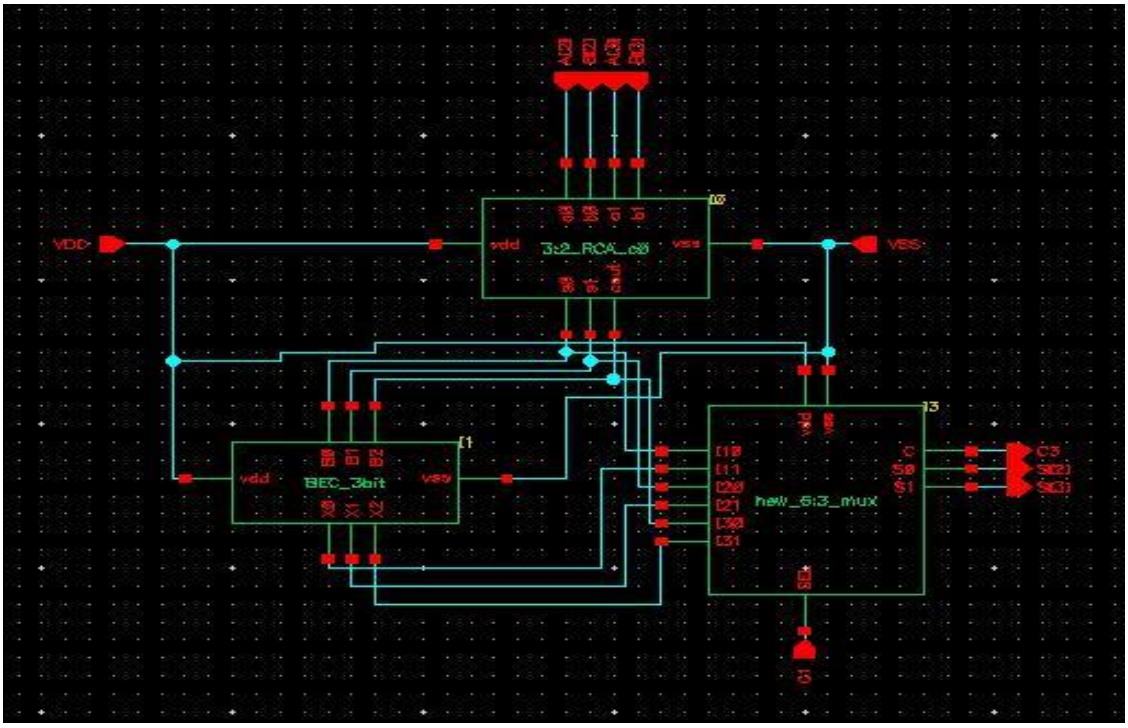


Figure 8. Stage 2 of modified SQRT CSA

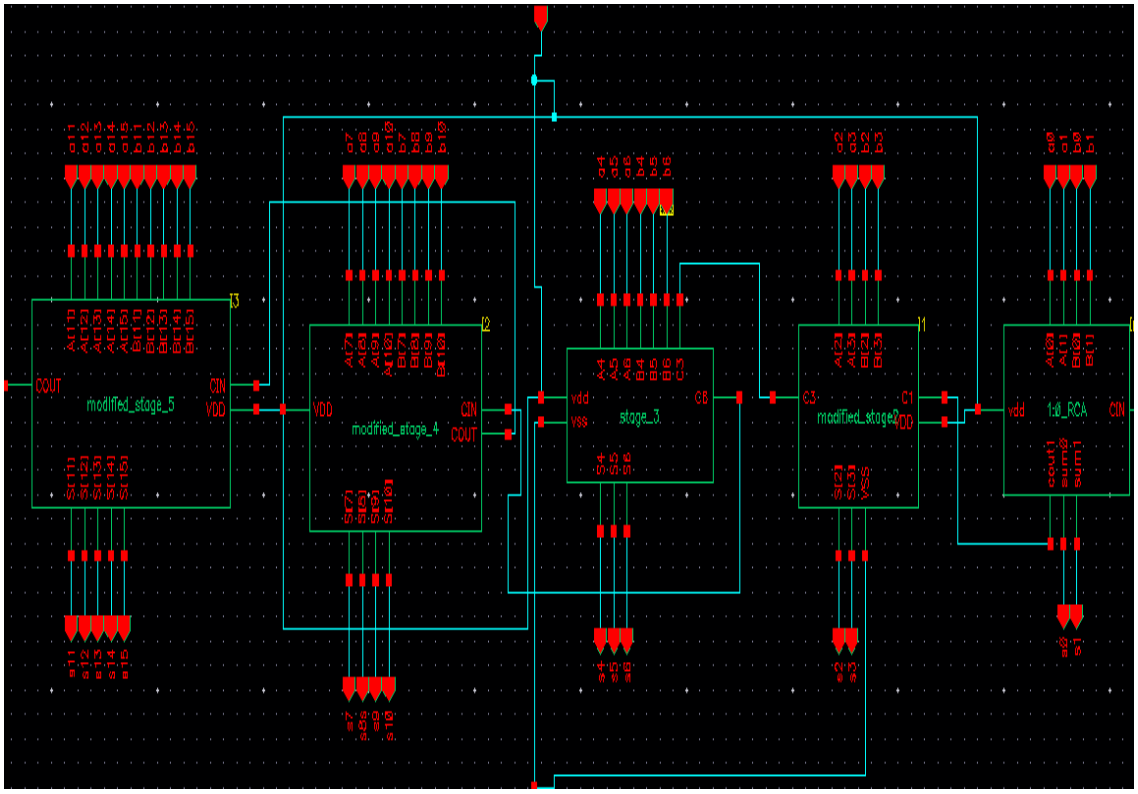


Figure 9. Combined 16-bit modified CSA adder

4. RESULTS AND DISCUSSION

4.1. Power calculations

Power consumption of each stage is calculated to check the performance. Maximum power consumption is calculated for individual stages in Cadence tool using following steps: i) While simulating the design in virtuoso analog design environment window select OUTPUT→save all. ii) In save all enable all options. iii) run simulation. iv) In waveform window select BROWSER→Results→Open results, select Waveform data, a window will pop up, here select *psf* file. v) In left side of waveform window, we can observe a browser. In browser double click on *Tran* option. Here we have current, voltage and power signals at various parts of the design. vi) Double click on *Pwr* option then we can observe wave of power signal in waveform window. vii) The maximum power consumption can be observed at the maximum peak of the waveform.

4.2. Improved design

Figure 10 shows an implementation of 3T AND gate. The changed CSA is progressed through decreasing the quantity of transistors used to put into effect the adder. To achieve the improvement, the BEC block of the modified CSA is replaced with improved BEC architecture.

The improved BEC uses 3 transistor (3T) AND gate logic. The logic of the 3T AND gates is based on PMOS and NMOS pass transistors (PTL). The main benefit of employing this AND gate design is that it reduces the number of transistors, resulting in a smaller space. The 3T AND gate used in BEC is designed using the same transistor parameters used for all the other gates in the adder. The cell blocks of the 3T AND is generated and used to improve the BEC. New BEC blocks are generated by replacing the conventional AND gates with improved AND gates. Improved 3-bit BEC is shown in Figure 11. All the stages of the modified adder are replaced with improved BEC with different input bits according to the stage. The overall transistor count, delay and power consumption of each stage is obtained for comparison.

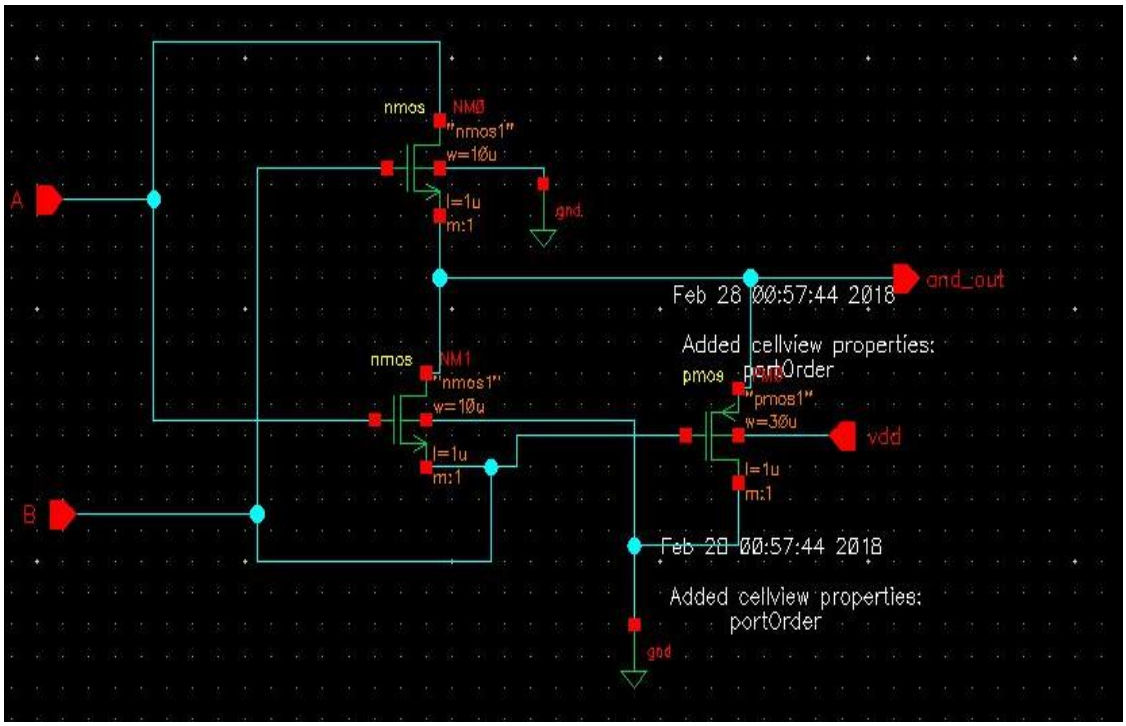


Figure 10. Implementation of 3T AND gate

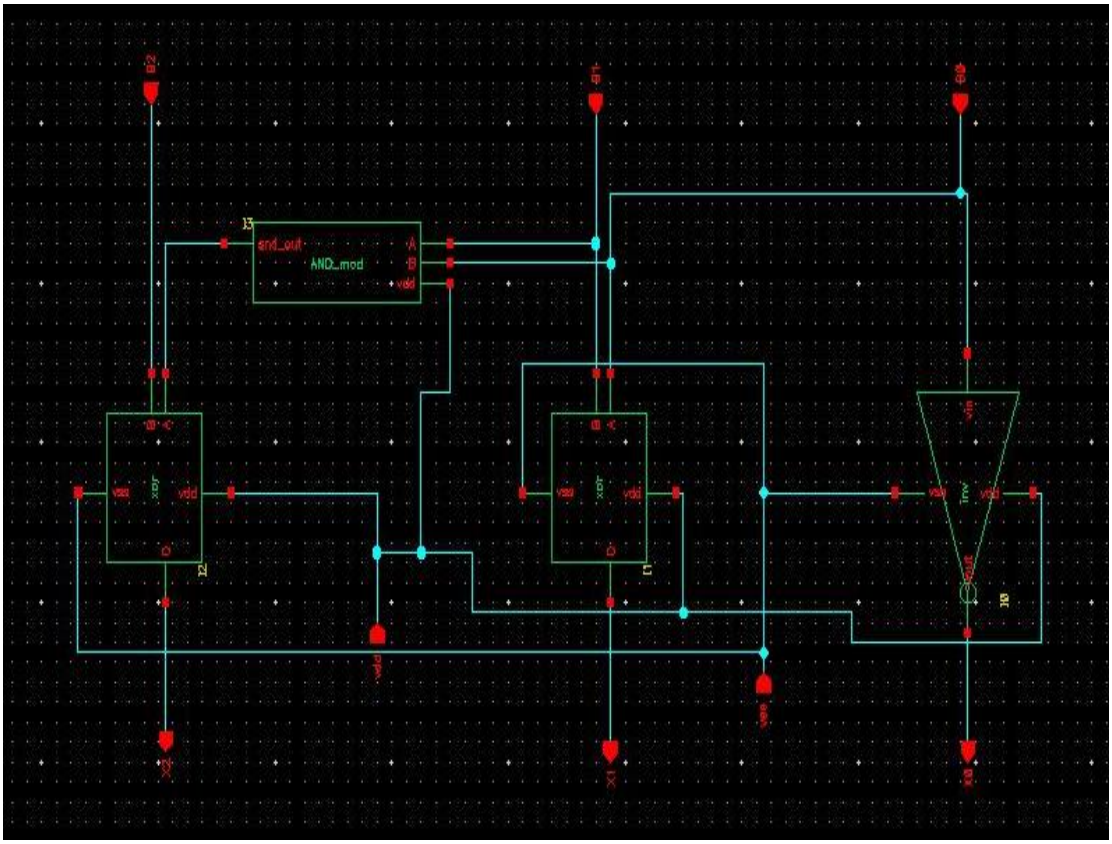


Figure 11. Improved 3-bit BEC

4.3. Simulation results

Table 1 shows simulation results of CSA and Table 2 shows simulation results of improved CSA The modified CSA adder stages are simulated in Spectre simulator 180 nm technology with 1.8 power supply. The parameters like transistor counts, power consumption and delay of each stage is recorded and compared and is as shown in Table 3. From the tables, it is clear that the numbers of transistors are less for improved stages and the delay is also less compared to the modified stages of CSA.

Table 1. Simulation results of CSA

Stages	Transistor count	Power mW	Delay nS
(2bit) Modified Stage1	40	8.099	1.09
(2bit) Modified Stage2	74	12.78	2.13
(3bit) Modified Stage3	116	18.85	3.92
(4bit) Modified Stage4	156	19.12	4.09
(5bit) Modified Stage5	196	21.70	6.01

Table 2. Simulation results of improved CSA

Stages	Transistor count	Power mW	Delay nS
(2bit) Improved Stage1	40	8.099	1.09
(2bit) Improved Stage2	71	12.28	1.08
(3bit) Improved Stage3	110	18.53	2.25
(4bit) Improved Stage4	147	19.65	3.21
(5bit) Improved Stage5	184	24.10	4.51

Table 3. Comparison with existing work

	Carry Selet Adder [5]		Proposed Work	
Features	Transistor count (area)	Delay (nS)	Transistor count (area)	Delay (nS)
(2bit) Improved Stage1	40	1.61	40	1.09
(2bit) Improved Stage2	74	1.85	71	1.08
(3bit) Improved Stage3	116	2.30	110	2.25
(4bit) Improved Stage4	156	3.43	147	3.21
(5bit) Improved Stage5	196	4.82	184	4.51

5. CONCLUSION

In this paper, 16-bit CSA adder is designed by using a 3T AND gate using 180 nm CMOS technology. The improvement done to the modified 16-bit CSA adder by using a 3T AND gate has improved the area and delay of the adder circuit. Since the adder circuit have application in signal processing and multiplexers, the use of improved CSA adder architecture as the sub components in such applications can improve the overall response time and area of the whole applications.

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BIOGRAPHIES OF AUTHORS

Pavitha Uppinakere sathyanarayan is currently working as a Assistant professor in E & C department, M S Ramaiah Institute of Technology, Bangalore. Her research interest includes Low Power VLSI, Face Recognition. She has obtained her B. E in E & C from VTU and M. Tech in VLSI and Embedded Systems from VTU, Belagavi in the year 2005 and 2010 respectively. Curresntly She is persuing Ph. D from VTU; Belagavi. She can be contacted at email: pavitha@msrit.edu.

Mamtha Mohan working as an Assistant Professor at M S Ramaiah Institute of Technology since 16 years. She completed M. Tech at BMS College of Engineering in 2003 and completed Ph. D from Jain university, Bangalore in 2019. She is a member of IEEE and ISTE. Her research interserts are Image Processing, Biomedical Engineering, Wireless Communication, optical Communication Netwroks, Computer Communication Netwroksand Data Structuress. She can be contacted at email: mamtha.m@msrit.edu.

Sandeep Kakde is presently working as Assistant Professor in Yeshwantrao Chavan College of Engineering, Nagpur. He has over nineteen years of industry and college experience, worked as a Senior Design Engineer at Bharat Electronics Limited, Bangalore, as a Senior Design Engineer in Sanyo LSI Technology India Private Limited, ITPL Park, Bangalore, deputed as a Senior Deign Engineer in Sanyo Semiconductors, Japan and as an Assistant Consultant in Tata Consultancy Services, Bangalore. He received his B.E. degree in Electronics Engineering Department from the Visvesvaraya Regional College of Engineering (renamed Visvesvaraya National Institute of Technology), Nagpur, India, in 2000; M. Tech degree in VLSI Design area from Electronics Engineering Department, Yeshwantrao Chavan College of Engineering, Nagpur, India and received Ph. D degree in Electronics Engineering from the University of Nagpur. He can be contacted at email: sandip.kakde@gmail.com.

Annam Karhik Research student in branch of ECE-Veltech Dr. RR & Dr. Sr University, Chennai. He obtained M.Tech (ECE) diploma from Mallareddy institute of technology & science (JNTUH), obtained B.Tech (ECE) from Vaageswari College of engineering (JNTUH). He Worked as Assistant professor in Institute of Aeronautical Engineering, Dundigal, Hyderabad. His regions of interest consists of Digital Signal Processing, Speech processing, Embedded Systems. He can be contacted at email: karthik011190@gmail.com.