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A 4th-order Switch-capacitor Low-pass Filter for Quartz Gyroscope Interface Circuit

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Abstract

This paper presents the computer aided design of a 4th-order switch-capacitor low-pass filter applied in quartz gyroscope interface circuit. After a introduction of switch-capacitor filter (SCF) and its application in quartz gyroscope, the system-level analysis and design is given. Then the circuit design of amplifier, CMOS switch and non-overlapping clock is described. The Fourth-order low-pass SCF has been implemented under 0.5um CMOS process and simulated in computer aided design software. The final simulation results show that the passband is 99.7Hz, and the maximum pass-band ripple is about 0.14dB.The stop-band is 1KHz, and the minimum stop-band attenuation is 78.6dB.

Keywords*: Quartz gyroscope, Switch-Capacitor, Low-Pass Filter, Computer Aided Design*

1. Introduction

Micro-machined sensor is the combination of MEMS technology and inertial technology. And it becomes a research hotspot in recent years. Compared with traditional inertial sensors, Micro-machined sensor combines the advantages of MEMS and Integrated Circuit technology, such as little volume, low price and low mass [1-2]. As an important kind of inertial sensors, Quartz gyroscope is widely used in Inertial Navigation System (INS), Global Positioning System (GPS), Intelligent Robot and so on. The market demand of gyroscope is very large [4-6]. With the need of high performance and high resolution of quartz gyroscope, more attentions are pay at the low-pass filter in gyroscope's interface circuit [7-8].

Passive LC filter was used in gyroscope in early time and its inductance accounts for a large area which is difficult for integration. The RC filter has a good solution for this problem which has no inductance in the circuit. The active RC filter is easier to achieve integration. But integrated RC filter's performance is not high. Because its performance is related to resistance and capacitance, stability and precision of integrated resistance is very low in CMOS process. With the urgent need of the new integrated filter technology, switched capacitor filters came out.

Passive LC filter was used in gyroscope in early time. Though it has high stability, in low frequency range of applications its inductance accounts for a large area which is difficult for integration. The RC filter has a good solution for this problem which has no inductance in the circuit. And the active RC filter is easier to achieve integration. But integrated RC filter's performance is not high. If the stopband is very low, the resistor would be very large which would acquire large area. And its performance is related to resistance and capacitance, but stability and precision of integrated resistance are very low in CMOS process [9-10]. With the urgent need of the new integrated filter technology, switch-capacitor filters came out.

In the switch-capacitor filter, switch-capacitor structure is used to replace the resistor in the RC circuit. The switched capacitor filter's advantages include low power consumption, high levels of integration, high performance and high anti-interference ability [11]. The performance of such filter is determined only by the switching frequency and capacitor network. Accurate capacitance is easy to achieve in monolithic silicon and its manufacture precision can reach 0.01% [12-13]. Therefore, the switched-capacitor filter has great practical significance in quartz gyroscope interface circuit.

The remaining of this paper is organized as follow: section 2 gives the system-level analysis and design of fourth-order SCF, section 3 gives the design of circuit modules, section 4

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is the Computer Aided Design (CAD) simulation, section 5 shows the test result and discussion and last section a conclusion of this paper is given.

2. System-level Analysis and Design

In quartz gyroscope the requirements of the filter are: passband should be 100Hz, the maximum pass-band ripple should be less than 0.3dB, stopband should be 1KHz, and the minimum stopband attenuation should be bigger than 60dB. The common filter functions used frequently are Butterworth filter, Chebyshev filter and Elliptic filter. The amplitude characteristic of Butterworth filter decreases linearly, but the decreasing rate is very slow. Chebyshev filter's has a little ripple in stopband or passband. Both stopband and passband have ripples in Elliptic filter, but the its decreasing rate is the fastest. After consideration of pass-band ripple and stopband attenuation in this filter, 4th-order Chebyshev II filter is chosen.

The 4th-order switch-capacitor filter consists of two 2nd-order unit. In this project a common second-order module—Fleischer-Laker biquad filter architecture as Fig. 1 is used to constitute 4th-order filter. The transfer function of the Fleischer-Laker biquad filter architecture can be written as follows:

$$\frac{V_{out}^{e}(z)}{V_{in}^{e}(z)} = \frac{(DJ - AH)z^{-2} - [D(J+I) - AG]z^{-1} + DI}{(DB - AE)z^{-2} - [2DB - A(C+E)]z^{-1} + DB} \tag{1}$$

$$\frac{V_{1}^{e}(z)}{V_{in}^{e}(z)} = \frac{(EJ - BH)z^{-2} + [B(G+H) - E(I+J) - CJ]z^{-1} - [I(C+E) - GB]}{(DB - AE)z^{-2} - [2DB - A(C+E)]z^{-1} + DB} \tag{2}$$

In these equations, A, B, C, D, E, F, G and H are the capacitor ratios in circuit.

After determination of the order and filter type, based on the passband and stopband, by the Matlab design the poles and zeros are got. After an optimization of the poles and zeros for the circuit realization, the poles and zeros of the filter transfer function are:

$$\text{Zeros} = \begin{cases} 0.97 + 0.06j \\ 0.97 - 0.06j \\ 0.95 + 0.03j \\ 0.95 - 0.03j \end{cases} \qquad \text{Poles} = \begin{cases} 0.97 + 0.06j \\ 0.97 - 0.06j \\ 0.95 + 0.03j \\ 0.95 - 0.03j \end{cases} \tag{3}$$

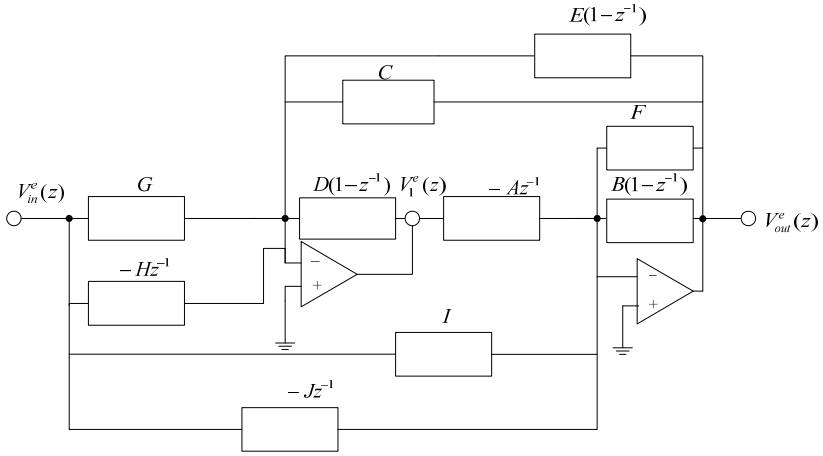

Figure 1. Topology of Fleischer-Laker biquad filter architecture

Then make the poles and zeros pair. The pairing should follow the principle: the poles closest to the unit circle in z-plane have the highest priority to pair with the closest zeros [7]. Through this way it gets two second-order transfer function as follows:

$$\begin{cases} H_1 = \dfrac{G_1(1-0.6z^{-1}+0.9z^{-2})}{(1-1.9z^{-1}+0.9034z^{-2})} \\ H_2 = \dfrac{G_2(1-0.8z^{-1}+0.97z^{-2})}{(1-1.94z^{-1}+0.94455z^{-2})} \end{cases} \quad (4)$$

where $G_1 \times G_2 = 0.0000102$. The value of G_1 and G_2 influence the value of capacitors in circuit. In circuit a large capacitor ratio is not wanted, it is better for values of G_1 and G_2 closed to each other [8]. So this paper choose $G_1 = G_2$ =0.0032. The transfer function of this 4th-order switch-capacitor filter can be written as follows:

$$H = H_1 * H_2 = \frac{0.0032(1-0.6z^{-1}+0.9z^{-2}).(1-0.8z^{-1}+0.97z^{-2})}{(1-1.9z^{-1}+0.9034z^{-2}).(1-1.94z^{-1}+0.94455z^{-2})} \quad (5)$$

Through Matlab simulation of the transfer function, amplitude characteristic curve and phase characteristic curve are shown in Figure 2 and Figure 3. In Figure 2 and 3, H represents the amplitude and phase characteristics of the whole 4th-order filter. H1 and H2 representing the first stage and second stage. It can be got from the Figures that 4th-order the low-pass filter is smooth within the passband and the passband ripple is almost non-existent. The passband cutoff frequency is 100Hz, stopband cutoff frequency is 1KHz, and the stopband minimum attenuation is about 83.5dB. The phase varies linearly within the passband. The ideal model simulation meets the expected targets.

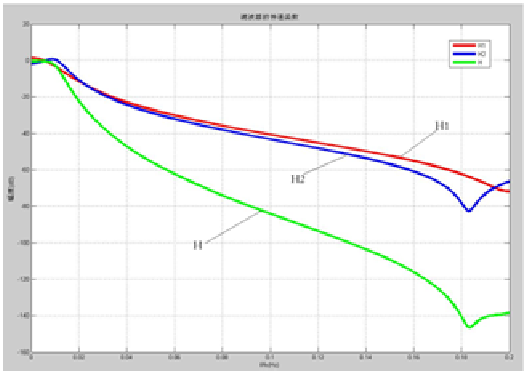

Figure 2. Amplitude characteristic curve in system- level simulation

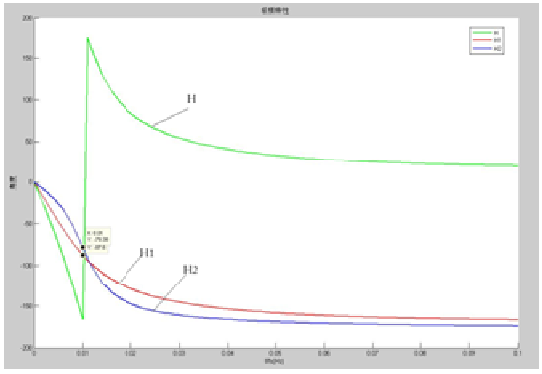

Figure 3. Phase characteristic curve in system-level simulation

3. Design of Circuit Modules

3.1. Amplifier Design

Amplifier is a very important part in the whole switch-capacitor filter. High linearity of amplifier is needed to achieve a good performance of filter, so the DC gain of amplifier should be high. To achieve high gain, a proper structure should be chosen. The amplifier used in this filter is a folded cascade two-stage structure as Fig.4. The folded cascade two-stage structure can fulfill the request of gain. The DC gain is:

$$A_{DC} = g_{m1}.(g_{m6}r_{ds6}r_{ds4} \parallel r_{ds8}).g_{m15}.(r_{ds15} \parallel r_{ds16}) \quad (6)$$

where g_{m1}, g_{m6} and g_{m15} are the transconductance of M1, M2 and M15. r_{ds6}, r_{ds8}, r_{ds15} and r_{ds16} are the drain-source resistors of M4, M8, M15 and M16.

A high slew rate is required for a fast capacitor charging. The second stage employs the current mirror. The output MOSFET M15 is driven by first stage's output and the output stage works in Class AB to increase slew rate which is determined by current of first stage and compensated capacitor C_1 . The compensated capacitor C_1 is used to realize a good phase margin. The sample frequency in this filter is 20KHz. So the gain bandwide (GBW) of amplifier should be several times of sample frequency. This structure can realize the high gain bandwide and high gain. The GBW of the amplifier is:

$$GBW = \frac{g_{m1}}{C_1} \tag{7}$$

From the simulation result of the amplifier in Figure 5 it is got that GBW is 41.6MHz when the load capacitor is 10PF, Phase Margin is 62°and gain is 80.4dB.

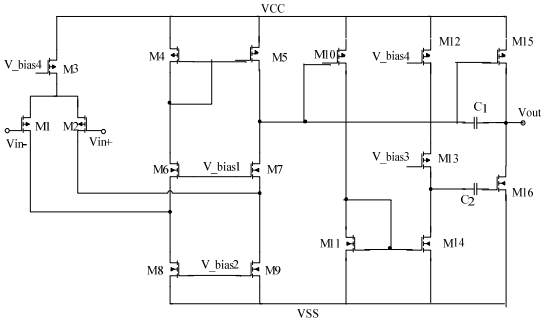

Figure 4. Structure of amplifier

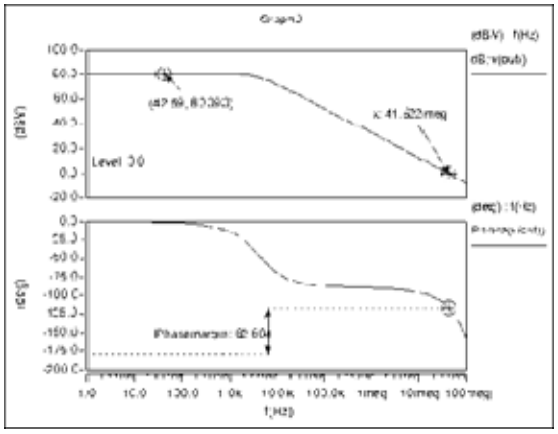

Figure 5. Bode diagram of amplifier

3.2. Switch Design

Switches generally use CMOS to realize the complementary switch. If only the PMOS or NMOS used in switch, the on-resistance would be very large. In switch capacitor circuit charge injection effect would seriously damage the work of filter. So the design of switch uses six CMOS transmission gate switch structure to suppress the charge injection effect, as shown in Figure 6.

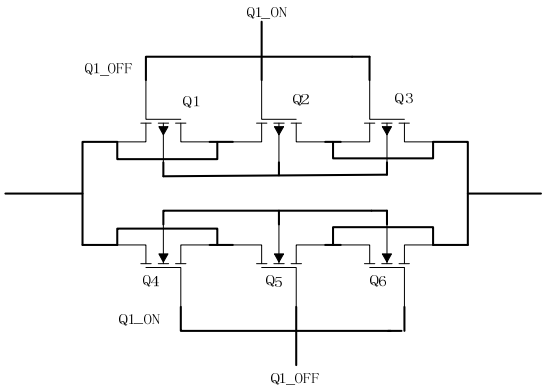

Figure 6. Structure of Switch

Width of *Q1*, *Q3* is half of *Q2* and width of *Q4*, *Q6* is half of *Q5*. When the clock signal is coming, the middle tubes inject positive (negative) charge, but both sides of the tubes driven by a reverse clock signal produce an equal amount of negative (positive) charge, which greatly offsets the channel charge injection effect. In practical application, the charge injection effect can't counteract completely, but can be weakened greatly.

3.3. Clock Design

The switches in filter are controlled by two 20KHz non-overlapping clocks. The two-phase non-overlapping clocks in filter are generated by an input clock source. The input clock is divided by two branches. In order to prevent overlapping, NAND gate and inverter are placed on each branch road. The design of the non-overlapping clock generating circuit is shown in Figure 7: clk is the input clock, ϕ_1, ϕ_2 is a pair of non-overlapping clock.

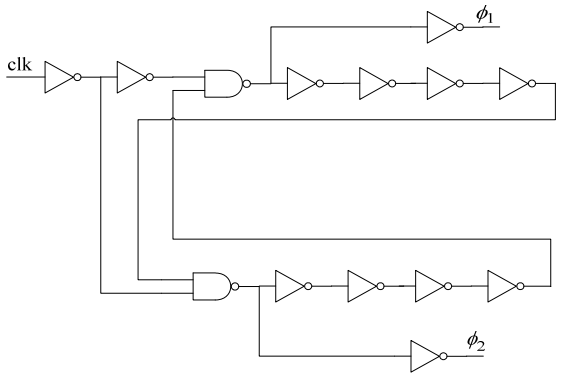

Figure 7. Clock generator

4. Simulation and Discussion.

The 4th-order SCF system is simulated by 0.5um CMOS process as Figure 8. The capacitor ratio of the circuit is same as factors in Eq.(5). By the Cadence Spectre AC simulation, Figure 9 shows the amplitude characteristic curve. And it is got that passband cut-off frequency is 99.7Hz and stopband attenuation is -78.6dB at 1KHz.

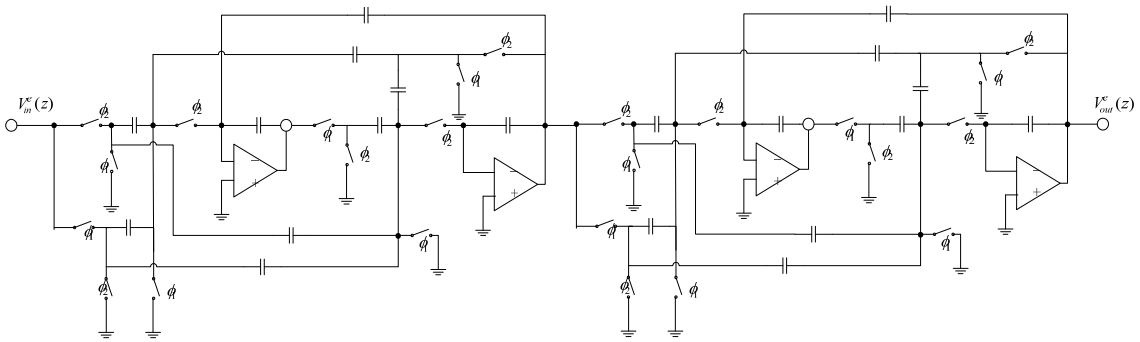

Figure 8. Circuit of the whole 4th-order SCF system

From Figure 10 the system phase characteristic curve, it is got that phase changes linearly in passband. Figure 11 shows the passband ripple is about 0.14dB.

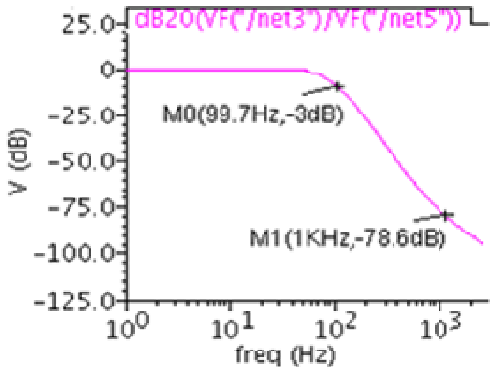

Figure 9. Amplitude characteristic curve in circuit simulation Figure

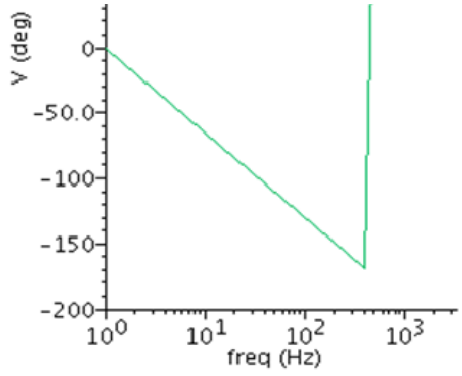

Figure 10. Phase characteristic curve in circuit simulation

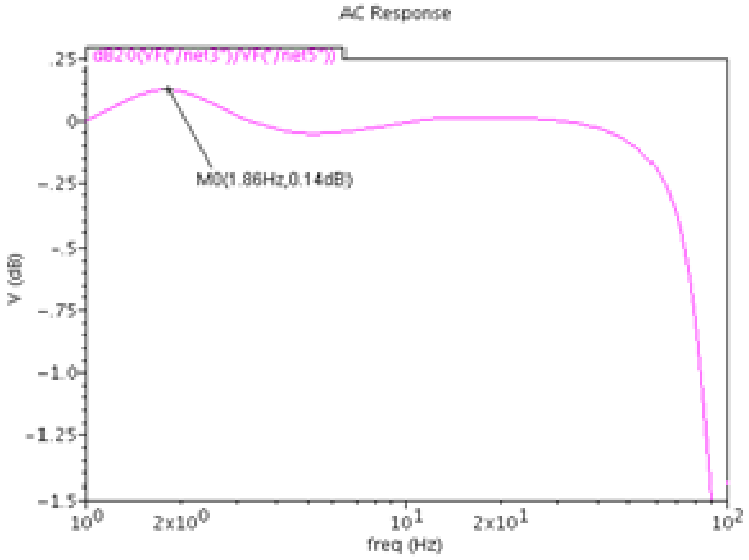

Figure 11. Passband ripple in circuit simulation

In contrast with the system-level of the filter system, the circuit simulation has a pass band ripple around 0.14dB, and its stopband attenuation at 1KHz less than ideal simulation by 8dB. And its phase characteristic curve has a small amount of offset. But these differences are inevitable in circuit design. So these should be taken into consideration in system-level design.

5. Test and Discussion

The switch-capacitor filter designed as above is fabricated in CMSC 0.5um CMOS process. The test PCB of switch-capacitor filter is shown as Figure 12. In the test PCB there is an oscillator to supply a 2GHz input clock. The 2GHz input clock would be divided by clock generator to create the 20KHz control clock.

The input signal is gotten by a signal generator. The input amplitude is fixed at 1V. But the input frequency is changed to get the amplitude characteristic of switch-capacitor filter chip. The frequency of input signal is chosen from 1Hz to 1KHz. Figure 13 is the test result of switch-capacitor filter's amplitude characteristic. The test result is almost same as the simulation of CAD software Cadence Spectre, that passband is almost 100Hz, ripple in passband is very little and stopband attenuation at 1KHz is almost -80dB.

Figure .12 Test PCB of SCF Chip

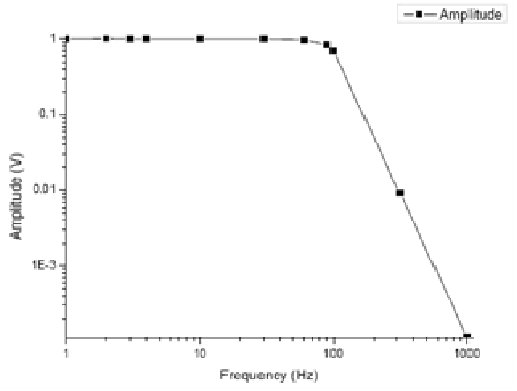

Figure 13. Test amplitude characteristic of SCF Chip

6. Conclusion

With the advancement in networking and multimedia technologies enables the distribution and sharing of multimedia content widely. In the meantime, piracy becomes increasingly rampant as the customers can easily duplicate and redistribute the received multimedia content to a large audience. critical [1]. Although encryption can provide multimedia content once a piece of digital content is decrypted, the dishonest customer can redistribute it arbitrarily.

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