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Low power architecture of logic gates using adiabatic techniques

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ABSTRACT

The growing significance of portable systems to limit power consumption in ultra-large-scale-integration chips of very high density, has recently led to rapid and inventive progresses in low-power design. The most effective technique is adiabatic logic circuit design in energy-efficient hardware. This paper presents two adiabatic approaches for the design of low power circuits, modified positive feedback adiabatic logic (modified PFAL) and the other is direct current diode based positive feedback adiabatic logic (DC-DB PFAL). Logic gates are the preliminary components in any digital circuit design. By improving the performance of basic gates, one can improvise the whole system performance. In this paper proposed circuit design of the low power architecture of OR/NOR, AND/NAND, and XOR/XNOR gates are presented using the said approaches and their results are analyzed for power-dissipation, delay, power-delay-product and rise time and compared with the other adiabatic techniques along with the conventional complementary metal oxide semiconductor (CMOS) designs reported in the literature. It has been found that the designs with DC-DB PFAL technique outperform with the percentage improvement of 65% for NOR gate and 7% for NAND gate and 34% for XNOR gate over the modified PFAL techniques at 10 MHz respectively.

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1. INTRODUCTION

Energy consumption is a crucial parameter in ultra large scale integration (ULSI) technology. Presently, many electronic devices are portable, compact and show high performance. The reduction in power dissipation is the most important factor for achieving higher performance with high density. In complementary metaloxide semiconductor (CMOS) circuits, several new approaches are emerging to achieve low power consumption. When timing requirement is not crucial, adiabatic logic is the most outstanding approach amidst the various techniques to lessen the power consumption in CMOS circuits [1]. Adiabatic logic suggests the make use of a trapezoidal power clock that permits charging or discharging at a steady current without current flow. Therefore, lesser amount of energy is dissipated by adiabatic circuits [2]. Adiabatic logic works on alternating current supplies instead of direct current, which makes the recycling of energy in the circuit [3].

Adiabatic logic is a unique technique for creating logical circuits that assures exceptional density and very less power consumption. Bennett first proposed this technique in 1992 and declared that the energy

could in principle be saved and used again. A significant amount of research has been accomplished on logic circuit design using the adiabatic techniques. The complementary pass logic adiabatic gated (CPLAG) XOR gate designed with an asynchronous reset facility [4]. Adiabatic computing for CMOS integrated circuits was presented, which is based on the dual threshold CMOS and gate length biasing approach [5]. NAND/NOR gate are deisgned based on positive feedback adiabatic logic (PFAL) and two phase clocked adiabatic static CMOS logic (2PASCL) techniques [6]. Two phase adiabatic dynamic logic (2PADL) is used to design a carry lookahead adder which has the advantages of energy efficiency and lower switching power due to the usage of gate overdrive because of this feature it can be used in a variety of low-power very large scale integrated (VLSI) designs [7]. Further, energy efficient different gates are design using various adiabatic approach like CMOS, 2N2P, efficient charge recovery logic (ECRL) and PFAL adiabatic logic for low power applications [8]. A energy efficient AND/NAND and XOR/XNOR gates and carry lookahead adder are designed using noval charge sharing improved pass gate adiabatic logic (CSIPGL) technique which is operating uses four-phase power clock sources [9]. In recent years, much investigation has been reported on the design of inverter [10], gates [11]-[16], adder [17]-[22], subtractor [23], multiplexers [24], [25] and flip flops [26]-[28]. The circuits that dissipate more heat and consume more power need expensive cooling alternative, resulting in higher device costs. The adiabatic logic approach have been asserted as a possible means for energy recovery. Logic gates are the fundamental units of any digital system and thus, this paper aims at designing high performance gates which can improve the overall system performance. Moreover, MPFAL and direct current diode based positive feedback adiabatic logic (DC-DB PFAL) adiabatic approaches result into ultra low power circuit which is the need of current electronics era.

This paper presents the design of low power OR/NOR, AND/NAND, and XOR/XNOR gates using Modified PFAL and DC-DB PFAL techniques. Further, the comparative analysis of these techniques with the other adiabatic techniques such as ECRL, PFAL and with the conventional CMOS approach is carried out to investigate the performance metrics of gates under study. For analysis, 45 nm technology nodes are used with the supply voltage of 0.8V.

The remainder of this paper is organized as follows. Section 2 presents the basics of adiabatic logics. The design of proposed logic gates using adiabatic techniques are is presented in section 3. Sections 4 and 5 discuss the comparative analysis and results respectively. The paper is concluded in section 6.

2. ADIABATIC LOGIC

Adiabatic logic circuits have been emphasized for having an energy recovery principle. The term "adiabatic" states to a process in which a thermodynamic system interacts with its environment without transferring heat or matter. These circuits have three conditions as follows [12].

a) When there is a large voltage difference between the drain and source terminals, the transistor should be switched off.
b) When current is flowing through the transistor, it should be turned on.
c) Never pass current through diode.

Adiabatic logic has a very low energy dissipation, but at the cost of complex circuitry Adiabatic circuits are classified into two types that are fully and quasi-adiabatic. Quasi-adiabatic circuits undergo from some adiabatic loss due to current leakage caused by non-ideal switches, but these are easier to design hence, are preferred over fully adiabatic circuits.

2.1. Power dissipation in adiabatic circuits

In conventional CMOS logic, power consumption happens during the charging and discharging of the circuit. In CMOS circuits, a constant voltage is employed as a source, in which the energy is transferred from the power supply to the output node. Due to switching events, the energy from the output node travels to the ground.

In low-power circuits, adiabatic logic employs reversible logic to reduce power dissipation by using residual energy and improves the energy efficiency. Instead of static operating voltage, a trapezoidal power clock signal is used to retrieve the signal energy. In adiabatic logic, a constant current supply is utilized instead of a constant voltage supply to charge the load capacitance. Figure 1 depicts adiabatic charging and discharging.

The current ($i_c(t)$) and energy (E_c) during charging is given by (1) and (2).

$$i_c(t) = C_{load} dV_c/dt = C_{load} V / T \quad (1)$$

$$E_c = (i_c^2 * R) * T \quad (2)$$

Where, R is the resistance and T is the voltage ramp period, V is the swing of the supply voltage.

The charge holding in the load capacitor is often reused AC type instead of DC. If the T> RC_{load} then charging the circuit time constant ($2RC_{load}$) is much smaller than T, since the energy dissipation is small. The dissipation of energy is decreased by decreasing the PMOS transistor on-resistance as the dissipated energy ($E_{adiabatic}$) is proportional to R and is given by (3) and (4) [1].

$$E_{adiabatic} = (i_c^2 * R) * T \quad (3)$$

$$E_{adiabatic} = R * C_{load}^2 * V^2/T \quad (4)$$

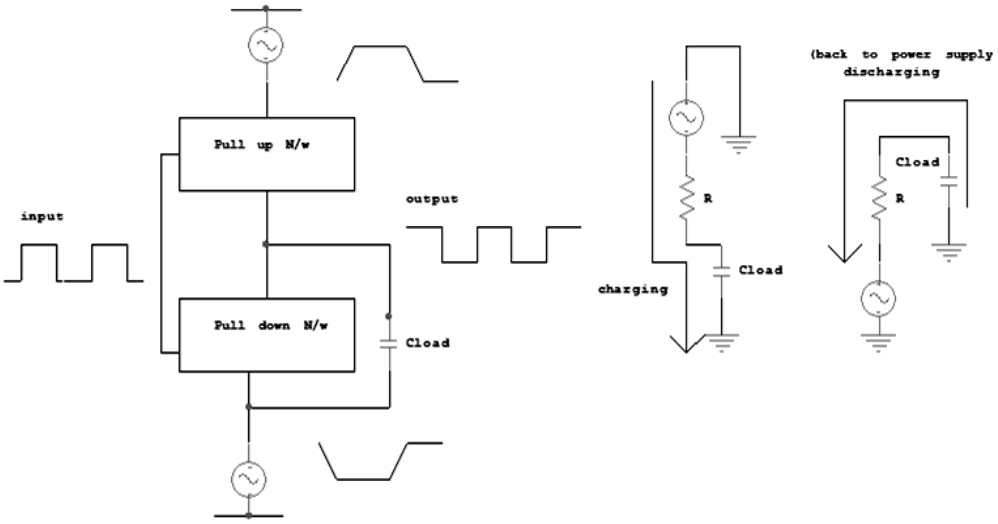

Figure 1. Adiabatic charging and discharging

3. IMPLEMENTATION OF LOGIC GATES USING DIFFERENT ADIABATIC TECHNIQUES

To limit energy loss from the circuit, adiabatic techniques are employed. These techniques use the trapezoidal waveform which has a crucial role in charge recovery. The clock has 4-phases that are evaluation, hold, recovery and wait. The junction capacitance charge and logic are evaluated during the evaluation phase and during the hold phase; the logic is retained and used as input for the next stage. The drawn power is returned to the source, during recovery phase. The circuit waits for the logic from the previous stage to be calculated in the waiting phase [29]. This section presents the design of low power logic gates such as OR/NOR, AND/NAND and XOR/XNOR using modified PFAL and DC-DB PFAL. For the analysis, 'In1' and 'In2' are taken as input voltage signals, Vpc is the power clock, and 'out' is the output voltage signal.

3.1. Design of basic gates using MPFAL

This section describes the design of the logic gates using a modified PFAL technique. The modified PFAL comprises a positive source of DC voltage (V_{dc}) between the source and ground terminal of a pair of cross-coupled inverters (M1, M3) and (M2, M4). In comparison to the traditional PFAL, these changes ensure the minimum dissipation of power in the circuit. The simulations are run at V_{dc} of 0.1 V. The designs under consideration are shown in Figures 2-4.

Simulations are run at 10 MHz frequency and results are obtained as shown in Table 1. NOR gate shows the power dissipation of 12.1 nW, delay of 31700 ps and delay power product of 385 aJ. Further, NAND gate shows the power dissipation of 2.83 nW, delay of 27600ps, and the power delay product of 78 aJ, while XNOR gate shows the power dissipation of 10.31 nW, delay of 6840 ps and the power delay product of 70.41 aJ, where abbreviation aJ stands for Auto Joule.

For comparative analysis, result is obtained through simulations at 10 MHz for the gates under study using conventional CMOS approach and the other two adiabatic techniques i.e. ECRL [30], [31] and PFAL [32], [33] as shown in Table 1. For other frequencies, the results are given in Table 2. The rise time comparison of basic gates is shown in Table 3.

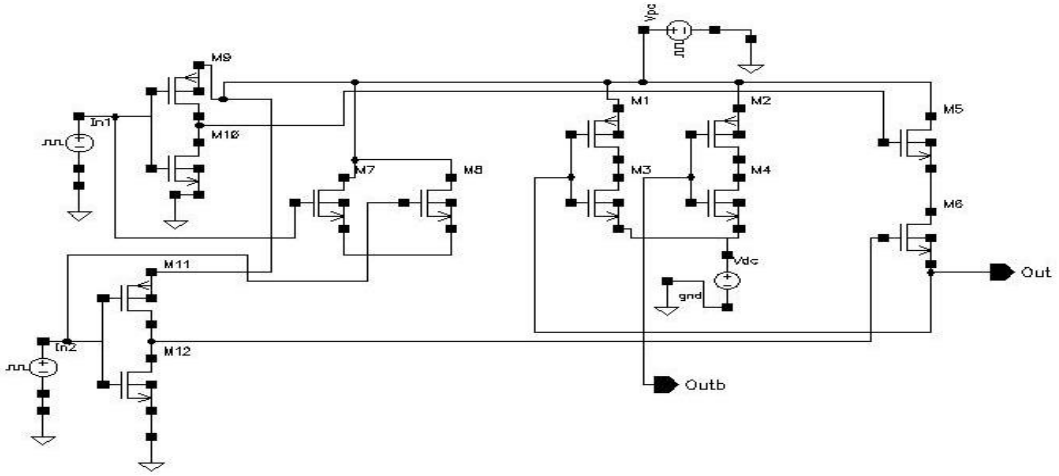

Figure 2. NOR/OR gate design based on modified PFAL

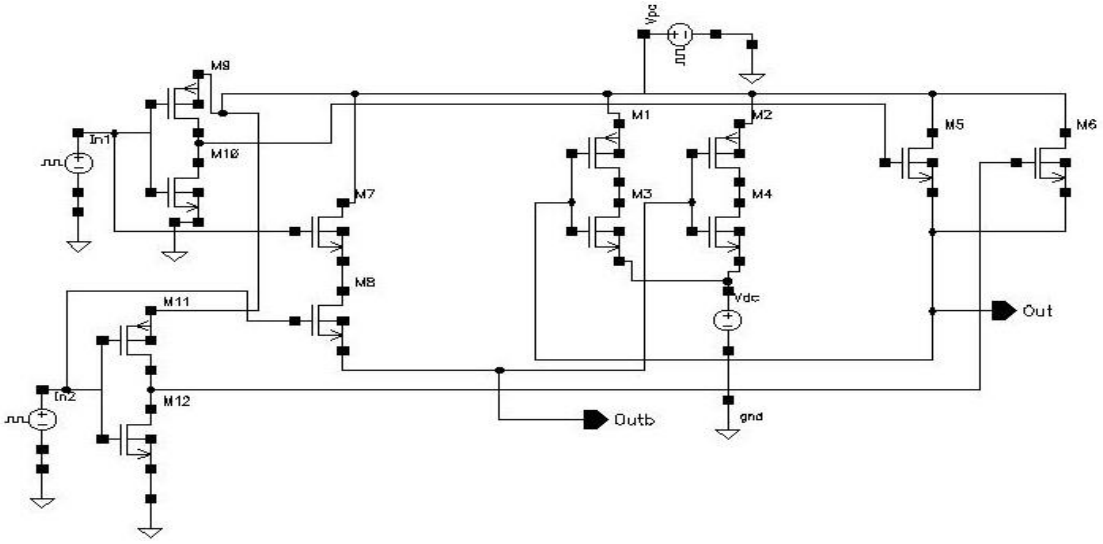

Figure 3. NAND/AND gate design based on modified PFAL

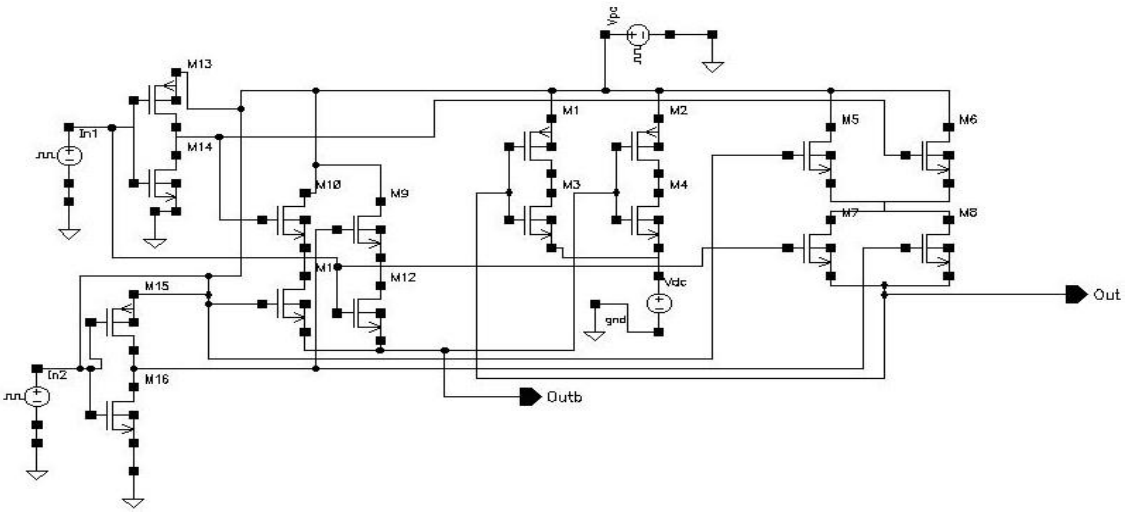

Figure 4. XNOR/XOR gate design based on modified PFAL

3.2. Design of basic gates using DC-DB PFAL

The modified PFAL approach can be further extended to lessen the consumption of power by using a new approach that is DC-DB PFAL. As illustrated in Figure 5, the DC-DB PFAL circuit consists of a DC voltage source (V_{dc}) connected between the source and ground terminal of (M1, M3) and (M2, M4) PFAL latch and pull-down block with an NMOS diode (M13). The diode at the bottom of the PFAL latch allows for easy control of the discharge path by lowering the discharge rate of the circuit's internal nodes, as well as level shifting. As a result of the level shifting, the leakage current of the output transistor and the gate to source voltage are reduced. Here, the NMOS diode operates in a saturation region, and thus, the current through the NMOS diode is given by (5).

$$I_{ds} = K (V_{gs} - V_t)^2 = K(V_{ds} - V_t)^2 \quad (5)$$

Where, K is the constant, drain to source current (I_{ds}), gate to source voltage (V_{gs}), drain to source voltage (V_{ds}) and threshold voltage (V_t). By applying a positive voltage (V_{dc}) of 0.1 V to the NMOS diode, V_{ds} is reduced. This, in turn, reduces the voltage drop ($V_{ds} - V_t$), and hence, I_{ds} also decreases. As a result, power dissipation is also minimized. Hence, DC-DB PFAL is the most power-efficient technique compared with other adiabatic methods. The design of NOR/OR, NAND/AND, and XNOR/XOR gates using the DC-DB technique are shown in Figures 5-7, respectively.

Simulations are run and results are obtained as shown in Tables 1-3. At 10 MHz frequency, NOR gate shows a power dissipation of 22 nW, delay of 5.68 pS and power delay product of 0.024 aJ. For NAND gate, the result shows a power dissipation of2.63 nW, delay of 4990 ps and power delay product of 13.1 aJ. However, XNOR gate shows the dissipation of power 2.82 nW, delay of 20000 ps and power delay product 56.41 aJ. The comparison of the results with the other techniques is shown in Tables 1 and 2.

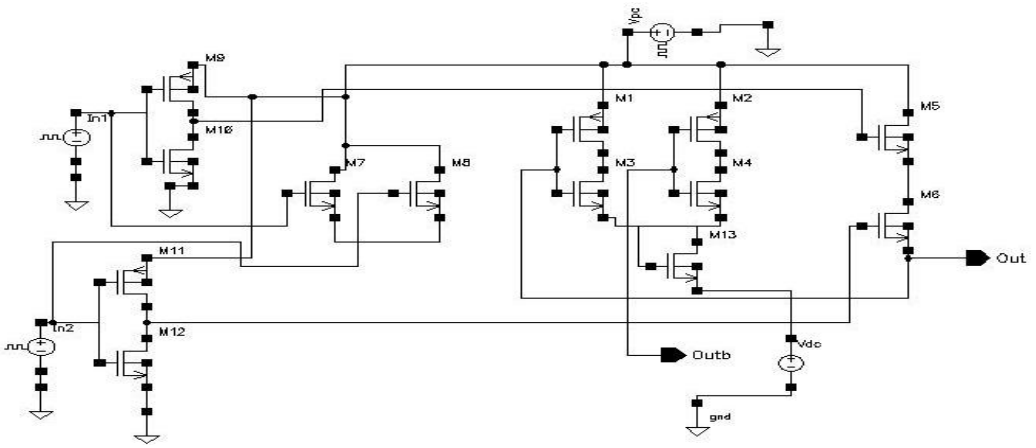

Figure 5. NOR/OR gate design based on DC-DB PFAL

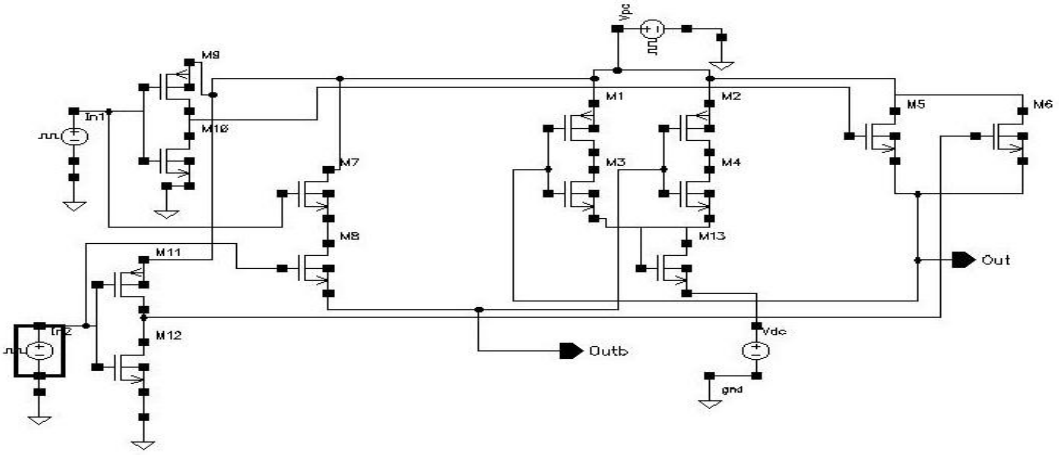

Figure 6. NAND/AND gate design based on DC-DB PFAL

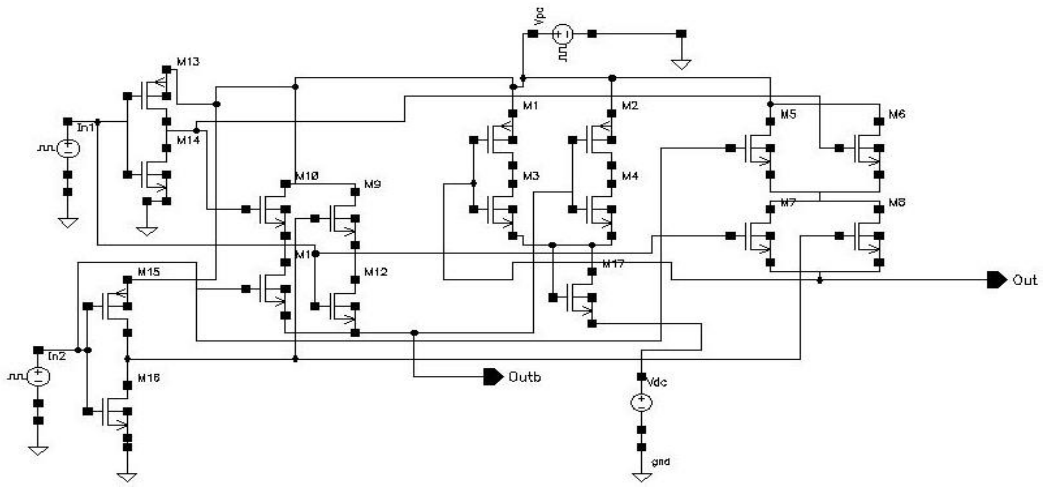

Figure 7. XNOR/XOR gate design based on DC-DB PFAL

4. COMPARATIVE ANALYSIS OF PROPOSED DESIGNS USING VARIOUS APPROACHES

This section presents a comparative analysis of different approaches for the proposed gates. The circuits of gates under study are simulated using different techniques to study the performance matrices such as power delay product and power dissipation by varying frequencies, rise time, and critical propagation delay. Table 1 illustrates the comparison of power delay product for proposed designs with other approaches. Further, Tables 2 and 3 show a comparative study of power dissipation at different frequencies and rise time respectively for the gates under study.

Table 1. Performance analysis of proposed gates for different adiabatic techniques including conventional approach at 10 MHz

Gate Types	Various Techniques	Power Dissipation (Nano Watts)	Delay(Pico Sec)	Power Delay Product (Atto Joule)
NOR	Conventional NOR gate	651	17.2	11.2
	ECRL NOR gate	12.3	79.1	0.009
	PFAL NOR gate	19.2	9500	182
	Modified PFAL NOR gate	12.1	31700	385
	DC-DB PFAL NOR gate	4.22	5.68	0.024
NAND	Conventional NAND gate	372	5250	1950
	ECRL NAND gate	4.51	25000	113
	PFAL NAND gate	4.01	9830	39.6
	Modified PFAL NAND gate	2.83	27600	78
	DC-DB PFAL NAND gate	2.63	4990	13.1
XNOR	Conventional XNOR gate	778	15800	12300
	ECRL XNOR gate	7.81	31500	246
	PFAL XNOR gate	5.77	5830	33.6
	Modified PFAL XNOR gate	10.31	6840	70.41
	DC-DB PFAL XNOR gate	2.82	20000	56.41

Table 2. Power dissipation of proposed gates for different adiabatic techniques including conventional approach at different frequencies

Gate Types	Various Techniques	Power dissipation (Nano Watts)		
		At 10 MHz	At 100 MHz	At 500 MHz
NOR	ECRL	12.3	14.16	2.975
	PFAL	19.2	18.22	5.156
	Modified PFAL	12.1	17.32	71.25
	DC-DB PFAL	4.22	3.191	0.7687
NAND	ECRL	4.51	5.649	0.8787
	PFAL	4.01	521.9	1.065
	Modified PFAL	2.83	3.39	10.65
	DC-DB PFAL	2.63	3.258	0.8356
XNOR	ECRL	7.81	5.13	1.927
	PFAL	5.77	5.734	1.905
	Modified PFAL	10.3	17.06	85.77
	DC-DB PFAL	2.82	3.55	0.8411

Table 3. Rise time of proposed gates for different adiabatic techniques including conventional approach at 10 MHz

Gate Types	Various Techniques	Rise Time (Femto sec.)
NOR	Conventional	242
	ECRL	10.7
	PFAL	1260
	Modified PFAL	154
	DC-DB PFAL	1.38
NAND	Conventional	10800000
	ECRL	324
	PFAL	0.0499
	Modified PFAL	1430
	DC-DB PFAL	0.598
XNOR	Conventional	242
	ECRL	88.4
	PFAL	570
	Modified PFAL	649
	DC-DB PFAL	1.38

Another significant parameter of the CMOS circuits is chip density that depends on the transistors count. Figure 8 shows the comparative investigation of transistor count in conventional CMOS approach and in different adiabatic techniques used for the proposed gates. It is observed that the DC-DB PFAL adiabatic logic approach uses additional transistors than conventional CMOS approach. However, at the same time, DC-DB PFAL consumes less power compared to the standard CMOS approach.

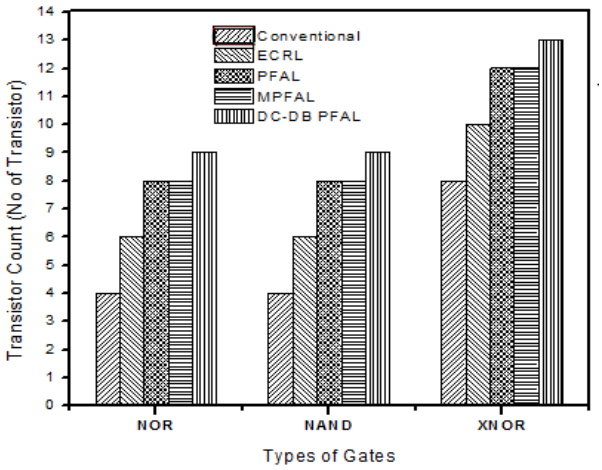

Figure 8. Comparison of transistors count for proposed gates using different techniques

5. RESULT ANALYSIS

This paper presents the design of low power architectures by modified PFAL and DC-DB PFAL adiabatic techniques. The performance analysis is carried and the results are compared with the other adiabatic techniques including the conventional technique for the parameters such as power dissipation, delay, power-delay product, rise time and transistor count. When the power dissipation is analyzed for various proposed gates such as NAND, NOR and XNOR, it has been found that the designs with DC-DB PFAL technique outperform with the percentage improvement of 68%, 78%, and 65% for NOR gate, 41%, 34%, and 7% for NAND gate and finally of 64%, 51%, and 34% for XNOR gate over the other techniques like ECRL, PFAL and modified PFAL techniques at 10 MHz respectively.

Also, it has been noticed that the consumption of power in DC-DB PFAL gate is further reduced when the circuits are operated in the range of 100 to 500 MHz. Therefore, the power dissipation of modified PFAL is increased in the mentioned operating frequency range. A comparative analysis of these techniques is shown in Table 2. Thus, DC-DB PFAL method excels among other adiabatic techniques when investigated for power consumption.

Moreover, propagation delay is one of the vital performance metrics when speed is concerned. In case of DC-DB PFAL, the delay in NOR gate is found lesser as compared to delay of NOR gates using other adiabatic techniques while NAND and XNOR gates designs using DC-DB PFAL have increased delay, as shown in Table 1. Further, the next essential parameter to check the functionality of basic gate is the power delay product. The assessment of power delay product for presented designs implies that the NOR, NAND

and XNOR gate designs with DC-DB PFAL implementation perform 99%, 83%, and 20% better than their MPFAL counterpart as given in Table 1.

Table 3 presents the rise time for various proposed gate designs with all the adiabatic structural methods. Finally, the transistor count is carried out for all the gates under study. The DC-DB PFAL methods require ore transistors when investigated with other methods as shown in Figure 8.

6. CONCLUSION

The aim of the electronic design is to retain a balance between the speed and power efficiency. This paper explores the design and detailed investigation of OR/NOR, AND/NAND, and XOR/XNOR gates using modified PFAL, and DC-DB PFAL adiabatic techniques. Further, the results are compared with other adiabatic techniques and the conventional CMOS approach. It is observed that the DC-DB PFAL style achieves the best performance among rest of the techniques. Further, a comprehensive analysis of the proposed circuits is carried out to examine various performance parameters. It is also demonstrated that the designs of NOR, NAND, and XNOR gates using DC-DB PFAL have an improvement of 65%, 7%, and 72% respectively, in power dissipation as compared to the similar circuits when designed using Modified PFAL. Further, the power–delay product of NOR, NAND, and XNOR gates using the DC-DB PFAL technique exhibit an improvement of 99%, 83%, and 20% respectively, as compared to their modified PFAL counterparts. In techniques such as conventional CMOS, ECRL, PFAL, Modified PFAL, the best performance parameters are attained by modified PFAL. Finally, it is concluded that the DC-DB PFAL style is valuable in applications where power saving is of primary importance. These applications include high-performance battery-operated digital portable systems for ultra-low-power devices in cardiac pacemakers, hearing aids, notebook computers, mobile phones, and digital aids.

REFERENCES

[1] D. Jayanthi, A. B. Shankar, S. Raghavan, and G. Rajasekar, "High speed multioutput circuits using adiabatic logic," in *Proc. IEEE International Conference on Emerging Trends in Engineering, Technology and Science*, October 2016, pp. 436-442, doi: 10.1109/ICETETS.2016.7603058.

[2] W. C. Athas and L. J. Svensson, "Reversible logic issues in adiabatic CMOS," in *Proc. IEEE Workshop on Physics and Computation*, Nov. 1994, pp. 111-118, doi: 10.1109/PHYCMP.1994.363692.

[3] N. Anuar, Y. Takahashi, and T. Sekine, "Two phase clocked adiabatic static CMOS logic and its logic family," *Journal of Semiconductor Technology and Science*, vol. 10, no. 1, pp. 1-10, 2010, doi: 10.5573/jsts.2010.10.1.001.

[4] M. Sharma and A. Noor, "CPL-Adiabatic Gated logic (CPLAG) XOR gate," in *Proc IEEE International Conference on Advances in Computing, Communications and Informatics*, Aug. 2013, pp. 575-579, doi: 10.1109/ICACCI.2013.6637236.

[5] W. Zhang, J. Hu, and L. Yu, "Adiabatic Computing for CMOS Integrated Circuits with Dual Threshold CMOS and Gate Length Biasing Technique," *Journal of Information Technology*, pp. 2392-2398, 2011, doi: 10.3923/itj.2011.2392.2398.

[6] A. K. Maurya and G. Kumar, "Adiabatic Logic : Energy Efficient Technique for VLSI Applications," in *Proc IEEE international Conference on Computer & Communication Technology*, Sept. 2011, pp. 234-238, doi: 10.1109/ICCCT.2011.6075164.

[7] P. Sasipriya and V. S. K. Bhaaskaran, "Design of Low Power VLSI Circuits Using Two Phase Adiabatic Dynamic Logic (2PADL)," *Journal of Circuits, Systems and Computers*, vol. 27, no. 04, 2017, doi: 10.1142/S0218126618500524.

[8] A. Anitha, S. Rooban, and M. Sujatha, "Implementation of energy efficient gates using adiabatic logic for low power applications," *International Journal of Recent Technology and Engineering*, vol. 8, no. 3, pp. 3327-3332, 2019, doi: 10.35940/ijrte.C4982.098319.

[9] A. L. Bhalerao, A. Mane, K. Pensenwar, B. P. Bhuvana, A. Anita Angeline, and V. S. K. Bhaaskaran, "Design of energy efficient carry lookahead adder using novel CSIPGL adiabatic logic circuit," *Journal of Physics: Conference Series*, vol. 1716, no. 1, 2021, pp. 1-7, doi: 10.1088/1742-6596/1716/1/012033.

[10] S. Soundar, T. Muthumanickam, T. Sheela, G. Ramachandran, C. A. Madhuvappan, and G. Sureshkumar, "Design of Power Efficient Logic Circuit using Adiabatic Technique," *Proteus Journal*, vol. 11, no. 7, pp. 178-188, 2020.

[11] A. Nicholas *et al.*, "Designing elementary-tree space compressors using AND/NAND and XOR/XNOR combinations," in *Proc IEEE Instrumentation and Measurement Technology Conference*, Jul. 2015, pp. 1408-1413, doi: 10.1109/I2MTC.2015.7151482.

[12] A. Nandal and D. Kumar, "A Study on Adiabatic Logic Circuits for Low Power Applications," *International Journal of Engineering Research & Technology*, vol. 5, no. 3, pp. 1-7, 2013.

[13] Y. Gupta and T. N. Sasamal, "Implementation of reversible logic gates using adiabatic logic," in *Proc IEEE Power, Communication and Information Technology Conference*, Oct. 2015, pp. 595-598, doi: 10.1109/PCITC.2015.7438067.

[14] M. Sharma, "Adiabatic logic based circuit optimization for ultralow power applications," *Journal of Information and Optimization Sciences*, vol. 41, no. 1, pp. 85-98, 2020, doi: 10.1080/02522667.2020.1715560.

[15] A. G. Vaishiba and A. Durai, "Energy efficient adiabatic logic circuit for improve security in DPA resistant RFID," *Jornal of Physics: Conference Series*, vol. 1716, no. 1, 2021, doi: 10.1088/1742-6596/1716/1/012043.

[16] P. Chauhan and B. Krishan, "Design and Analysis of Various Gates using Efficient Charge Recovery Logic (ECRL)," *International Journal of Signal Processing Image Processing and Pattern Recognition*, vol. 10, no. 11, pp. 1-12, 2017, doi: 10.14257/ijsip.2017.10.11.01.

[17] P. Bhati and N. Z. Rizvi, "Adiabatic Logic: An Alternative Approach to Low Power Application Circuits," in *Proc IEEE International Conference On Electrical,Electronics and Optimization Techniques*, March 2016, pp. 4255-60, doi: 10.1109/ICEEOT.2016.7755521.

[18] M. R. Taheri, R. Akbar, F. Safaei, and M. H. Moaiyeri, "Comparative analysis of adiabatic full adder cells in CNFET technology," *Science Direct Engineering Science and Technology, an International Journal*, vol. 19, no. 4, pp. 21190-2128, 2016, doi: 10.1016/j.jestch.2016.08.007.

[19] S. A. Marina, T. S. Pradeepa, and A. Rajeswar, "Analysis of full adder using adiabatic charge recovery logic," in *Proc IEEE International Conference on Circuit, Power and Computing Technologies*, Aug. 2016, pp. 1-6, doi: 10.1109/ICCPCT.2016.7530184.
[20] S. Koniki, U. Somanaidu, S. Reddy, and K. Nehru, "High Speed Full Adder Design with Analog Switch Level Restoration Technique," *International Journal of Creative Research Thoughts*, vol. 6, no. 1, pp. 370-376, 2018, doi: 10.6084/m9.doi.one.IJCRT1802384.
[21] T. R. Daram, B. N. Sri, D. Indhuja, G. Manisha, and A. K. Rao, "Low Power Design Of Carry Look Ahead Adder by using Adiabatic Logic," *International Journal of Advanced Science and Technology*, vol. 29, no. 7, pp. 5271-5282, 2020.
[22] C. Venkatesh, A. Mohanapriya, and R. S. Anandhi," Performance Analysis of Adiabatic Techniques using Full Adder for Efficient Power Dissipation," *ICTACT Journal On Microelectronics*, vol. 04, no. 01, 2018, doi: 10.21917/ijme.2018.0090.
[23] M. Sanadhya and D. K. Sharma, "Design and implementation of full subtractor using different adiabatic techniques," in *Proc IEEE International Women Engineering Conference Electronics Computing Engineering*, Dec. 2020, pp. 102-106, doi: 10.1109/WIECON-ECE52138.2020.9397967.
[24] S. D. Turaga, E. A. Jyothi, and K. J. D. Sai, "Power Reduction Technique Using Adiabatic Logic," in *Proc IEEE International Conference on Circuit, Power and Computing Technologies*, March 2014, pp. 1284-1290, 2014, doi: 10.1109/ICCPCT.2014.7055018.
[25] A. Sharma, H. Sohal, and K. Sharma "Area and Power Analysis of Adiabatic 2x1Multiplexer Designon 65nm CMOS Technology," in *Proc IEEE Conference*, 2016, doi: 10.1109/WECON.2016.7993489.
[26] P. Chaudhary, B. K. Das, and S. Ahuja, "Design of Low Power Memory Cell Using D Flip Flop Under Adiabatic Reduction Technique," in *Proc IEEE 3rd International Conference on Signal Processing and Integrated Networks*, Feb. 2016, pp. 20-23, doi: 10.1109/SPIN.2016.7566655.
[27] M. Sharma and A. Noor, "Positive Feed Back Adiabatic Logic : PFAL Single Edge Triggered Semi-Adiabatic D Flip Flop," *African Journal of Basic& Applied Sciences*, vol. 5, no. 1, pp. 42-46, 2013, doi: 10.5829/idosi.ajbas.2013.5.1.1118.
[28] J. Praveen, M. Bhuvanesh, B. S. Nagarakshitha, H. K. Bhanupriya, and K. A. Kumar, "A Design and Implementation of Adiabatic Logic on Low Power Application Circuits," *International Journal of Advanced Science and Technology*, vol. 29, no. 7, pp. 10130-10140, 2020.
[29] A. Blotti, S. Borghese, and R. Saletti, "Single-Inductor Four-Phase Power-Clock Generator For Positive-Feedback Adiabatic Logic Gates," in *Proc IEEE Informatica*, Sept. 2002, pp. 533-536, doi: 10.1109/ICECS.2002.1046218.
[30] I. A. Pindoo, T. Singh, A. Singh, A. Chaudhary, and P. M. Kumar, "Power dissipation reduction using adiabatic logic techniques for CMOS inverter circuit," in *Proc 6th IEEE International Conference on Computing, Communications and Networking Technologies*, Jul. 2015, p. 35239, doi: 10.1109/ICCCNT.2015.7395216.
[31] R. Yadav, A. Bakshi, J. Chowdhury, and J. K. Das, "Adiabatic approach for charge restoration in low power digital circuits," in *Proc2nd IEEE International Conference on Inventive Systems and Control*, Jan. 2018, pp. 473-477, doi: 10.1109/ICISC.2018.8399117.
[32] M. Sharma and A. Noor, "Reconfigurable CPLAG and Modified PFAL Adiabatic Logic Circuits," *Journal of Advances in Electronics*, vol. 2015, pp. 1-10, 2015, doi: 10.1155/2015/202131.
[33] S. P. S. Kushawaha and T. N. Sasamal, "Modified positive feedback adiabatic logic for ultra low power adder," in *Proc 2nd IEEE International Conference on Computational Intelligence and Communication Technology*, Feb. 2016, pp. 378-381, 2016, doi: 10.1109/CICT.2016.80.

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