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Investigating low order harmonics of sinusoidal pulse width modulation with voltage closed loop control

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ABSTRACT

This paper investigates the low order harmonics of a simplified approach to generate high quality sinusoidal pulse width modulation (SPWM) waveform produced by voltage source inverter (VSI). Programmable interface controllers (PIC) microcontroller was chosen to produce the signals in Real time with voltage feedback to control the puls width during direct current (DC) link voltage reduction. The research considered simplicity, durability, and reliability as conditions. The proposed technique was successfully passed one of the biggest challenges which is time criteria presence due to execution time of the feedback loop and the transient time required for power electronics switches to turn fully off and on, known as dead time. The proposed technique can be considered as practical, high feasibility according to economic point of view and its accuracy to the input variables. The pseudocode, algorithm, and flowchart for closed loop real time voltage control to produce SPWM system using microcontroller was explained, illustrated and verified. The desired objectives were accomplished to achieve system that is able to generate high quality real-time SPWM with closed loop control.

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1. INTRODUCTION

Pulse width modulation (PWM) is widely used in power electronics to produce sinusoidal waveform (SPWM), this procedure allows to digitize the system so that the sequence of voltage pulses can be generated by the on and off stats of the power switches [1]. The pulse width modulation techniques in inverters have been the main choice in power electronics for decades, because of its circuit simplicity, excellent control stablility, small size and light weight [2], [3]. PWM in voltage source inverter (VSI) with different switching techniques are commonly used in industrial applications and many of these techniques are based on analogue scheme except only few used digital.

Recently, with the orientation for renewable energy, new control techniques were needed. These techniques should be applicable, reliable, and economical in constriction and in power consumption, these requirements can be fulfilled in proficient way with the help of using programmable interface controllers (PIC) microcontrollers with proper interface [4]–[7]. The inverter technology is becoming more exensive with the spread of renewable energy sources such as photovoltaic and wind generation [8], this spread compined with technological demand required a continouos improvement in the field [9]. Sinusoidal pulse width modulation (SPWM) waveform consists of sequence of pulses in both positive as well as negative. These pulses have fixed amplitude with adjustable switching intervals as shown in Figure 1. The aim is to generate a train of pulses that can reconstract the fundamental waveform with an exact amplitude and frequency.

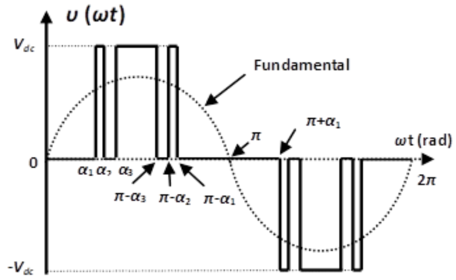

Figure 1. SPWM waveform

The assumption of symmetry around quarter of sine waveform, in Figure 1, guarantees that the even harmonics (2nd and 4th) will be zero, where all other harmonics will be either in phase or anti-phase with the fundamental. This assumption leads to admit that only odd harmonics do exist. Assuming that the PWM waveform is chopped times per half a cycle, the Fourier coefficients of odd harmonics are given by (1) [10]– [13].

$$f(wt) = \sum_{n=1,3,5...}^{\infty} bn \cdot \sin(nwt) \tag{1}$$

Where,

$$b_n = \frac{4V_{dc}}{n\pi} \sum_{n=1}^{\infty} \cos(nwt) \tag{2}$$

b_n: is the magnitude of the nth harmonic, n = 1, 3, 5… odd harmonic of angular frequency nω, while ω is the angular frequency of the fundamental component and V_{dc} is the amplitude of the square wave.

Several techniques to generate SPWM such as delta, delta-sigma, selective harmonic elimination, and space vector control are based on shifting signal harmonics frequency up to the carrier frequency and the decisive point between them is how much high residual harmonics can be produced or losses value by each method. When carries frequency is selected two points must be taking into consideration according to the frequency modulation ratio (m_f) value as in (2) [14].

$$m_f = \frac{f_{PWM}}{f_1} \tag{3}$$

Where, f_{PWM} and f_1 are PWM carrier frequency and fundamental frequency, respectively.

Firstly, attention need to be taken, where if m_f is not an integer, there will be a chance to produce subharmonics at output voltage. Secondly, if m_f is not odd, direct current (DC) component may exist and even harmonics can be presented at output voltage. While signals that contains carrier frequency can be easily filtered using low pass filter. However, the output transformer leakage reactances with a shunt capacitor are the main elements. Unfortunately, if DC component is presented at the output, it can cause big portion of losses.

Recently, generating SPWM waveform using microcontrollers to fed converters was a field of study for many researchers' and various techniques was implemented [1], [15]–[17]: i) Applying a mathematical expression such as Taylor series as (4):

$$e^x = 1 + \frac{x}{1!} + \frac{x^2}{2!} + \cdots, \text{for} -\infty \leq x \leq \infty\,, \tag{4}$$

taking into consideration machine cycle period per instruction is one microsecond then total execution time required to apply Taylor expression in (3) for first three terms there will be more than ten microseconds (usually up to seven iterations as a minimum value); ii) Generating waveform from previous stored values for SPWM and recall these values regardless to feedback rate to prevent extra execution time; and iii) Storing multiple SPWM values and recall a string of value for execution according to feedback rate and that can cause missing of linearity (due to low quantization with respect to feedback). Prior to the previous, all mentioned techniques can either caused huge time delay that lack the system from continues operation or fail to reach linear variation to the generated waveform according to the feedback.

2. PROPOSED TECHNIQUE

Produce modified recursive algorithm to reduce the computational complexity for online calculation when producing SPWM, is present in this work. The proposed technique should overcome the previous mentioned obstacles and will provide the following characteristics: i) Linearity of the voltage control, when feedback is implemented; ii) Low value of low-order harmonics at the output voltage; iii) Sufficient time allowance for proper operation of the inverter switches and control system; and iv) Continuity to generate the waveform without interrupt when feedback value changes.

Low cost eight-bit 16F877A PIC microcontroller [18] running at 20 MHz clock frequency with ten-bit resolution ADC, two 8-bit timers, one 16-bit timer, two analogue comparators and two capture compare PWM (CCP) shown in Figure 2 was selected to generate 50 Hz SPWM. Generating SPWM waveform such as in Figure 3, will be restricted to four parameters that are microcontroller clock frequency, execution time required per instruction, prescaler timers' value that is used and the 28-bit address length.

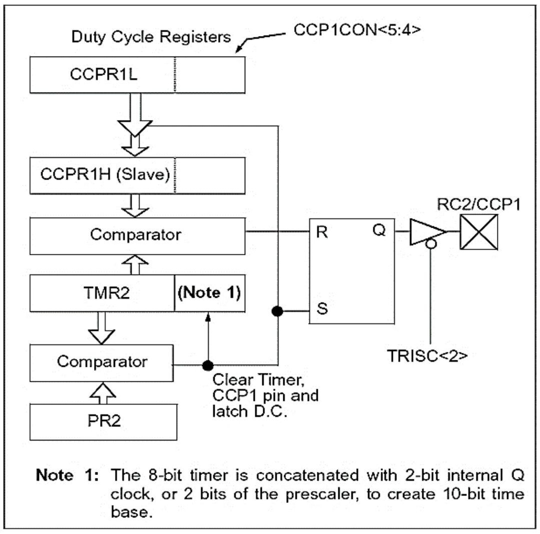

Figure 2. Simplified block diagram of PWM pinout inside the microcontroller

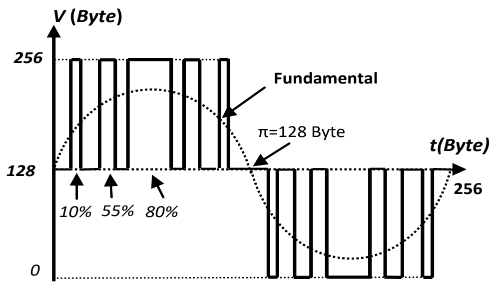

Figure 3. Generated SPWM from microcontroller

The proposed method based on dividing the address into two parts each 128 byte will represents 10 ms or half cycle of the sine wavein the other hand the sine wave magnitude is likewise segmented into two parts each 128 byte, as shown in Figure 4. The major section of the address executes the signal and only small fraction is added as a correction parameter. The correction parameter value changes in proportion to error value of the feedback and that will be added only when correction is required, as shown in the flowchart Figure 5.

The execution of SPWM algorithm requires three timers, the first one to hold the output for 10mSec (for half cycle), the second to count (128 µSec) till next duty cycle value while the third is needed to count between each pulse of PWM. For appropriate PWM timing value, two factors must be taken into considerations during the configuration of the timer module, which are "MCU clock Frequency and MCU bit's value" f_{OSC}=20 MHz, Oscillator period T_{OSC}=50 nSec.

Usually in wide range industrial inverters that are using analogue controllers, the carrier frequency of SPWM waveform is 7 kHz thus selected PWM frequency will be within the range of 7.8125 kHz (this value selected integer timer value). According to mention previously time period will divide into 256 bytes=2^8. Maximum possible timer clock frequency=7812.5*2^8=2 MHz.

$$T\arg et\ time\ prescaler\ value = \frac{Bus\ clock\ frequency}{Timer\ clock\ frequency} = \frac{20\ MHz}{2\ Mhz} = 10\ bytes\ (timer\ 1\ value) \quad (5)$$

Available prescaler timer values = {2, 4, 8, 16 …. 2^{16}}.

At this point, it is possible to select a divider rate from the listed values above, the value that equal to the result or closest greater value to the target prescaler timer value. For this case study, the prescaler can be set at 16 though only 10 bytes will be used. Sequentially to configure the second timer module for duty cycle, the period of the PWM signal in relation to the number of timer pulses during each PWM cycle must be calculated, once this value is calculated the output compare register values (the timer rate for generating the pulses) can be found as (6).

$$PWM\ period = 1/7812.5\ Hz = 128\ \mu Sec, \text{ and,}$$
$$PWM\ Period = [(Timer\ 1\ prescal\ value) + 1] \times 4\ Tosc\ (Timer\ 2\ prescal\ value)$$
$$128 \times 10^{-6} = (2^2 + 1) \times 4 \times 50 \times 10^{-9} \times TP2 \quad (6)$$

TP2=2^7 bit, while duty cycle will be obtained from Table 1.

PWM resolution is limited by the OSC clock frequency and PWM frequency as explained by (7).

$$resolution = \frac{\log\left(\frac{fosc}{f_{PWM}}\right)}{\log 2}\ byte \quad (7)$$

Where, f_{OSC} is the microcontroller clock frequency. While, $PWM\ resolution = \frac{log\left(\frac{20\ E6}{7.8125\ E3}\right)}{log2} \approx 11$ byte

Reducing PWM frequency to minimum value (4.3 kHz) can increase PWM waveform resolution by one byte and can reduce switching frequency, but unfortunately this can increase the low order harmonics value which increases parasitic losses and rise the requirement for increasing storage capacity for pseudocode. Yet the proposed technique required nine steps only to achieve the required resolution to reach the desired duty cycle. Sin wave in Figure 4 consists of Figure 4(a) shows how the half cycle of the sine wave is modified to be in bytes scale while Figure 4(b) shows the duty cycle value with respect to time base in bytes, during rated operation of the power inverter the duty cycle will not exceed 79% which is equal to 100 byte, this value is increasable to 128 byte in linear manner according to the feedback rate [19].

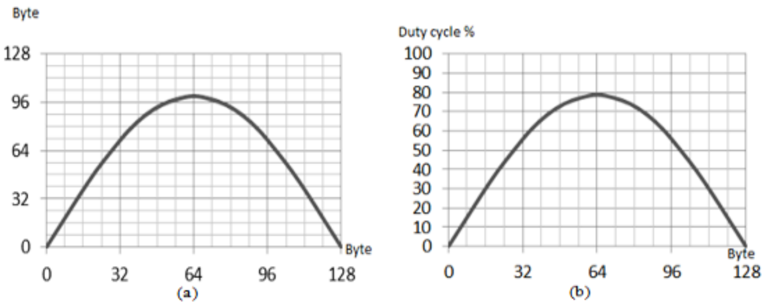

Figure 4. Sine wave: (a) In byte cycle and (b) In duty cycle

Then the Produced SPWM waveform quality can be evaluated with respect THD "total harmonic distortion" by utilizing (8) [20]–[22].

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} h_n^2}}{h_n} \quad (8)$$

3. ALGORITHM OF THE PROPOSED WORK

Taking advantage of micro-C language simplicity with the help of MPLAB; pseudocode was written and compiled to HEX code, flowchart in Figure 6 represents the running steps of the pseudocode. The produced switching angles are shown in Table 1. As shown in Figure 5, the code is divided into two parts; main and subroutine: The main part is responsible of configure fuses specified for PIC microcontroller 16F877A, reading the analog to digital conversion (ADC) value, and modified ADC, interleave dead time required for switches and calculating duty cycle value with respect to feedback value. While subroutine is responsible to execute PWM according to D duty cycle and counting eight-byte delay between each on pulse. Modifying ADC value from ten byte to eight bytes is easily done using (9).

$$ADC_{new} = ADC_{old}\ x\ 0.25 \tag{9}$$

The 0.25 indicate the ratio of 256 byte to 1024 byte. To find the duty cycle according to feedback value (10) can be used.

$$D_{new} = D_{old} \times ADC_{new} \frac{128}{256} \tag{10}$$

Duty cycle value will be recalculated each time of starting of PWM stream at 0˚, calculation time required to find the new ADC value and duty cycle value is imposed to interleave dead time at the 0˚ while timer will be called to interleave dead time at π or 128 bytes according to Table 1.

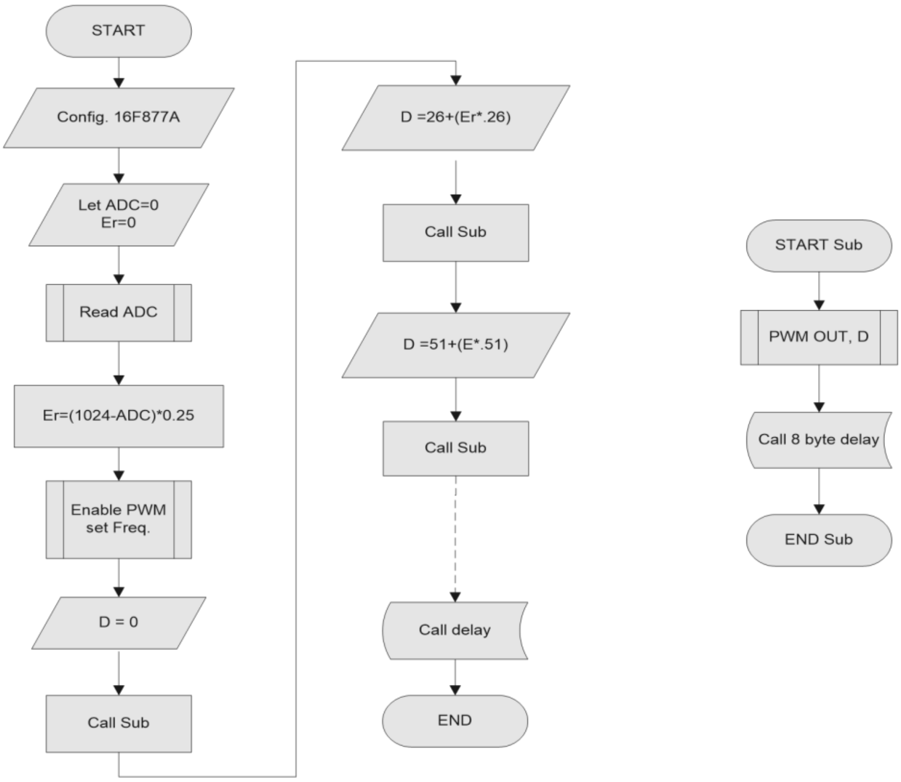

Figure 5. Flowchart of the executed pseudocode

Table 1. The generated half cycle sine wave table

Degrees (α)	Y P.U	X-Byte	Y-Byte	Duty cycle (%)	Time (mSec)
0	0	0	0	0	0
10	0.173648	7.111111	17	13.38583	555.5556
20	0.34202	14.22222	34	26.77165	1111.111
30	0.5	21.33333	50	39.37008	1666.667
40	0.642788	28.44444	64	50.3937	2222.222
50	0.766044	35.55556	77	60.62992	2777.778
60	0.866025	42.66667	87	68.50394	3333.333
70	0.939693	49.77778	94	74.01575	3888.889
80	0.984808	56.88889	98	77.16535	4444.444
90	1	64	100	78.74016	5000
100	0.984808	71.11111	98	77.16535	5555.556
110	0.939693	78.22222	94	74.01575	6111.111
120	0.866025	85.33333	87	68.50394	6666.667
130	0.766044	92.44444	77	60.62992	7222.222
140	0.642788	99.55556	64	50.3937	7777.778
150	0.5	106.6667	50	39.37008	8333.333
160	0.34202	113.7778	34	26.77165	8888.889
170	0.173648	120.8889	17	13.38583	9444.444
180	1.23E-16	128	0	0	10000

4. RESULTS AND DISCUSSION

Pseudocode was created and downloaded to the microcontroller according to the flowchart shown in Figure 5. Figures 6(a) to 6(f) show the output voltage waveform and its FFT correspond. Where the output waveform vary according to the feedback value and each sub-figure demonstrates the effect of changing by one-volt in the ADC input. This change affects the harmonic contain in the output voltage as presented. Figure 7 shows the fundamental, 3rd harmonic and 5th harmonic magnitude variation with respect to the input deviation step change, it is clear that the relation of deviation is linear to the voltage change of the feedback.

The generated waveform has THD value swaying between 11%-9% subject to vary according to the feedback voltage, during all cases where the harmonic exceded the limits of IEEE 519. However, the performance demonstrate better voltage quality in comparison to [15], [16], [23], [24]. Likewise, the proposed technique is at lower cost in comparison to other advanced technique such as in [25]. Figure 8 shows SPWM for quarter cycle and the imposed dead time required for semiconductors devices to mitigate the transient period of the switching.

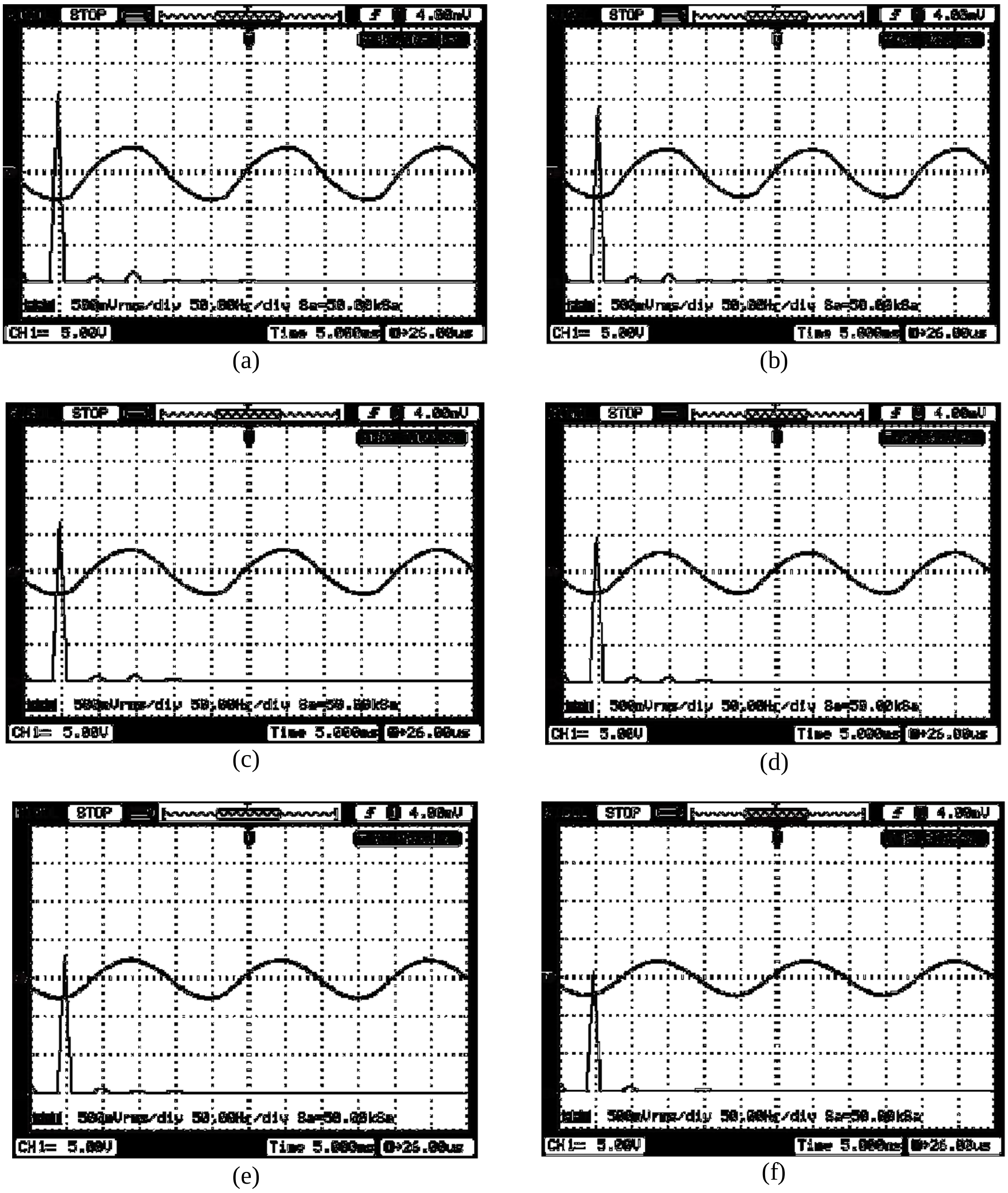

Figure 6. Voltage Fed to the feedback (a) no voltage presented, (b) one volt, (c) two volts, (d) three volts, (e) four volts, and (f) five volts

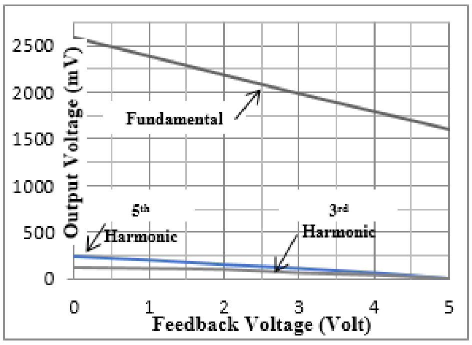

Figure 7. Harmonics in output vs feedback voltage

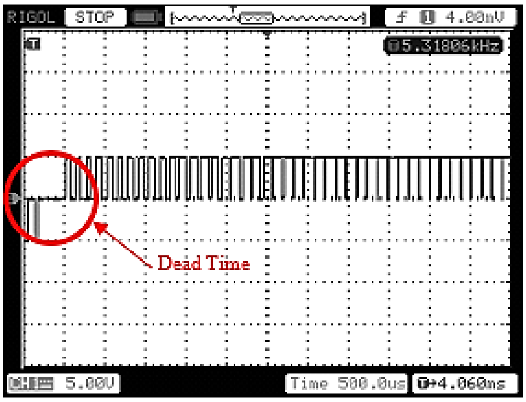

Figure 8. Dead time in SPWM waveform

5. CONCLUSION

According to the results, the proposed algorithm requires short time 300 µSec to complete calculation in comparison to other techniques that requires milliseconds as mentioned when implementing Taylor equation. The paper presented a contribution to produce SPWM with ability to change PWM switching angles with respect to feedback value in linear relation in compression to other techniques. The proposed technique uses the dead time delay required to ensure power electronics switches are fully off to count the waveform back to 0°. The proposed algorithm produces the SPWM with low magnitude of low order harmonics and low THD where it can be evaluated as high-quality signal was presented and by compairing the FFT result to other paper. Finally, proposed technique fulfills the requirements of simplicity, reliability, and low cost in comparison to other conventional techniques.

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