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A Method of Multi-channel Data Acquisition with Adjustable Sampling Rate

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Abstract

Sampling rate of current signal acquisition systems is singular. Aiming at this shortcoming, a method of multi-channel data acquisition (DAQ) with adjustable sampling rate is presented. The method realizes the cut-off frequency of anti-aliasing filter controlled by program with the help of switched-capacitor; by independently pulsing sampling signal of different ADCs, 16-channel sampling rate are adjustable within the range 50ksps, 25ksps, 10ksps, 5ksps, 1ksps. Theoretical analysis and experimental verification pointing at the proposed method are implemented: theoretical analysis shows that parameters of the filter meet the design requirements; experimental results show that cut-off frequency of the anti-aliasing filter matches variable sampling rate very well; choosing appropriate sampling rate according to the characteristics of the measured signal not only can well restore the measured signal, but also prevents system resources from waste. This method can meet needs of testing various signals with different frequency at the same time.

***Keywords*:** *data acquisition, adjustable sampling rate, multi-channel, anti-aliasing filtering*

1. Introduction

Data acquisition is the procedure of converting analog signal such as temperature, pressure, displacement to digital and displaying, transmitting, storing. It is the basic means to obtain information. When design a data acquisition system, selecting sampling rate is a critical work. If the sampling rate is too high, it is bound to waste system resources such as communication bandwidth and storage space; on the contrary, when the sampling rate is not high enough, signals whose frequencies is higher than the Nyquist frequency will cause aliasing. Once aliasing happens, it can not be filtered out from the discrete sampled data. So interference signals higher than the Nyquist frequency must be filtered out before sampling. Data acquisition system in Reference [1] is dedicated to neural signal sampling. It has 72 channels, but the sampling rate of each channel is fixed at 80ksps. Reference [2-6] are same in fixed sampling rate no matter what approaches they used and how they works. Data acquisition module in Reference [7] is designed for quick testing system of small satellites. It can works at either 1sps or 10sps. but once the specific channel has selected one kind of sampling rate, it can not be changed. Looking for a method applying to complex signal acquisition is always the goal in engineering designing. Aiming at this demand, a data acquisition method with multi-channel and adjustable sampling rate is presented in this paper. In this method, sampling rate of each channel can be preseted according to the characteristics of analog signals. It achieves generality to some extent.

2. Structure of the Adjustable Sampling Rate DAQ Card

The structure of the adjustable sampling rate DAQ card is shown in Figure 1. The 16bit ADC samples and quantifies sensor's output signal which is conditioned and anti-aliasing filtered, then the FPGA buffers data frames and uploads to PC via a parallel interface.

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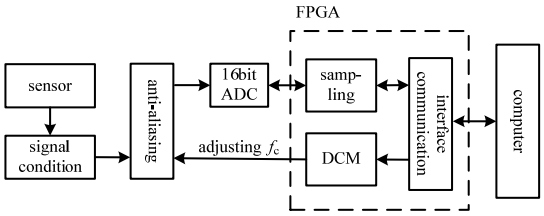

Figure 1. The Structure of the Adjustable Sampling Rate DAQ Card

The DAQ cards can be connected distributedly according to user's need, Each ADC can be configured in human-computer interaction among five sampling rate, 50ksps, 25ksps, 10ksps, 5ksps and 1ksps. Data processing method and the matching of filter's cut-off frequency with adjustable sampling rate are the core problems to be solved, on this basis, the realization of high-precision is analysed.

3. Data Processing under Multiple Sampling Rates Condition

Sampling rate of ADCs on one board may different, meanwhile, the parameters are separated between devices. Therefore A/D conversions for all ADCs do not end simultaneously even if they begin at the same time. In this case, using one FIFO to buffer the convertion result, as general used, is likely to cause frame confusion. For this reason it can not satisfy the data processing requirement under the condition of multiple sampling rates. In this paper ping-pong operation is adopted, as shown in Figure 2, this guarantee the reliability and speed of data processing.

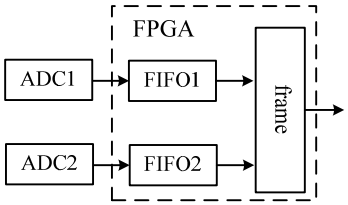

Figure 2. Procedure of Forming Frame

Two ADCs' output data enter FPGA via different channels. After identifying a frame alignment signal which is separated from another one by 1ms, the internal control module reads a certain amount of data from each FIFO to form a data frame, for example, when the sampling rate of ADC1 is 50ksps and the ADC2's is 1ksps, the control module firstly enables FIFO1 and reads all data during 50 A/D conversion cycles, and then turns to FIFO2 and reads all data during one A/D conversion cycle. The two parts are formed a data frame and uploaded to PC. The PC decomposes a piece of data in the same format, and then restores the initial analog signal of every channel .

In consideration of the cost, dedicated FIFO chip as Reference [8] and Reference [9] used is deserted. It's replaced by soft FIFO instantiated with internal block RAM of FPGA. The depth of each block RAM can hold a ADC conversion outputs with 50ksps sampling rate during 1ms.

4. Matching of Anti-aliasing Filter's Cut-off Frequency with Sampling Rate

Passive filter and RC active filter features high requirement of discrete component and complexity of the design process. More importantly, their cut-off frequency can hardly match with adjustable sampling rate.

Reference [10] realized cut-off frequency changing by means of changing outside RC network using multiplexers. This circuit features complex structure and difficultly designed compensation circuit, what's more, it occupied so much PCB space that it can hardly satisfy multi-channel synchronization acquisition system.

In the Reference [11], MCU controls multiplexers and relays to choose a filter within several independent ones that have a certain fixed cut-off frequency, this method can not realize continuous adjustment of cut-off frequency.

The cut-off frequency of switched-capacitor filter is proportional with the input clock, i.e. clock-tunable. So it's easy to change cut-off frequency by providing different clock frequency. LTC1068 is one type of switched-capacitor filter. In this design, LTC1068 is applied to form four-order Butterworth lowpass filter. The problem matching filters' cut-off frequency with ADCs' sampling rate reaches a good solution.

Signal may fold back and distort if its frequency near to sampling rate of LTC1068 itself. On the other hand, the internal high-speed switching leads to feed through effect and introduces noise too. For this reason, it is essential to add lowpass filters, both before and behind LTC1068, respectively, to limit bandwidth, as shown in Figure 3. LTC1068's internal switching frequency and sampling rate are both so much higher than the desired signal frequency that it greatly reduces the difficulty of designing lowpass filters, a simple one-order RC circuit can meet the requirements.

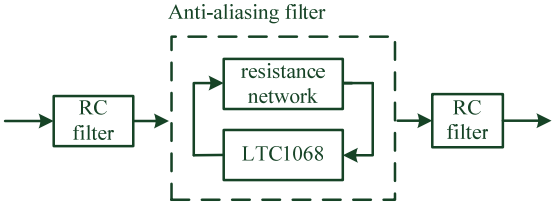

Figure 3. The Structure of Anti-aliasing Filter

5. The Realization of High-precision Sampling

5.1. Using High-resolution ADC

Resolution and signal-to-noise ratio (SNR) is the two most important parameter to reflect the accuracy of ADC. At the ideal case, the following relationship exists between them [12]:

$$SNR_{idial} = 20\log_{10}\left(\frac{2^{(N-1)}\cdot\frac{q}{\sqrt{2}}}{\frac{q}{\sqrt{12}}}\right) = 6.02N + 1.76 \quad (1)$$

Wherein q is the ideal code element width, N is the nominal resolution of ADC.

In practical application, signal-to-noise ratio is inevitably reduced by the harmonic distortion (THD) introduced from device itself, take the THD into account, and figure out the practical SNR, that is the signal-to-noise ratio and distortion (SINAD) [13-15].

$$SINAD = -20\log_{10}\sqrt{10^{-SNR/10} + 10^{THD/10}} \quad (2)$$

Substitutint the SNR_{ideal} in Equation (1) with the $SINAD$ in Equation (2), and get the ADC's effective resolution (ENOB):

$$ENOB = \frac{SINAD - 1.76}{6.02} \quad (3)$$

It follows that the effective resolution of ADC is bellow its nominal resolution. So the 10 bits effective resolution is needed in theory for achieving the accuracy requirement of 0.1%, that is to say the nominal resolution should be at least 12 to 14 bits. In the design, to provide error toleranct margin to offset the error introduced by the previous stage circuit, the AD7606 with 16 bits resolution is choosed.

5.2. Introducing Oversampling

AD7606's internal digital filter allows a selectable oversampling function. The lower switching frequency is, the greater internal selectable oversampling ratio (OS) is, but at the same time the 3dB bandwidth is also decreased. Depending on the difference of frequency of signal measured, synthetically considering the AD7606 bandwidth, the switching frequency and oversampling ratio, the ralationship bettween them is shown in Table 1.

Table 1. Correlation of Oversampling Ratio, 3dB Bandwidth and Conversion Frequency

3dB bandwidth	13.7kHz	10.3kHz	6kHz	3kHz	1.5kHz
conversion frequency	50ksps	25ksps	10ksps	5ksps	1ksps
OS	4	8	16	32	64

The introducing of oversampling reduces the quantization error within the passband, and moves the generated harmonics outside the passband, so makes the SNR performance further improved, therefore a correction factor should be added into Equation (1) in order to reflect the ultimately improving extent of SNR, such is shown in the following Equation (4) [13-15]:

$$SNR=6.02N+1.76+10\log_{10}\frac{f_s}{2\cdot BW} \quad (4)$$

Wherein, $10\log_{10}\frac{f_s}{2\cdot BW}$ is the correction factor, f_s is the sampling rate after introducing oversampling, *BW* is the bandwidth of signal measured. Assuming that *BW* is equal to the 3dB bandwidth of AD7606, take the 4 times over-sampling rate in Table 1 as example,

$$\text{Correction factor} = 10\log_{10}\frac{4\times 50\text{k}}{2\times 13.7\text{k}} \approx 8.6\text{dB} \quad (5)$$

As shown, the SNR has been improved 8.6dB, that is 9.9dB when the oversampling ratio is 8, so following this way, the larger oversampling ratio is, the more SNR is improved.

5.3. Reducing the Error of Conditioning Circuit

A high precision acquisition can not be achieved only depending on high-resolution ADC, but the preamp conditioning circuit is equally important. When the measured signal amplitude range is 0~5V, while the input range of AD7606 is -5V to +5V, it will lose half of the quantization precision without conditioning. In this design, the method is to subtract 2.5V from the measured signal and then to amplify the result 2 times.

In the subtraction circuit, the measured signal as "minuend" is connected to the noninverting input terminal of op amp, while 2.5V as "subtrahend" is connected to the inverting input terminal of op amp, this kind of structure can avoid the consequences which the equipment is damaged when the current flow backward the signal measured. The 2.5V voltage is provided by a precision reference voltage source ADR421, that will reduce the source port error. At the same time ADR421 as the external reference source of AD7606 provide a reference for its quantization process.

The selected noninverting amplifier circuit whoes high input impedance can improve the quality of signal output by the front stage circuit, and what more important is the gain of such a structure will not be reflected by the output impedance of front stage circuit, so it can be accurately fixed at 2 to improve the conditioning precision. Additionally, the high quality resistors

whose accuracy is 0.1% and temperature drift coefficient is 10ppm/℃ will be used in entire conditioning circuit.

6. Theoretical Analysis and Performance Testing

6.1. Theoretical Analysis

In essence anti-aliasing is lowpass filtering. As shown in Figure 4, f_s is sampling rate, and f_h is the highest useful frequency component appearing in desired signal. When ADC uses f_s to samples 0~f_h , signal within frequency band of (f_s-f_h)~f_s is regarded as interfering signal because it will be symmetrically superimposed on the useful frequency band of 0~f_h , centering on $f_s/2$. For this reason, signals whose frequency is greater than (f_s-f_h) should be at least attenuated to the quantization level of the ADC [16].

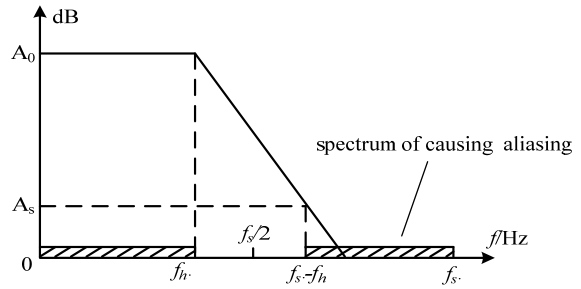

Figure 4. The Diagram of Causing Aliasing

According to the n-order Butterworth frequency response function:

$$\left|A(j\omega)\right| = \frac{A_0}{\sqrt{1+\left(\frac{\omega}{\omega_C}\right)^{2n}}} \tag{6}$$

Equality of As follows ω can be deduced, wherein A_s is the amplitude attenuation value of signal outside the stopband, ω is angular frequency at a certain frequency point and ω_c is the angular frequency corresponding to f_c :

$$A_s = 20\log_{10}\frac{\left|A(j\omega)\right|}{A_0} = -10\log_{10}\left(1+\left(\frac{\omega}{\omega_c}\right)^{2n}\right)\text{dB} \tag{7}$$

Outside the stopband $\omega >> \omega_c$, that is $\omega / \omega_c >> 1$, equality (7) can be simplified as follow:

$$A_s \approx -10\log_{10}\left(\frac{\omega}{\omega_c}\right)^{2n}\text{dB} \tag{8}$$

Therefore, the order of filter should be $n \approx \frac{A_S}{20\log_{10}\frac{\omega}{\omega_c}}$.

Referring to Table1, suppose f_h was 13.7 kHz, conversion frequency was 50ksps and the oversampling ratio of AD7606 was configured as four times. That is to say, the actual sampling rate f_s is 200ksps. In this case, frequency components higher than (200k-13.7k)=186.3kHz must be filtered out because this part will be superimposed on the desired signal. Generally speaking, high frequency noise has small amplitude. Assuming that the

amplitude is as big as 5V, i.e. the upper bound of AD7606's analog input, the noise would have to be attenuated to $\pm\frac{1}{2}$LSB (76μV), that is:

$$A_s = 20\log_{10}\frac{5}{\frac{1}{2}\text{LSB}} \approx -96\text{dB} \quad (9)$$

When A_s= -96dB and $\frac{\omega}{\omega_c}=\frac{f}{f_c}=\frac{186.3\text{kHz}}{13.7\text{kHz}}\approx 13.6$, We conclude that n≈4.2 according to the Equation (8).

The needed smallest filter's order in extreme case is given above. In fact, amplitude of noises are far less than 5V and a larger oversampling ratio can be chosen, so four order filter can meet requirement.

6.2. Performance Test

According to the parameters calculated above, with the help of auxiliary software FilterCAD, the simulation result of ideal fourth-order Butterworth anti-aliasing filter is given, as the frequency response curve shown in Figure 5(a).

When testing the actual anti-aliasing filter, set cut-off frequency to 10kHz, input a standard sinusoidal signal and measure the output then compute the attenuation value. Like this, dozens of signals ranging from 50Hz to 30kHz are tested. The results are depicted in Figure 5(b), in scatter plot form. Table 2 lists a section data of the results.

When ADC's sampling rate changes, filter's cut-off frequency should also be adjusted accordingly. Figure 5(c) gives the frequency-attenuation scatter plot measured respectively when cut-off frequency is 6kHz, 3kHz and 1.5kHz.

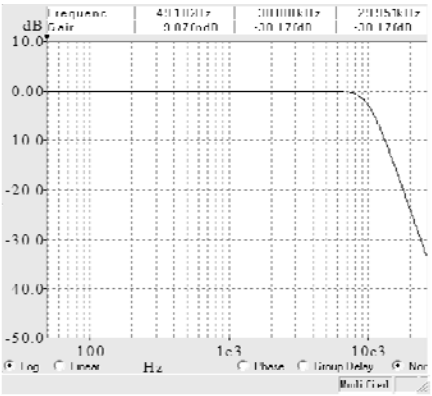

Figure 5(a). The Simulation of the Amplitude-frequency Characteristic

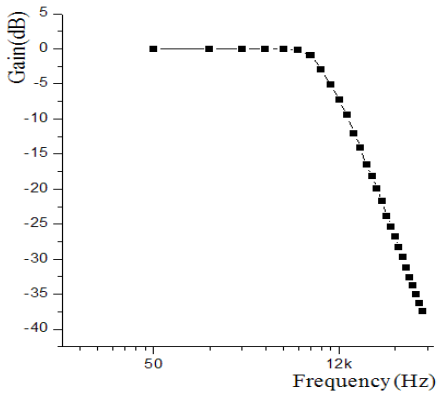

Figure 5(b). The Measured Amplitude-Frequency Characteristic

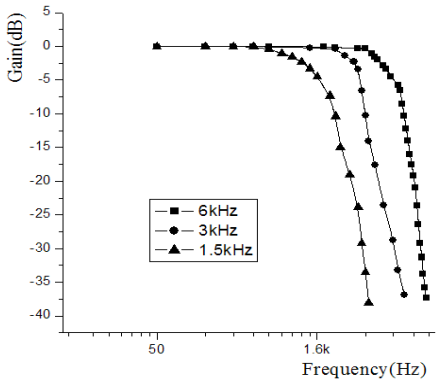

Figure 5(c). Amplitude-frequency Characteristic of Different Cut-off Frequency

When contrasting Figure 5(b) with 5(a), it can be seen that the amplitude attenuation of each frequency band is approximately equal; by contrasting Figure 5(b) with 5(c) we can see that amplitude has almost no attenuation within the passband and tends to roll off steeply along a close-to-straight line outside the stopband, no matter which cut-off frequency is. Those imply that the filter provides good performance.

Table 2. Data Before and Behind Filter

Frequency(Hz)	Amplitude (mV) original signal	Filtered	Gain(dB)
1k	4000	4000	0
3k	4000	3960	-0.0873
5k	4000	3920	-0.17548
8k	4000	3600	-0.91515
10k	4000	2840	-2.97483
12k	4000	1720	-7.33063
14k	4000	1000	-12.0412
16k	4000	596	-16.5363
18k	4000	400	-20
20k	4000	256	-23.8764
22k	4000	182	-26.8398
24k	4000	130	-29.7623
26k	4000	93.6	-32.6157
28k	4000	71.2	-34.9916
30k	4000	53.6	-37.4579

A superimposed signal, which is obtained by adding a 200kHz 5V_{pp} sine wave to a 1kHz 5V_{pp} one, act as the input of the sampling system, as shown in Figure 6(a). Here, the 1kHz sine wave is seen as desired signal. Take 50ksps as AD7606's conversion frequency and set over sampling ratio to four times. Under these circumstances, "high frequency" higher than 199kHz needs to be filtered out to obtain a pure 1kHz sine wave without aliasing. Figure 6(b) shows the output wave of the filter. The output wave, which is a 2.5V_{pp} 1kHz sine wave, implies that 2.5V is "subtracted" from the input signal and the 200 kHz signal is filtered out.

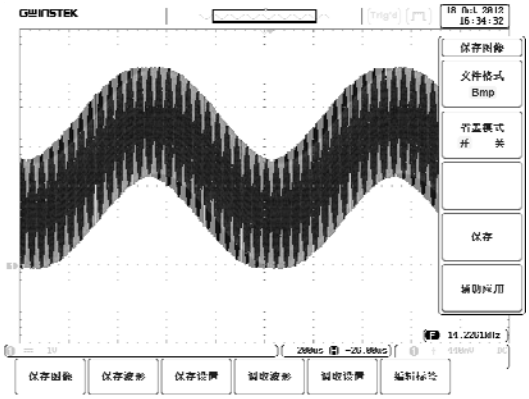

Figure 6(a). Input a Superimposed Signal

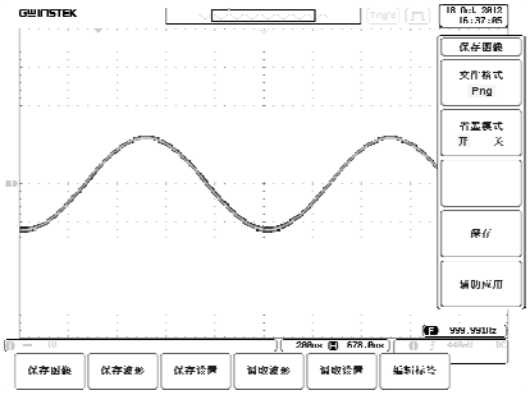

Figure 6(b). Signal Behind Anti-aliasing Filter

With the help of computer test software, A/D conversion results are depicted as waveforms, as shown in Figure 7. The wave in Figure 7(a) contains 50 points per period, corresponding to 50ksps. Similarly, Figure 7(b) and Figure 7(c) respectively shows waveforms corresponding to 25ksps and 10ksps.

By contrasting three waveforms in Figure 7, it can be seen that 25 points are enough to restore the input signal very well, but 10 points are not; while 50 points will inevitably cause unnecessary waste of system resources.

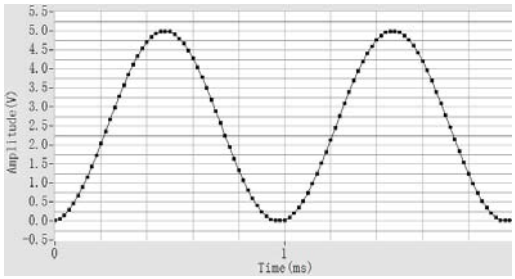

Figure 7(a). Waveform Corresponding to 50ksps

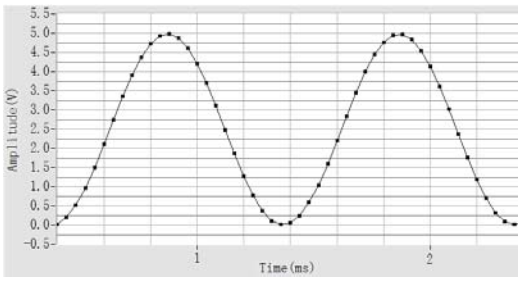

Figure 7(b). Waveform Corresponding to 25ksps

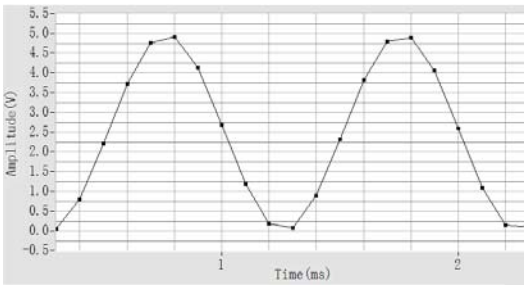

Figure 7(c). Waveform Corresponding to 10ksps

7. Conclusion

A multi-channel DAQ card with adjustable sampling rate is designed. In this design, the sampling rate can be preseted in human-computer interaction; the acquisition accuracy is improved through methods, such as selecting high-resolution ADC, introducting over-sampling technology, and decreasing conditioning circuit error and so on; otherwise the cut-off frequency of anti-aliasing filter can be program-controlled adjusted along with the difference of sampling rate. The test results show that: well-performed anti-aliasing filter can effectively filter out high-frequency interference which may cause aliasing; and the adjustable sampling rate can provide the most appropriate points to restore the tested signal, which is very essential for achieving optimization configuration of system.

In the future, a further research can be done in the correction of anti-aliasing filter's nonlinear phase shift and the heightening of ADC's conversion frequency.

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