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A novel design for hardware interface board with reduced resource utilization

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ABSTRACT

The final cost of an integrated circuit (IC) is proportional to its testing time. One of the main goals of test engineers when building an IC test solution is to reduce test time. Reduction of Test time is achieved by multi-site testing where multiple ICs are tested simultaneously using automated test equipment (ATE). During multi-site testing, if a certain test requires abundant resources, it is accomplished by testing one set of ICs at a time while the other ICs remain idle, thus lengthening the total test time. In digital-analog hybrid ICs, both analog and digital tests need to be performed, increasing the tester resource requirement and causing digital resource shortage. This paper describes a hardware interface board (HIB) design for a test case of a digital-analog IC on Teradyne's ETS-364 ATE. The HIB's design allows the ATE to perform multi-site I^2C based tests, which usually require lot of tester resources, utilizing only two digital resources and one measurement resource. This design achieves halving the I^2C test time while lowering the number of resources necessary for multi-site testing compared to set-by-set testing. The proposed work has achieved up to 90.625% of resource reduction for multi-site testing for a single test.

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1. INTRODUCTION

The testing of an integrated circuit (IC) on an automated test equipment (ATE) requires multiple tester resources connected to a single pin and a single resource connected multiple pins. The different tests to be conducted on the IC are done so one after the other. For each test, particular resources have to be connected to each pin of IC during the start and have to be disconnected at the test so that a different set of resource can be connected for a different test. To facilitate this, a printed circuit board (PCB) containing multiple relays, controlled by the tester, is used as an interface between the ATE and the IC. This board is called the hardware interface board (HIB) or device interface board (DIB). The ATE used for this design is eagle test systems -364 (ETS-364) by Teradyne. The ETS-364 general-purpose mixed-signal tester platform has a high degree of accuracy. This testing device is intended primarily for high-volume testing of ICs.

The changing essence of circuit development is portrayed in [1]. Agrawal [2], goes into detail on the definition of the test and how electrical devices got their inspiration. Estimation of coverage is accomplished by identifying all the features of each un-detected test case not known while the project is under development

of the fault list. Test coverage has been described in depth in [3]. Hashempour *et al.* [4] discusses the study of several sites with regard to multi-site testing of very large-scale integration (VLSI) chips. Here Xiang *et al.* [5], shows a unique ATE for ICs. Most commonly, a test for internal circuitry is done in the field, which is known as field service or after-the-fact repair. Additional information about ATE is obtained from [6]-[12], while the information regarding I2C, PMBus and DAC is derived from [13]-[21]. Test models, test methodology and testing of digital devices on ATE, shown in Figure 1, is explained succinctly in [22]-[26].

The system is an all-in-one hardware and software construction with an interconnected architecture. This tool is very ideal for use in many areas which demand high throughput. On each site on ETS-364, floating resources are provided separately. By increasing site isolation, this increases the site's security. There are up to 133 mega vectors per second (MVPS) digital vector rate possible, which is made possible with the device's compatibility for up to 240 analogue channel pairs and 128 digital channel pairs. The ETS-364 consists of a rack to hold all power supplies and resources along with a short test head where the hardware interface board is mounted. Some of the resources present in ETS-364 utilized for this design in Figure 1.

- Analog pin unit (APU): It is used to force and measure analog voltages and current. There are 96 APU resources in ETS-364.
- Quad measurement unit (QMS): It is a resource which exclusively measures voltage. It is a high precision unit with a very high input impedance so as to not draw current from the tester and alter the voltage reading. There are 16 QMS pins in the tester.
- Digital pin unit (DPU): It is a resource used to provide and sense digital data. There are 64 pins in ETS-364.

The HIB is mounted on the test head of ETS-364. The HIB shown if Figure 2 is four-site HIB capable of testing four IC's together parallelly. All the resources available in the tester are brought out to the test head in the form of pogo pins. When the hardware interface board is placed and secured onto the test head, all the tester resources come onto the HIB. These resources can be seen on the periphery of the HIB seen on Figure 2. However, all resources of the tester need not be used for the testing of a particular IC. Therefore, from the resources, only required resources are brought from the periphery to the IC pins. Since multiple IC's need to be mounted onto the HIB at a time and also repeatedly, an interface called the socket is constructed on top of the HIB. All the hardware connections are made to the pins of the socket while a robotic handler takes the ICs and presses them into the socket for testing. After testing, the ICs are placed into the appropriate pass/fail bin after which the next set of ICs are pressed into the socket. The I^2C protocol in this design is based on the PMBus protocol for power management ICs.

Figure 1. ETS-364 tester [22]

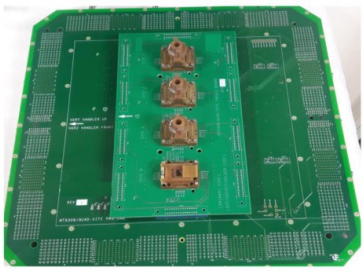

Figure 2. Hardware interface board [22]

2. TEST CASE DEFINITION

The test used as a benchmark test for reducing the number of number of resources used without compromising the test time is explained in this section. A model IC functionality is defined to decide the test solution. These are as follows:

- The integrated circuit is a digital IC which has multiple registers to store data from certain computations performed by the IC.
- This data is used to communicate with the outside world through an I^2C protocol.
- The data line is an open-drain configuration which can provide a logic low state but provides a high impedance state instead of a logic high state. The circuit in Figure 3 describes the open-drain configuration used in the IC.

When the IC wants to write a logic low, the logic controller switches ON the metal oxide semiconductor field effect transistor (MOSFET) pulling down the voltage to '0' volts. When the IC wants to write a logic high, the logic controller switches OFF the MOSFET causing the line to go to high impedance 'Z' state and a voltage level of 3.3V from the pull-up appearing on the data line. This IC design can be used to define the test methodology for this functionality as follows:

- The test consists of writing data into the device registers through a 'I^2C write protocol'.
- Each individual register is accessed individually and data is written.
- 'Acknowledgements' from the IC are read back to see success of data transmission.
- After all registers are written, they are accessed again with an 'I^2C read protocol'.
- The data read back is compared to the initial data written.
- Based on results of comparison, the ICs are transferred to the pass/fail bin.

The HIB circuitry for the existing design methodology and the subsequent modifications and improvements are explained in the further sections.

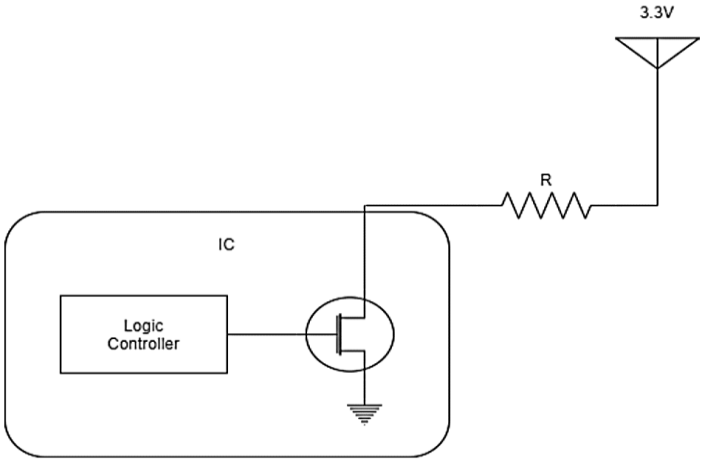

Figure 3. IC pull-up circuitry

3. EXISTING HIB DESIGN WITH MINOR MODIFICATION

The layout in Figure 4 describes the method in which HIBs are designed. Since, I^2C testing requires two pins from each IC and this test has to be run parallelly for all four sites, eight DPU pins, have been selected from the pogo pins on the periphery of the HIB. The HIB has four sites upon which sockets are mounted and the PCB tracks are hardwired onto them. The four ICs to be tested are placed onto the sockets.

The testing process is simple and straightforward for this HIB layout. The data pins, IO#2, IO#4, IO#6, and IO#8 are placed in a group in the tester. Similarly, the clock pins IO#1, IO#3, IO#5 and IO#7 are also grouped. The intention of grouping is to ensure that all data pins transmit the same data together while all the clock pins are synchronized together.

Considering an example where there are only four DPU pins available, the sites are split into odd sites and even sites where odd sites are tested first after which the even sites are tested. This type of testing doubles the testing time for this particular test. A modification where the test time need not be sacrificed is explained below.

While the data line of the circuit is a bidirectional line which is used for both reading and writing data into the IC, the clock line is a monodirectional line where the signals move from the tester to the device. Compared to the IC, the tester is a powerful resource and can drive large amounts of current to ensure that a logic stays at a particular level. Even if there is a shortage in the amount of drive current, buffers can be added to the HIB to ensure that required current is provided. This modification requires a single DPU resource as a clock line for each site while the number of data lines depend upon the number of sites on the hardware interface board. The layout in Figure 5 is a representation of having a single clock line with four data lines. This brings down the total pins required for this test from eight to five without decreasing the tester time. In this layout however, four data lines are still being used and the number of data lines will increase with increase in the number of sites and therefore is not the perfect solution. The next section aims to provide amicable solution to this problem.

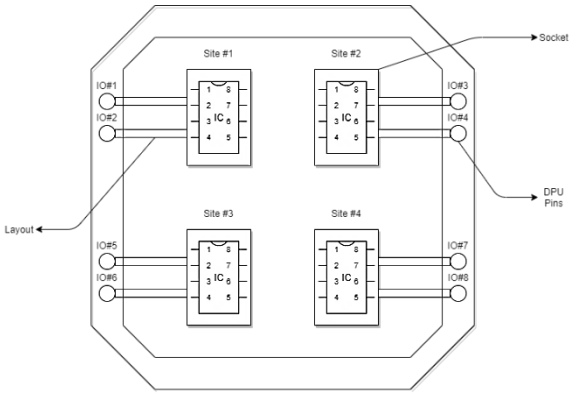

Figure 4. HIB layout–existing architecture architecture

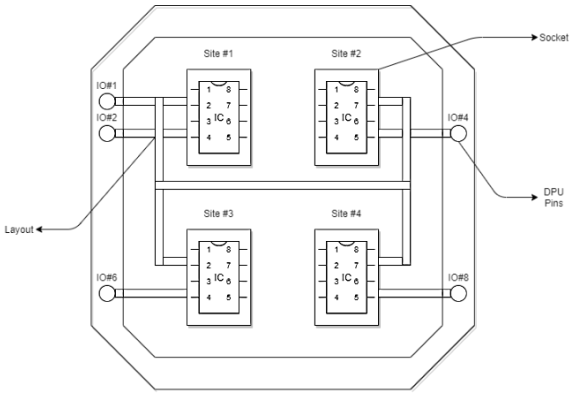

Figure 5. HIB layout–modified architecture-I

4. HIB MODIFICATION–II

This section aims to design a HIB circuitry with minimal and constant number of pins irrespective of number of sites on the HIB. The circuit is designed by having a common data and clock lines to each IC. However, before the data line is connected to the socket, a unidirectional buffer is added. This allows only one direction of current through it, i.e., from the tester to the socket. The net between the buffer to the ground is connected to a four-input digital to analog converter (DAC) such that the net form the first site is connected to the least significant bit (LSB) of the DAC, and so on until the fourth site is connected to the most significant bit of the DAC.

The output of the DAC is provided to the quad measurement unit (QMS) which accurately measures the analog voltage from the DAC and the test program converts the analog output obtained back to the binary value to which the individual outputs can be mapped back to the outputs of the IC. The DPU of the ATE is capable of generating a clock which can be used to digitize other resources on the tester. Therefore, though continuous values are provided to the tester form the DAC output, the output voltage is measured only when a particular clock signal is provided from the DPU. In the circuit in Figure 6, the green tracks denote the data line while the red tracks denote the clock line. During write operation, the DPU digitizes the QMS whenever the acknowledgment pulses are needed to be read and during read operation, the DPU digitizes the QMS such that all the data is read as analog signals and is the decoded. Therefore, it can be seen in this section that the HIB circuit design requires only three pins irrespective of the number of sites in the HIB, the only change being the number of input bits to the DAC.

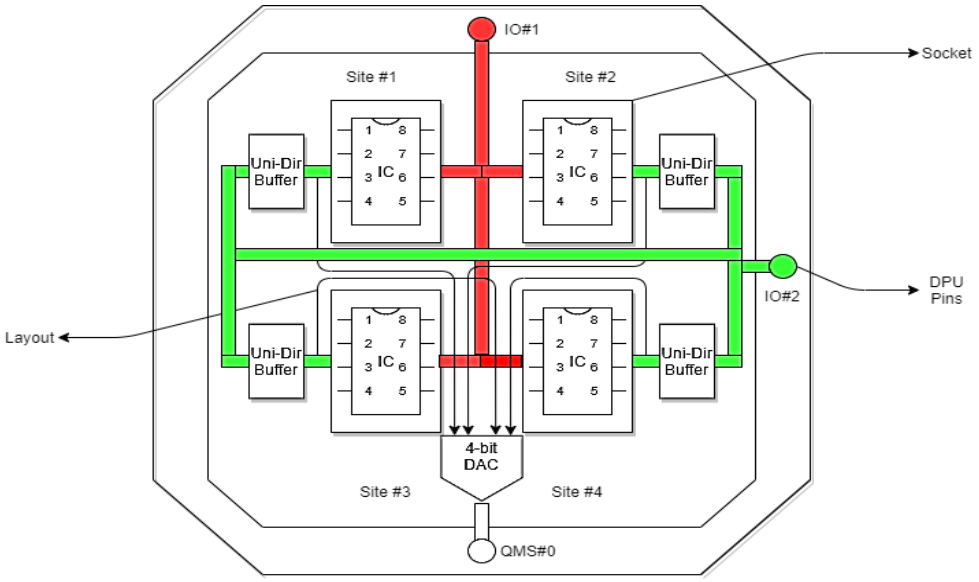

Figure 6. HIB layout–modified architecture

5. RESULTS AND DISCUSSION

In this section, the hardware interface board circuitry with the different design styles: the basic style, odd-even site style, common clock style and the common data style are compared to obtain the improvements of the modifications over the basic version. The comparison between different circuit designs in Table 1 provide an insight to the reduction in the number of resources used. While the circuit is designed for a four site HIB, the results can be obtained for other sites as well. Since, the proposed work requires only three resources irrespective of the number of sites in the HIB, the reduction of resources increases with increase in the number of sites.

Since ETS-364 ATE can support a maximum of sixteen sites, a sixteen-site solution will have the maximum reduction in the resources used while keeping the testing time constant. The graphs in Figure 7, provide a visual representation of the reduction of resources. It can be seen that with the final modification made in the HIB circuitry, the resources required for the test remains constant.

Table 1. Resource usage comparison for a single test

	Resources Used for a single test		
Number of Sites	Basic HIB Circuit	HIB Modification -I	HIB Modification - II
1	2	2	3
2	4	3	3
4	8	5	3
8	16	9	3
16	32	17	3

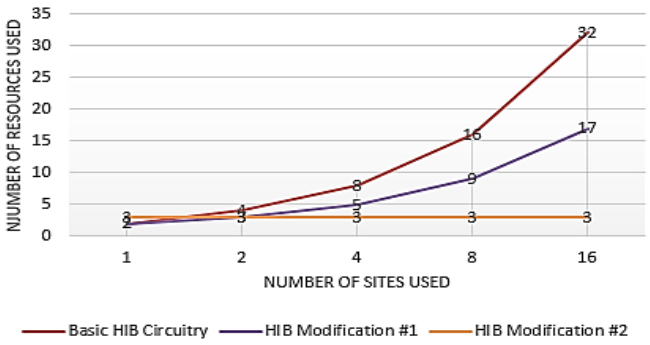

Figure 7. Number of sites vs resources used

6. CONCLUSION

From the proposed work, it can be concluded that the modification of the HIB circuitry for a four site IC provided over 62.5% reduction in resources used for a single test and 81.25% and 90.625% reduction in resources for eight site and sixteen site HIBs respectively for a single test. When compared to odd–even site testing, the methodology proposed halves the test time. Although, this improvement is for a single test and an IC will have multiple tests, the design can still save a lot of tester resources and enable more sites to be tested simultaneously, thereby reducing testing time.

REFERENCES

[1] D. Comer, "The changing face of circuit design," *IEEE Potentials*, vol. 25, no. 3, pp. 26-30, Jul. 2006, doi: 10.1109/MP.2006.1657759.

[2] V. D. Agrawal, "Electronic testing for SOC designers," *Proceedings of ASP-DAC/VLSI Design 2002. 7th Asia and South Pacific Design Automation Conference and 15h International Conference on VLSI Design*, Jan. 2002, doi: 10. 1109/ASPDAC.2002.994877.

[3] K. Hird, K. Parker, and B. Follis, "Test coverage: What does it mean when a board test passes?" In *Proceedings. International Test Conference*, Oct. 2002, pp. 1066-1074, doi: 10.1109/TEST.2002.1041863.

[4] H. Hashempour, F. Meyer, and F. Lombardi, "Analysis and evaluation of multisite testing for VLSI," *IEEE Transactions on Instrumentation and Measurement,* vol. 54, no. 5, pp. 1770-1778, Oct. 2005, doi: 10.1109/TIM.2005. 855099.

[5] Z. J. Xiang, X. Hu, L. Wang, and Z. Li, "An automatic test equipment for integrated circuits in the extreme environments," in *2016 International Conference on Integrated Circuits and Microsystems (ICICM)*, Nov. 2016, pp. 46-49, doi: 10.1109/ICAM.2016.7813561.

[6] S. Sundar *et al.,* "Low cost automatic mixed-signal board test using IEEE 1149.4," in *2007 IEEE International Test Conference*, Oct. 2007, pp. 1-9, doi: 10.1109/TEST.2007.4437629.
[7] S. Kannan, "Automatic test program generation and novel test techniques for testing radio frequency and high-voltage device interface boards," Theses and Dissertations - Department of Electrical & Computer Engineering (ECE), 2013, [Online]. Available: https://ir.ua.edu/handle/123456789/1705
[8] N. S. Rai, N. Palecha, and M. Nagarai, "A brief overview of Test Solution Development for Semiconductor Testing." *2019 4th International Conference on Recent Trends on Electronics, Information, Communication & Technology (RTEICT)*, 2019, pp. 205-209, doi: 10.1109/RTEICT46194.2019.9016857.
[9] S. Kannan and B. C. Kim, "Automatic diagnostic tool for Analog-Mixed Signal and RF load boards," in *2009 International Test Conference,* Nov. 2009, pp. 1-1, doi: 10.1109/TEST.2009.5355836.
[10] P. N. Variyam and A. Chatterjee, "Enhancing test effectiveness for analog circuits using synthesized measurements," in *Proceedings. 16th IEEE VLSI Test Symposium*, 1998, pp. 132-137, doi: 10.1109/VTEST.1998.670860.
[11] L. Nichols, D. Lowenstein, and J. LaGrotta, "Ate system level calibration and its impact on cost, quality and schedule," in *2014 IEEE AUTOTEST*, 2014, pp. 1-7, doi: 10.1109/AUTEST.2014.6935113.
[12] K. Vanitha and C. A. S. Moorth, "Implementation of an integrated FPGA based automatic test equipment and test generation for digital circuits," in *Proc 2013 International Conference on Information Communication and Embedded Systems (ICICES),* Chennai, 2013, pp. 1-6, doi: 10.1109/ICICES.2013.6508284.
[13] C.-T. Chiang and Y.-C. Huang, "A 12-bit multi-channel non-calibrating dual-mode successive approximation adc for power management bus (pmbus) devices," in 2008 *IEEE Instrumentation and Measurement Technology Conference*, 2008, pp. 568-572, doi: 10.1109/IMTC.2008.4547101.
[14] R. V. White and D. Durant, "Understanding and using pmbus/spl trade/ data formats," in *Twenty-First Annual IEEE Applied Power Electronics Conference and Exposition*, 2006, doi: 10.1109/APEC.2006.1620636.
[15] M. Shivakumar, B. S. Premananda, and A. Keste, "Automation of device validation using digital power technology and pmbus communication," in *2016 Second International Conference on Cognitive Computing and Information Processing (CCIP),* 2016, pp. 1-6, doi: 10.1109/CCIP.2016.7802855.
[16] R. V. White, "Pmbus: A decade of growth: An open-standards success," *IEEE Power Electronics Magazine*, vol. 1, no. 3, pp. 33-39, 2014. doi: 10.1109/MPEL. 2014.2330492.
[17] C. Codrea, N. Lucas, and J. Gutierrez, "Implementation and evaluation of digital power management in a medium power conversion module," in *4th International Conference on Integrated Power Systems*, 2006, pp. 1-6.
[18] T. Instruments, "KeyStone Architecture Inter-IC Control Bus I^2C," SPRUGV3, 2011, [Online]. Available: https://www.ti.com/lit/ug/sprugv3/sprugv3.pdf
[19] K. Mattes, "The Osi model," 2020, [Online]. Available: https://karlmatthes.medium.com/the-osi-model-febdecc68c05.
[20] C. Semiconductor, "Smbus block diagram," 2017, [Online]. Available: https://www.cypress.com/documentation/component-datasheets/smbus-and-pmbus-slave.
[21] E. R. Castillo, C. D. Samson, G. N. Ortiz, and M. J. B. Enojas, '14-bit ADC as voltage monitoring device for power supply module 6 using I2C interface," *Indonesian Journal of Electrical Engineering and Computer Science*, vol. 23, no. 2, Aug. 2021, pp. 709-16, 2021, doi: 10.11591/ijeecs.v23.i2.pp709-716.
[22] Teradyne, "Eagle Test Systems – ETS-364," 2021, [Online]. Available: https://www.teradyne.com/products/ets-364/#appconfig
[23] X. Wen, Y. Yamashita, S. Kajihara, L. T. Wang, K. K. Saluja, and K. Kinoshita, "On Low-CapturePower Test Generation for Scan Testing," 23rd IEEE VLSI Test Symposium (VTS'05), 2005, pp. 265-270, doi: 10.1109/VTS.2005.60.
[24] S. E. Thomas and P. R. Nishanth, "Development of Automated Test Equipment for ESP Controllers," in *Proc. 2017 2nd IEEE International Conference on Recent Trends in Electronics, Information & Communication Technology (RTEICT),* Bangalore, 2017, pp. 869-872, doi: 10.1109/RTEICT.2017.8256721.
[25] A. Muttaqin, Z. Abidin, R. A. Setyawan, and I. A. Zahra, "Development of Advanced Automated Test Equipment for Digital System by Using FPGA," *Indonesian Journal of Electrical Engineering and Computer Science*, vol. 15, no. 2, pp. 661-670, Aug. 2019, doi: 10.11591/ijeecs.v15.i2.pp661-670.
[26] X. Weikun, Z. Huibin, and Z. Qiuli, "Testing FPGA devices on an Automatic Test Equipment," in *Proc. 2013 IEEE International Conference on Information and Automation (ICIA)*, Yinchuan, 2013, pp. 65-70, doi: 10.1109/ICInfA.2013.6720271.

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