Mitigating board endorsement through re-spinning with surface-mounted device under test pad

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ABSTRACT

The two-part legacy board device under test (DUT) pad has been very useful for testing of microelectronic packages. However, this board has been subjected to many repair endorsements due to open connection of DUT pad and cut traces of the board components as recorded. Board re-spin is used to improve the performance of the test boards in microelectronic packages production. It improves the board development to create more functional printed circuit boards for testing and introduces the use of modern tools and software applied to the schematic creation up to the production board debugging. This paper presents a method of creating test boards for the development and manufacturing of microelectronic packages and integrated circuits. The two-part board is converted into a single board interface which eliminates the open DUT connections. A surface-mounted DUT pad is introduced to replace the old hypertact pins which are included in the re-spin board for a more robust performance. The schematic creation and board debugging were done to lessen problems caused by connection faults. In result, producing re-spin boards mitigates board endorsement which in return increases the manufacturing output performance. A faster and convenient setup was achieved when the old two-board setup was eliminated.

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1. INTRODUCTION

In the production of microelectronic packages and integrated circuit (IC) products, printed circuit board (PCB) test boards are normally used [1], [2]. It includes the two-part legacy boards which are widely used for testing ICs. These legacy boards are subjected to many endorsements for repair as in the study conducted by one of the leading semiconductor manufacturers in the Philippines in 2018 as presented in Figure 1. Most of the problems encountered based on these endorsements are due to open connection of device under test (DUT) pad and cut traces, which has 60 counts of endorsements. The second largest according to this graph is the defective passive components with 34 counts of endorsements. This project was done in order to improve the connection of the board design by integrating the two-part legacy board interface design to a single board interface design. Both the layout connection will be improved and minimize or eliminate, if possible, the open DUT pad connection of the board. Furthermore, the placement of the component to a single board is maximized.

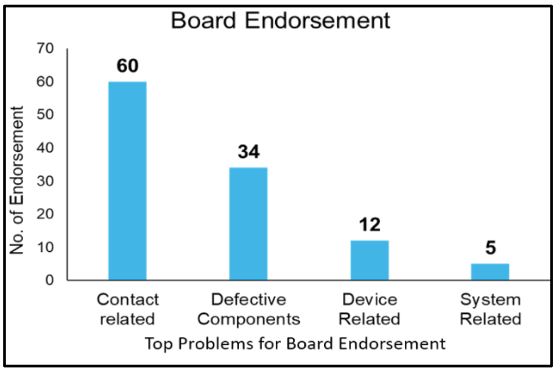


Figure 1. Board endorsement record of 2018

The DUT board, contactors, and the automatic test equipment (ATE). A device under test (DUT) board is a PCB which links the ICs and other test head. It is attached to the ATE [3]–[7] for testing microelectronic packages and other test equipment [8]. To speed testing of IC packages, [9] have presented a method to handling information to be tested in ATE. The ATE configuration needs contactors which matches DUTs, as some of it are based on patterns of testing [10]. Flexible and reconfigurable designs of ATE for mixed signal devices were presented [11] in which configurations play critical roles for different types of microelectronic packages. One of the needed components for configuration is the selectrion of contactors and its assembly, such as presented by [12] in which the electrical and mechanical properties required must be met. The existing test handler must conform to the assembly of contactors for testing the microelectronic devices.

Several variations of ATEs were modeled with the application of information technology to optimize tests and evaluation of DUTs. The ATE is a machine that is designed to perform tests on different DUTs [13]–[16]. Applications of ATE to total or comprehensive check of devices were also displayed by [17], [18]. Mixed signal systems with analog functions can also be tested using digital test channels of ATEs which was presented by [19].

Re-spinning and replacements. The two-part legacy board DUT pad is utilizing a hyper-tact contact design which is prone to contact failure. By re-spinning the board, its design is improved including the DUT pad [20]. The surface mounted DUT pad will be a replacement of the old hyper-tact contact design which will also be included upon the board re-spin to stabilize the connection of the board to the DUT pad. The two-part legacy board design is frequently subjected to re-soldering of the DUT pad connections and jump wires leaving traces on board components. The replacement of defective components is recurrent in the repair which is prone to a worst case of sending the board for offsite repair of defective hyper-tact connector pin which is so costly.

This paper presents a solution in mitigating the board endorsement due to open DUT pad connections and traces and re-spin the two-part board into a single board interface (SBI). The DUT pad connection using hyper-tact pin contact was replaced with surface mount contact [21] which turned out to minimize the repair and maintenance. This setup makes a more stable and secure connection of the board DUT pad to prolong the board life span. These are verified through correlation of data between the old and the new board performances.

2. RESEARCH METHOD

2.1. Re-spinning the two-board into an SBI

The board re-spin project needs several steps of process to make the re-spin [22]. It takes weeks to do a single process to ensure and eliminate the error that may come across during the process. Board re-spinning provides innovation to adapt to new technology and enhances the board design to a new way of the contact DUT pad. Components are being updated which prolongs the life span of the board. The functionality between the board is compared but with expectations of almost the same output in test parameters. Figure 2 presents the two the re-spinning of the two-board setup into an SBI.

The two-board setup consists of the adapter board and the DUT board. The board design is outdated, and the compatibility of the board is at random for both the adapter board and the DUT board and the connection of the DUT pad is uncertain for any loss or open connection. The DUT board has direct contact from the DUT during testing. This board holds the major parts of the components that includes operational amplifiers like digital-to-analog (DAC), analog-to-digital (ADC), passive components, relays, and other different integrated circuits which are needed by the DUT to test its functionality. All the large relays are mounted in the adapter board. It serves as the direct interface connection from the automated test equipment resources which is compiled serially in a board cage. Every slot is labeled according to its function to easily identify the signal connection of the board coming from the resources.

The newly re-spin board is an SBI with a DUT pad. This board eliminates the compatibility problem and zeroed the open contact connection repair of contact DUT pad. This printed circuit board has the same function in terms of testing an IC product. It holds all the components in an organized and immense space compared to the old board and it simplifies the function of the two-part board by catering its components and connection to a single printed circuit board interface. The re-spin board is much easier to debug given that the measuring of the signal is much easier during probing of pins of the component. The new re-spin board has its contact DUT pad modified where this action takes place during the schematic entry process. The comparison between the old and the new DUT pad is presented in Figure 3. The DUT pad was changed from a hyper-tact contact connection to a surface mounted contact connection which eliminates the open connection of the contact DUT pad.

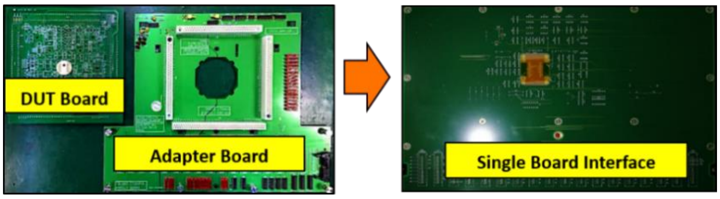


Figure 2. Converting two-board into and SBI

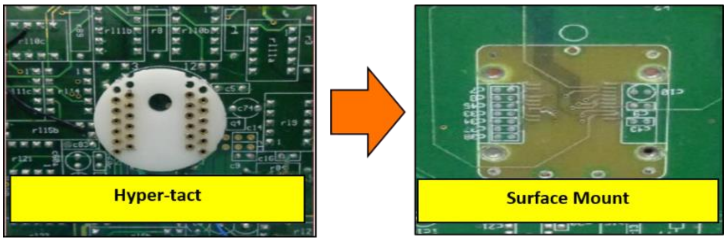


Figure 3. Contactor and DUT pad comparison

2.2. The flow processes

The flow process of the board re-spin methodology from software to hardware is presented in Figure 4. The first step is the schematic entry followed by the design layout of the PCB into a Gerber file [23], [24]. The Gerber file will be sent to the board fabrication houses to fabricate and assemble the board and its components. After the board is fabricated, debugging and correlation of the board will follow to test its functionality.

The schematic entry is the process of creating or updating the schematic diagram of the board circuitry using CAD tool software where every component of the board is declared together with its description and specification. This process enables the updating of the board with new compofnents when the old components are obsolete. A library folder is attached in the CAD tool software to check for component replacement available to the obsolete component. A generated excel file will be provided in every schematic design which contains the bill of materials (BOM) of the board. Once the schematic design is finished it will now move or enter for PCB layout. See Figure 5 for the re-spin block diagram.

The hardware design or the footprint change is the process of PCB layout which determines the actual output or physical appearance of the board. This process includes the board traces and connection layout to every component of the board. After finishing the layout, it will save to a Gerber file format which will be sent to the board fabrication house together with the BOM. The hardware fabrication process includes the layer imaging, layer etching, drilling, plating, masking, surface finish, silkscreen application, continuity testing, profiling and packaging. A flying probe is used to check the continuity of the board in its test points. Visual checking machine is used to check the right size and alignment of the drilled hole for “via”. After all this step, the fabricated board is now moved for assembly.

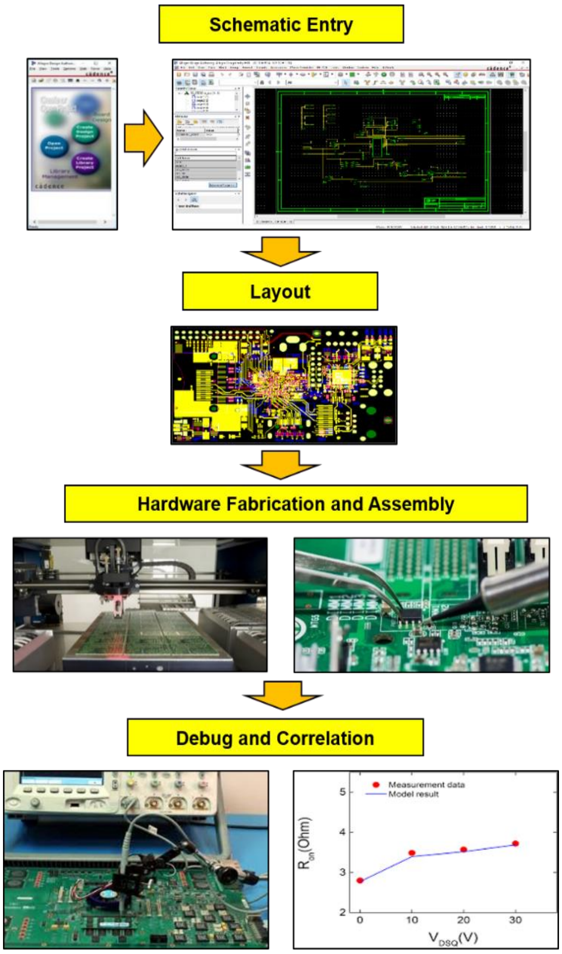


Figure 4. The board re-spin process flow from software to the hardware development

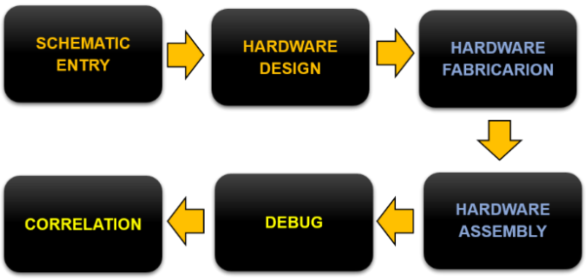


Figure 5. The re-spin board process block diagram

Hardware assembly is the process wherein the installation or soldering of the board components is being done which is referred to in the BOM. There are semiconductor companies that require the component to be in compliance to the restriction of hazardous substance (RoHS) component to be installed to the board [25]. After all the components are installed, the fabricated board is now ready for debugging.

To test the functionality of the board, debugging is done along with the board check test. It includes debugging to the component level, cross probing of the schematic drawing of the old board design to the new board design, manipulating the source of the automated test equipment to check if the current, voltage, and other signals are being applied to the component of the board. A debugger software tool helps determine the failure of the test parameter [26]. To compare the old and the new board correlation is used where the data from serial testing of the known good unit device are compared with respect to each parameter to determine the performance and functionality [27]. Once the old and new board is correlated, it is now ready for production.

2.3. Tests and evaluation

Debugging the re-spin board is done to pass all the parameters needed in the board check test. It is a requirement for every board to check the functionality and reliability of components for the new re-spin board prior to the device testing. It includes checking and measuring all the connections of the board, its relays, all the passive components, and all the signal connections of the operational amplifier. All of the components are at their ready state or default state condition.

After the software debugging modification of the test program is needed in the engineering environment. This modification is called the program load file compilation. This test method enables the debugger tool during loading of the board check testing program. The debugger tool helps entrapping failing parameters and saves breakpoints for failing parameters of the board check test. It checks the status of the signal channels in terms of voltage and current, identifies the source of testing, states the status of relay in real time and shows the step by step testing of the program’s parameter.

Once the board check is passed all the parameters, the new re-spin board undergoes serialized testing of five known good units. Loop testing is then performed about 30 times for every device. The old board will undergo the same procedure of serialized testing using the five known good units used for the new re-spin board with 30 times loop test for data gathering.

3. RESULTS AND DISCUSSION

3.1. PCB re-spin fabrication and tests results

A single board interface with new DUT pads with surface mount contact mechanism replaced the old board. The final physical re-spin board was fabricated as presented in Figure 6. Ready for board check test, debugging and data gathering for correlation to the old board. Some of the problems encountered during the board check test are listed in Table 1.

To correct this failure, the board debugging is needed to isolate the problem and to satisfy all the test parameters of the board check test. Data logging the parameter of the board check during testing is advised to capture and identify the reading of the failed parameter compared to the upper and lower limit of the parameter. Printed schematic drawing of both old and new re-spin board is needed during debugging to aid for the comparison and traceability of connection during probing of traces and the signal input/output of components connection.

Figure 6. The fabricated re-spin board-an SBI with new with surface mount DUT pads

Table 1. Parameter failure board check

Board Check Test Failure	Analysis	Corrective Action	Remarks
(-) 10 V_{ref} Bias to IC5 buffered to IC4	1. Output signal of IC4 op-amp is connected to the +5 V supply coul of relay 14. 2. Incorrect connection of series-parallel resistor input at relay 5.	1. Cut the signal connection of IC4 to the coil of relay 14 and correct connection to pin 2. 2. Cut the series-parallel connection at pin 7 of relay 5. Reroute the connection of the series connection to the pin 5 of relay.	Four voltage reference Bias passed.
Relay check and IC offset	Incorrect connection of 4-channel signal of A to D verified by focusing a 0101 but code to MUX	Correct and interchange the input channel signal to D-A	Relay check and IC offset passed
Channel chek dB13	High voltage supply is measured from the signal. Lose connection of signal is found at the output opin5 of relay 3.	Connect the signal fo db13 form pin 5 of relay 3 to pin6 of relay 2.	Channel check passed.

The usage of software's status tool in signaling voltage and current manipulation is presented in Figure 7. The status tool displays the status of the signals, channels and relays. For example, a +5 V supply voltage is manually drawn from the ATE resources to test the relay's coil and contacts. The measurement can be done using a digital voltmeter by probing to the board's "vias" which are scattered on the board component's input and output traces. This helps a lot in debugging the board and for checking if the induced signal from the ATE is reflected to the voltmeter's reading.

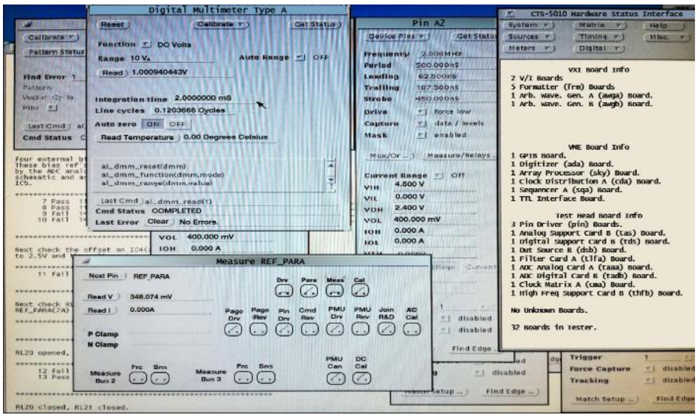
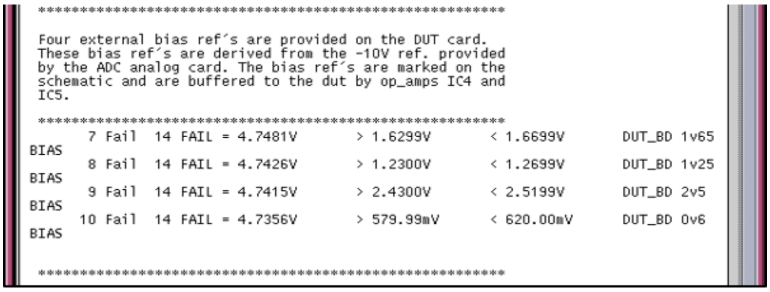


Figure 7. The ATE status tool used to monitor the voltage and current signal manipulation

The failed parameters example for test parameters 7-10 is presented in Figure 8. As an example, the checking and comparing of the schematic's incorrect connection of resistor to pin 5 of relay no. 14 is shown in Figure 9. This was verified at component probing upon checking of signal and forcing voltage to toggle the coil of the relay using automated test equipment resources. An open connection was observed during the test probing. Re-routing is done to sustain the connection of the series resistor to the pin 5 of relay no. 14.



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******************************************************
Four external bias ref's are provided on the DUT card.
These bias ref's are derived from the -10V ref. provided
by the ADC analog card. The bias ref's are marked on the
schematic and are buffered to the dut by op_amps IC4 and
IC5.
******************************************************
      7 Fail  14 FAIL = 4.7481V    > 1.6299V    < 1.6699V    DUT_BD 1v65
BIAS
      8 Fail  14 FAIL = 4.7426V    > 1.2300V    < 1.2699V    DUT_BD 1v25
BIAS
      9 Fail  14 FAIL = 4.7415V    > 2.4300V    < 2.5199V    DUT_BD 2v5
BIAS
     10 Fail  14 FAIL = 4.7356V    > 579.99mV   < 620.00mV   DUT_BD 0v6
BIAS
******************************************************
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Figure 8. Example of display of failure in test parameters 7, 8, 9, and 10

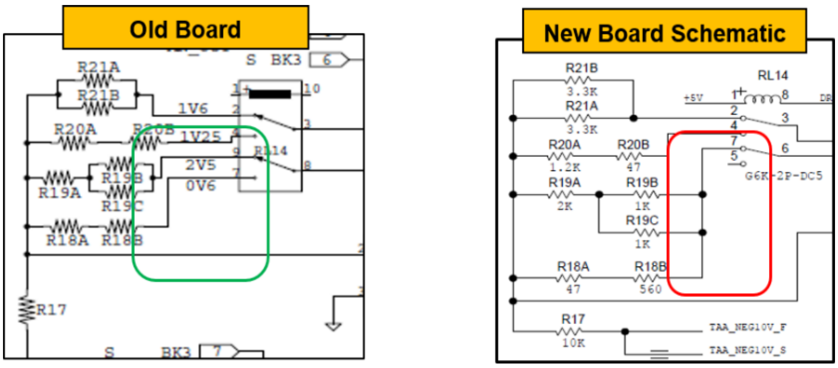


Figure 9. Pin connection of ATE signal to relay 14

Another example of connection is presented in Figure 10. The output signal connection of the buffer amplifier is connected to the +5 V pin supply of the relay coil. To correct the connection, re-routing the output signal to pin2 of the relay is done. This action was verified upon tracing the +1 V signal that is forced to the buffer. It was found out that the signal was not able to flow to the pin 3 connection of the relay no. 16. With the adjustments and corrections on connection traces made, the parameters 7, 8, 9, and 10 passed the board check test after checking and validating the working circuitry based on the old and new schematic of the board as presented in Figure 11. Relay check ensures the functionality of the board signal switching during testing [28] which was presented in Figure 12. This relay acts as a switch for the transmission of current and voltage signals from one channel to another, from an op-amp to the board components for signal processing.

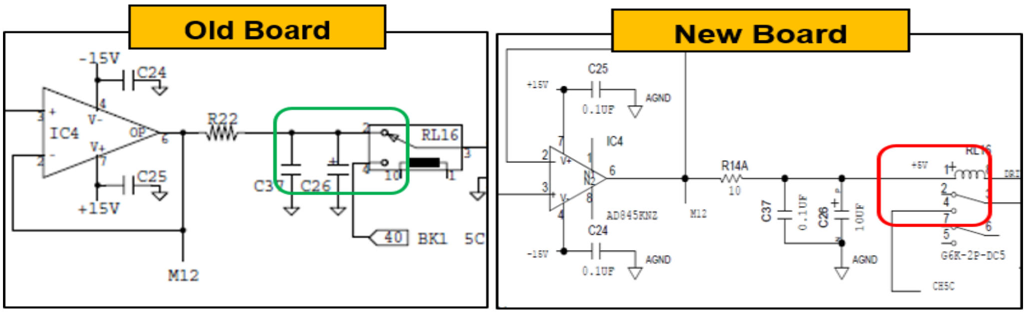


Figure 10. Output signal connection of buffer op-amp to relay 16

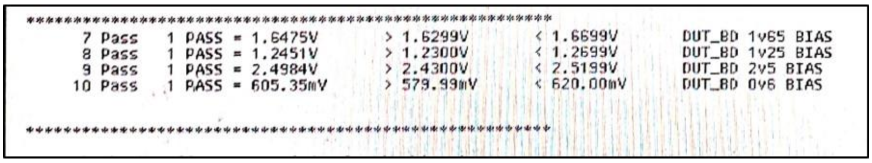


Figure 11. Display of passed test parameters 7, 8, 9, and 10

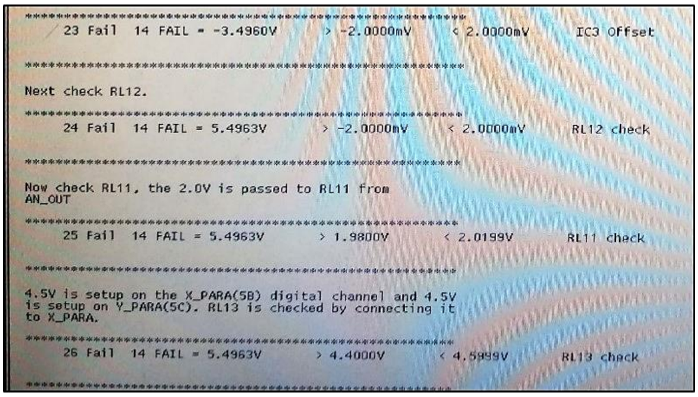


Figure 12. Relay check parameter failed

Multiplexer (MUX) signal connections checks were also done using the new board with its schematic shown in Figure 13. In this diagram, the channels A to D to MUX input were connected incorrectly. The inverted LSB and MSB leads to the mis-signal switching of the MUX. This causes the failure of the relay checking. Incorrect bit output was observed upon manually forcing +5 v to the input of channels. A 0101-bit signal combination as a sample is set to switch the MUX which is incorrect based on the truth table provided on the data sheet of the MUX IC. To correct it, interchanging and correcting the connection of the input channel signal from A-D to D-A results in a 0101-bit signal, which verifies the provided truth table of the MUX IC.

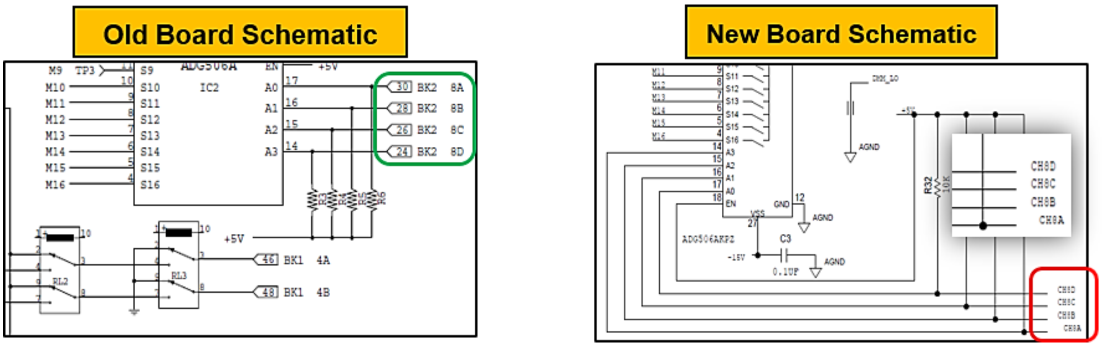


Figure 13. Channel A to D input to 8/16 Bit MUX IC

With adjustments in connections, the relay check parameters finally passed. The last parameter that the board check test is the signal check from the ATE resources. There were failed parameters upon signals checking as shown in Figure 14. A cut signal connection from pin no. 5 of relay 3 to pin no. 6 of relay 2 was also observed as seen in Figure 15. These parameter failures are due to lost signal of signal 4 B upon entering the relay pin no. 6 of relay no. 3. After all the verification, debugging, probing and tracing of connection of the new re-spin board, the board check test is now successfully passed and satisfied all the parameters. Repeatability test is executed to test the consistency of board check. To add to its consistency, the board is verified and tested to another ATE platform.

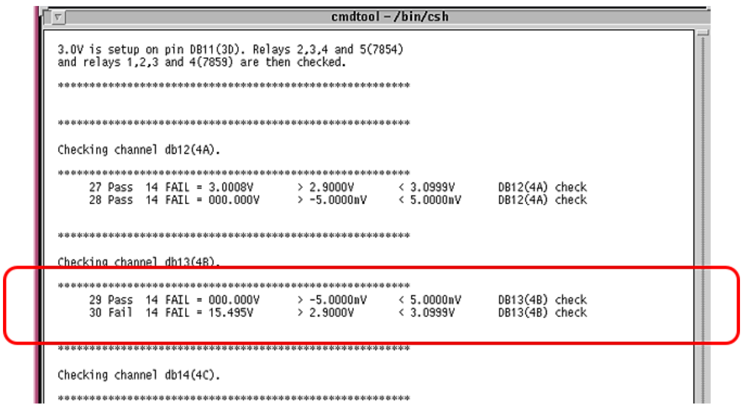


Figure 14. Channel signals checking

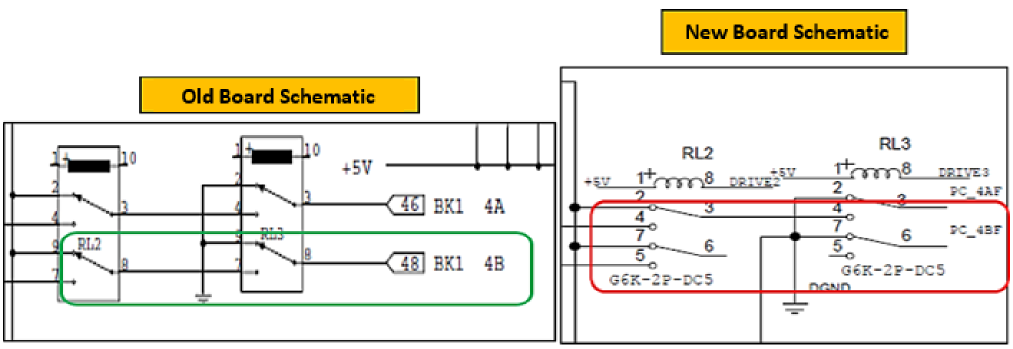


Figure 15. Lost connection on signal 4b

The passed parameters test result of the board check test is presented in Figure 16. The new and the old board will undergo serialization device loop testing which consists of five known good devices when all the parameters passed. These data gathered in the loop test are correlated using a software application. Through this process the reading of each parameter is determined by means of standard deviation and mean shift reading graph with percentage limit to determine if the test parameters have passed or failed. Four common parameter failures encountered after correlating the data gathered. This does not mean that the new re-spin board is not functioning compared to the old board, rather, these are common failures that can also be seen using the old board in testing those products. These common test parameter failures are presented in Table 2. To check the correlation of each parameter, a software tool is used to graph and compare the parameter reading of both boards. The graph of each failed parameter is passed, keeping within the limit of the parameter as shown in Figure 17. The new respin board, compared with the erratic data plot of slew rate and Ios Vs test parameters in Figures 17(a)-(c), has stable output as shown in Figure 17(d). Thus, the deviation is out of percentage limit for the correlation. It also shows that the new re-spin board has a stable data plot distribution reading compared to the old board with erratic data plot distribution for slew rate testing and Ios Vs testing parameters. The new re-spin board functionality has improved data plots reading in testing the products.

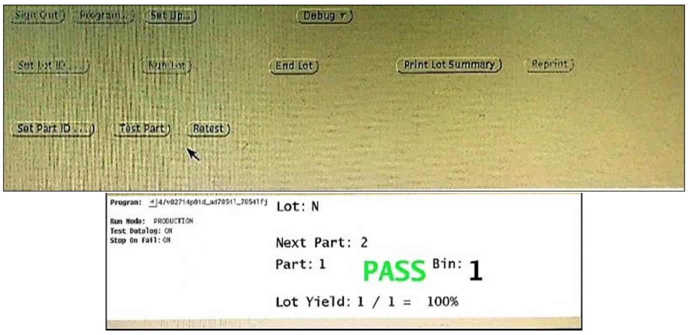
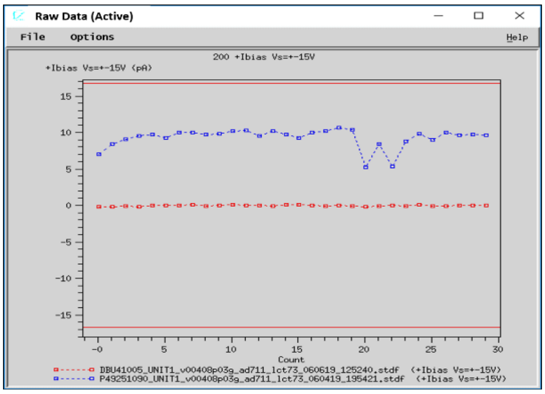
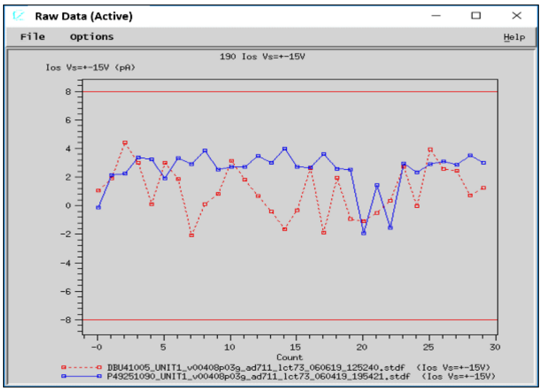


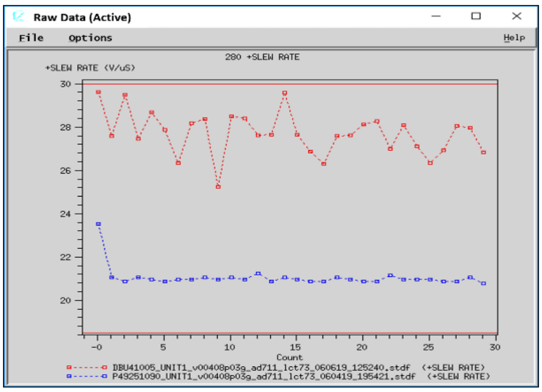
Figure 16. Board check test result



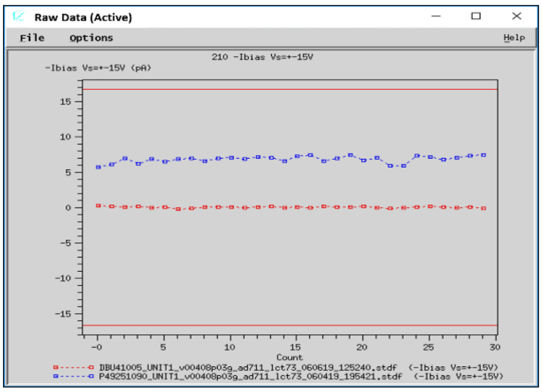
(a)



(b)



(c)



(d)

Figure 17. Failed units' correlation graph: (a) 200 Ibias Vs test, (b) Ios Vs test, (c) Slew rate test, and (d) 210 Ibias Vs test

Table 2. Parameter failure of board check

Test Name	Test Result	Mean Shift Criteria
I_{OS} $V_S = \pm 15$ V	Fail	Fail
+ I_{BIAS} $V_S = \pm 15$ V	Fail	Fail
- I_{BIAS} $V_S = \pm 15$ V	Fail	Fail
+ Slew Rate	Fail	Fail

4. CONCLUSION AND FUTURE WORK

The board re-spin is a solution for most of the board that has been outdated by the fast-growing electronic evolution. It helps to maximize or minimize the size of the board which depend on its usage. The integration of the two-part board to a single board interface gives a better result by reducing the open DUT connection of the board. The replacement of the contact DUT pad into a surface mounted type also gives a good result by eliminating the two-part board compatibility problem. This lessens the offsite repair of the board in replacing the hyper-tact pins connector. The new re-spin board has a better and stable reading supported by the graphs and data plot provided upon the correlation of the board. In the future, re-spinning will be applied to other board components to eliminate jump wires to avoid connection errors. Re-spin will also be applied from a single contact site testing to multiple site testing for increasing the performance of the board.

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